Features

- **Fast**
  - **—CY7C510–45 has a 45-ns (max.) clock cycle (commercial)**
  - **—CY7C510–55 has a 55-ns (max.) clock cycle (military)**
- **Low power**
  - **— I_{CC} (max. at 10 MHz) = 100 mA (commercial)**
  - **— I_{CC} (max. at 10 MHz) = 110 mA (military)**
- **V_{CC} margin 5V ±10%**
- **All parameters guaranteed over commercial and military operating temperature range**
- **16 x 16 bit parallel multiplication with accumulation to 35-bit result**
- **Two's complement or unsigned magnitude operation**
- **Capable of withstanding greater than 1001V static discharge voltage**
- **Pin compatible and functional equivalent to Am29510 and TMC2110**

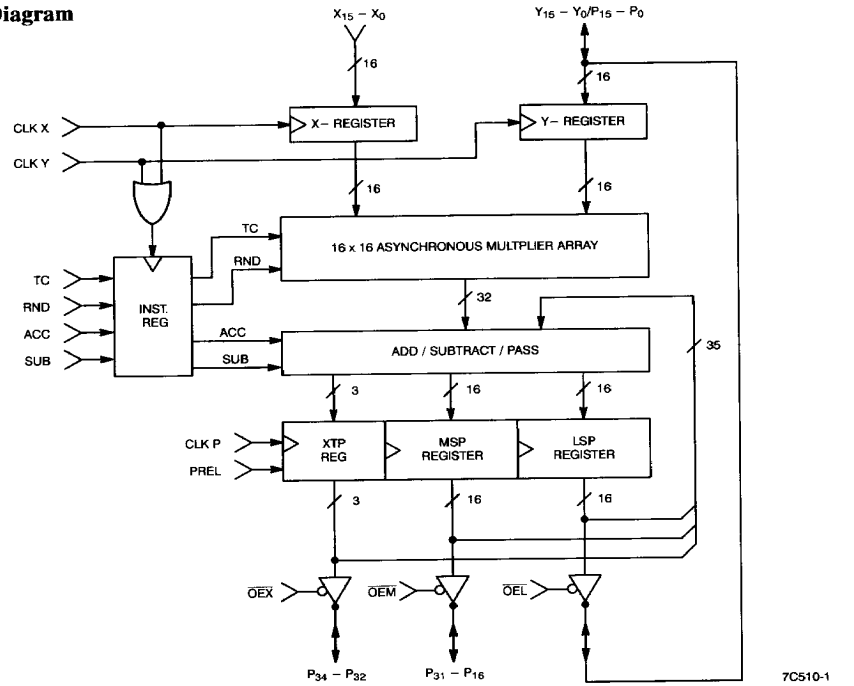
Functional Description

The CY7C510 is a high-speed 16 x 16 parallel multiplier accumulator that operates with a 45-ns clocked multiply accumulate (MAC) time (22-MHz multiply accumulate rate). The operands may be specified as either two's complement or unsigned magnitude 16-bit numbers. The accumulator functions include loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, or preloading the accumulator from the external world.

All inputs (data and instruction) and outputs are registered. These independently clocked registers are positive edge-triggered D-type flip-flops. The 35-bit accumulator/output register is divided into a 3-bit extended product (XTP), a 16-bit most significant product (MSP), and a 16-bit least significant product (LSP). The XTP and the MSP have dedicated ports for three-state output; the LSP is multiplexer with the Y-input. The 35-bit accumulator/output register may be preloaded through the bidirectional output ports.

6 LOGIC

Logic Block Diagram



Selection Guide

		CY7C510–45	CY7C510–55	CY7C510–65	CY7C510–75
Maximum Multiply-Accumulate Time (ns)	Commercial	45	55	65	75
	Military		55	65	75

Functional Description (continued)

The CY7C510 incorporates a 16-bit parallel multiplier followed by a 35-bit accumulator. All inputs (data and instruction) and outputs are registered. The 7C510 is divided into four sections: the input section, the 16 x 16 asynchronous multiplier array, the accumulator, and the output/preload section.

The input section has two 16-bit operand input registers for the S and Y operands, clocked by the rising edge of CLK X and CLK Y, respectively. The four-bit instruction register (TC, RND, ACC, SUB) is clocked by the rising edge of the logical OR of CLK X and CLK Y.

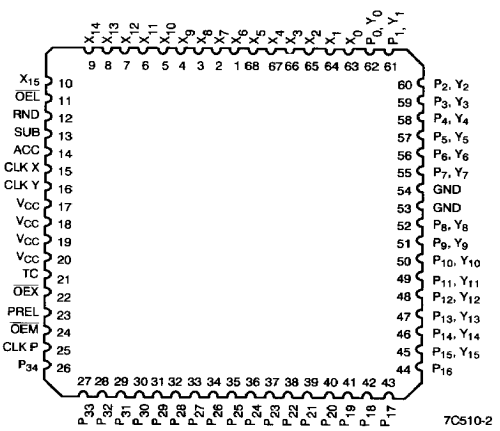
The 16 x 16 asynchronous multiplier array produces the 32-bit product of the input operands. Either two's complement or unsigned magnitude operation is selected, based on instruction bit TC. If rounding is selected, (RND = 1), a "1" is added to the MSB of the LSP (position P_{15}). The 32-bit product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator section.

The accumulator function is controlled by ACC, SUB, and PREL. Four functions may be selected: the accumulator may be loaded with the current product; the product may be added to the accumulator contents; the accumulator contents may be subtracted from the current product; or the accumulator may be preloaded from the bidirectional ports.

The output/preload section contains the accumulator/output register and the bidirectional ports. This section is controlled by the signals PREL, $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$. When PREL is HIGH, the output buffers are in high-impedance state. When the controls $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are also HIGH, data present at the output pins will be preloaded into the appropriate accumulator register at the rising edge of CLK P. When PREL is LOW, the $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ signals are enable controls for their respective three-state output ports.

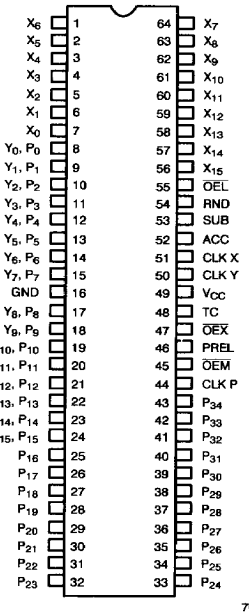
Pin Configurations

LCC/PLCC
Top View



7C510-2

DIP
Top View



7C510-3

PGA
Top View

	51 NC	50 X_{15}	48 RND	46 ACC	44 CLK Y	42 TC	40 PREL	38 CLK P	36 P_{33}	
53 X_{13}	52 X_{14}	49 $\overline{OEL}$	47 SUB	45 CLK X	43 V_{CC}	41 $\overline{OEX}$	39 $\overline{OEM}$	37 P_{34}	35 P_{32}	34 NC
55 X_{11}	54 X_{12}								32 P_{30}	33 P_{31}
57 X_9	56 X_{10}								30 P_{28}	31 P_{29}
59 X_7	58 X_8								28 P_{26}	29 P_{27}
61 X_5	60 X_6								26 P_{24}	27 P_{25}
63 X_3	62 X_4								24 P_{22}	25 P_{23}
65 X_1	64 X_2								22 P_{20}	23 P_{21}
67 Y_0, P_0	66 X_0								20 P_{18}	21 P_{19}
68 NC	1 Y_1, P_1	3 Y_3, P_3	5 Y_5, P_5	7 Y_7, P_7	9 Y_8, P_8	11 Y_{10}, P_{10}	13 Y_{12}, P_{12}	15 Y_{14}, P_{14}	18 P_{16}	19 P_{17}
■	2 Y_2, P_2	4 Y_4, P_4	6 Y_6, P_6	8 GND	10 Y_9, P_9	12 Y_{11}, P_{11}	14 Y_{13}, P_{13}	16 Y_{15}, P_{15}	17 NC	

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Ambient Temperature Under Bias ..... − 55°C to +125°C
Supply Voltage to Ground Potential ..... − 0.5V to +7.0V
DC Input Voltage ..... − 0.5V to +7.0V
DC Voltage Applied to Outputs ..... − 0.5V to V_{CC} Max.
Output Current into Outputs (LOW) ..... 10 mA
Static Discharge Voltage ..... >1001V
(Per MIL-STD-883 Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	− 55°C to +125°C	5V ±10%

Notes:
1. T_A is the "instant on" case temperature.

Preload Function Table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	Output Register XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = Output buffers at high impedance (disabled).
Q = Output buffers at low impedance. Contents of output register available through output ports.
PL = Output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLK P.

Accumulator Function Table

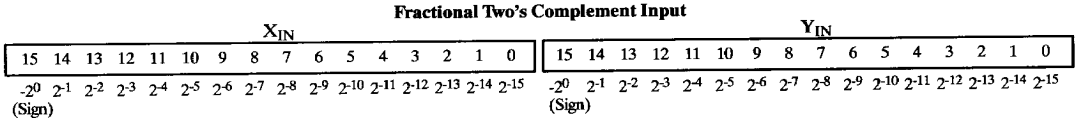
PREL	ACC	SUB	P	Operation
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

Pin Definitions

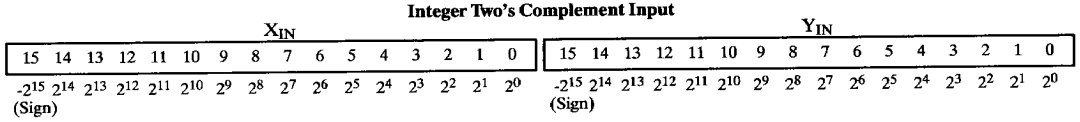
Signal Name	I/O	Description
$X_{15} - X_0$	I	X-Input Data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
$Y_{15} - Y_0$ ($P_{15} - P_0$)	I/O	Y-Input Data/LSP Output Data. When this port is used to input a Y value, the 16-bit number may be interpreted as two's complement or unsigned magnitude. This bidirectional port is multiplexed with the LSP output ($P_{15} - P_0$), and can also be used to preload the LSP register.
$P_{34} - P_{32}$	I/O	Extended Product (XTP) Output Data. This port is bidirectional. The extended product emerges through this port. The XTP register may also be preloaded through this port.
$P_{31} - P_{16}$	I/O	MSP Output Data. This port is bidirectional. The most significant product emerges through this port. The MSP register may also be preloaded through this port.
$P_{15} - P_0$	I/O	LSP Output Data. This port is bidirectional. The least significant product emerges through this port. The LSP register may also be preloaded through this port.
CLK X	I	X-Register Clock. X-Input data are latched into the X-register at the rising edge of CLK X.
CLK Y	I	Y-Register Clock. Y-Input data are latched into the Y-register at the rising edge of CLK Y.
CLK P	I	Product Register Clock. XTP, MSP, and LSP are latched into their respective registers at the rising edge of CLK P. If preload is selected, these registers are loaded with the preload data at the output pins via the bidirectional ports. If preload is not selected, these registers are loaded with the current accumulated product.
$\overline{OEX}$	I	Output Enable Extended. When LOW, the extended product bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the XTP port may be used for preloading. See Preload Function Table.
$\overline{OEM}$	I	Output Enable Most. When LOW, the MSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.
$\overline{OEL}$	I	Output Enable Least. When LOW, the LSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.
PREL	I	Preload. When HIGH, the three bidirectional ports may be used to preload data into the accumulator register at the rising edge of CLK P. The three-state controls ($\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$) must be HIGH to preload data. When LOW, the accumulated product is loaded into the accumulator/output register at the rising edge of CLK P. The output drivers must be enabled ($\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$ must be LOW) for the accumulated product to be output. Ordinarily, PREL, $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are tied together. See Accumulator Function Table.
TC	I	Two's Complement Control. When HIGH, the 7C510 is in two's complement mode, where the input and output data are interpreted as two's complement numbers. The device is in unsigned magnitude mode when TC is LOW. This control is loaded into the instruction register at the rising edge of CLK X + CLK Y.
RND	I	Round Control. When HIGH, rounding is enabled and a "1" is added to the MSB of the LSP (P_{15}). When LOW, the product is unchanged. This control is loaded into the instruction register at the rising edge of CLK X + CLK Y.
ACC	I	Accumulate Control. When HIGH, the accumulator/output register contents are added to or subtracted from the current product (XY) and this result is stored back into the accumulator/output register. When LOW, the product is loaded into the accumulator register, overwriting the current contents. This control is loaded into the instruction register at the rising edge of CLK X + CLK Y.
SUB	I	Subtract Control. When both ACC and SUB are HIGH, the accumulator register contents are subtracted from the current product XY and this result is written back into the accumulator register. When ACC is HIGH and SUB is LOW, the accumulator register contents and current product are summed, then written back to the accumulator register. This control is loaded into the instruction register at the rising edge of CLK X + CLK Y. See Accumulator Function Table.

CY7C510 Input Formats

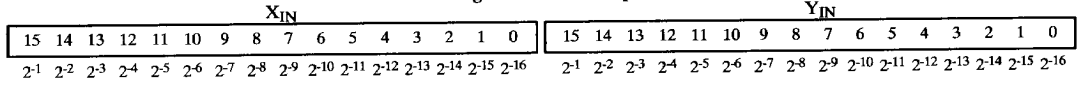
Fractional Two's Complement Input



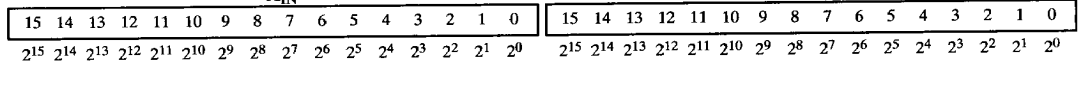
Integer Two's Complement Input



Unsigned Fractional Input

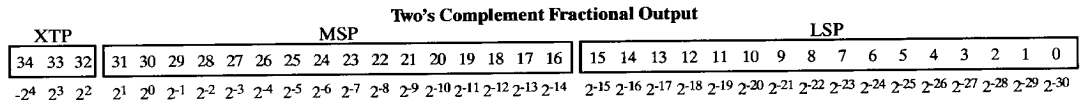


Unsigned Integer Input

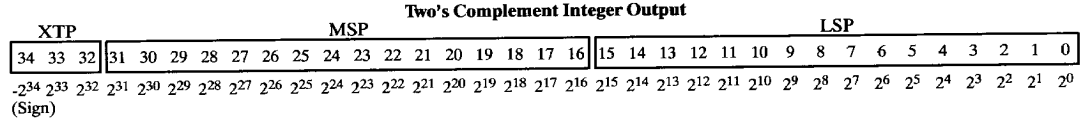


CY7C510 Output Formats

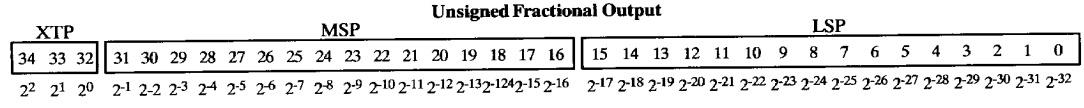
Two's Complement Fractional Output



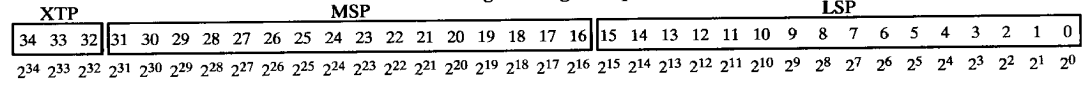
Two's Complement Integer Output



Unsigned Fractional Output



Unsigned Integer Output



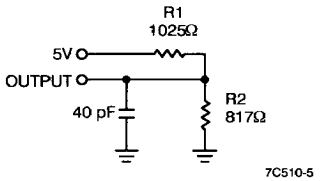
Electrical Characteristics the Over Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 0.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0		V
V_{IL}	Input LOW Voltage				0.8	V
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V		− 0.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V		4.0		mA
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	μA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_{IN} = 7.0V			10	mA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V		− 3	− 30	mA
I_{OZL}	Output OFF (High Z) Current	V_{CC} = Max., $\overline{OE}$ = 2.0V			− 25	μA
I_{OZH}	Output OFF (High Z) Current	V_{CC} = Max., $\overline{OE}$ = 2.0V		25		μA
$I_{CC}(Q_1)$[4]	Supply Current (Quiescent)	V_{CC} = Max., V_{IN} = [GND to V_{IL}] or [V_{IH} to V_{CC}]			30	mA
$I_{CC}(Q_2)$[4]	Supply Current (Quiescent)	V_{CC} = Max., V_{CC} ≥ V_{IN} ≥ 3.85V, 0.4V ≥ V_{IN} ≥ GND	Commercial		20	mA
			Military		25	
I_{CC}(Max.)[4]	Supply Current	V_{CC} = Max., f_{CLK} = 10 MHz	Commercial		100	mA
			Military		110	

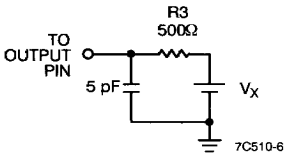
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Output Loads used for AC Performance Characteristics

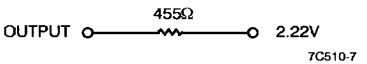


Normal Load (Load 1)



Three-State Delay Load (Load 2)

Equivalent to: THÉVENIN EQUIVALENT



Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. For I_{CC} measurements, the outputs are three-stated. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given frequency, use 30 mA + I_{CC}(AC) where I_{CC}(AC) = (7 mA/MHz) × Clock Frequency for the commercial temperature range. I_{CC}(AC) = (8 mA/MHz) × Clock Frequency for military temperature range.
5. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over Operating Range[2]

Parameters	Description		7C510–45		7C510–55		7C510–65		7C510–75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply Accumulate Time			45		55		65		75	ns
t_S	Set-Up Time		20		20		25		25		ns
t_H	Hold Time		3		3		3		3		ns
t_{PW}	Clock Pulse Width		25		25		30		30		ns
t_{PDP}	Output Clock to P			30		30		35		35	ns
t_{PDY}	Output Clock to Y			30		30		35		35	ns
t_{PHZ}	$\overline{OEX}$, OEM to P; $\overline{OEL}$ to Y (Disable Time)	HIGH to Z		25		25		30		30	ns
t_{PLZ}		LOW to Z		25		25		30		30	ns
t_{PZH}	$\overline{OEX}$, OEM to P; $\overline{OEL}$ to Y (Enable Time)	Z to HIGH		30		30		35		35	ns
t_{PZL}		Z to LOW		30		30		35		35	ns
t_{HCL}	Relative Hold Time		0		0		0				ns

Test Waveforms

Parameter	V_X	Output Waveform—Measurement Level
All t_{PD}'s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	V_{OL}, 0.5V, 2.6V
t_{PZH}	0.0V	0.0V, 1.5V, V_{OH}
t_{PZL}	2.6V	2.6V, 1.5V, V_{OL}

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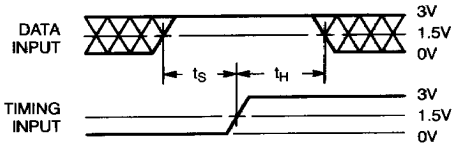
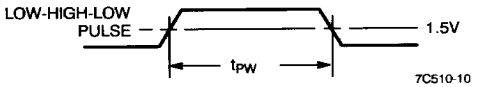
Set-Up and Hold Time[6]



7C510-9

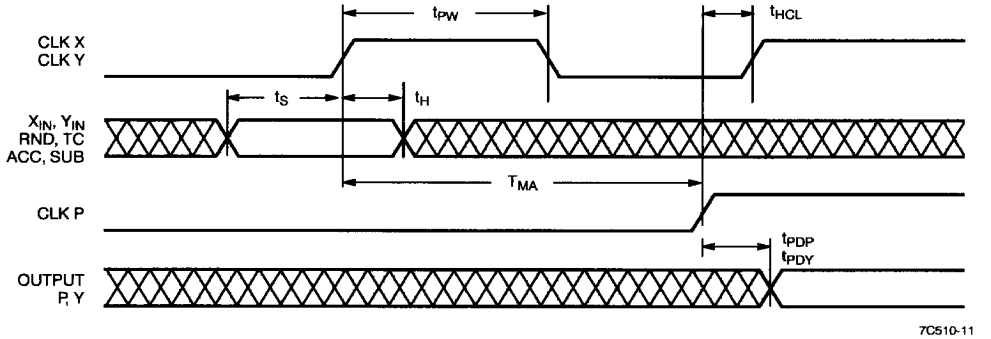
Pulse Width[7]



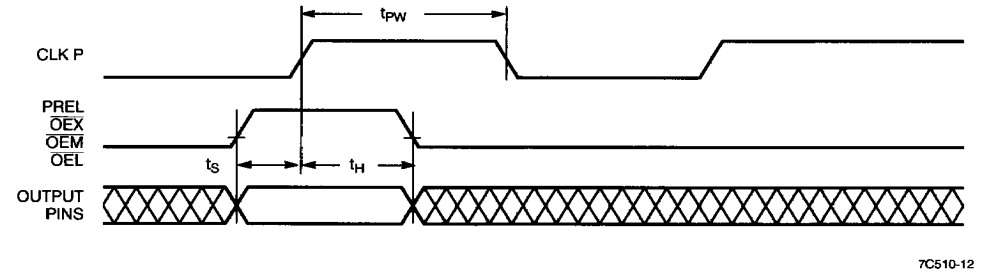
7C510-10

Notes:
6. Cross hatched area is don't care condition.
7. Diagram shown for HIGH data only. Output transition may be opposite sense.

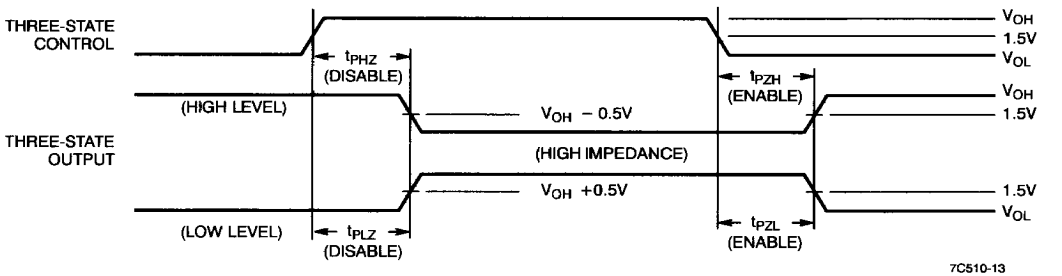
CY7C510 Timing Diagram



Preload Timing Diagram

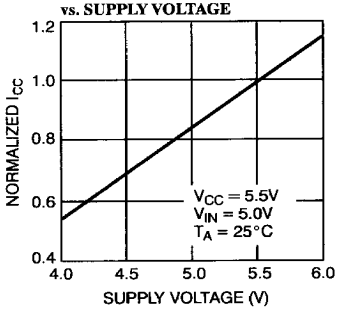


Three-State Timing Diagram

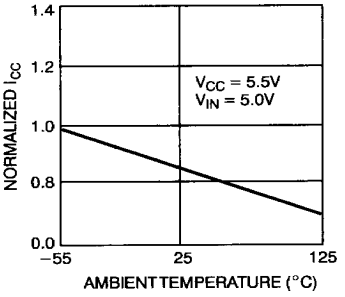


Typical DC and AC Characteristics

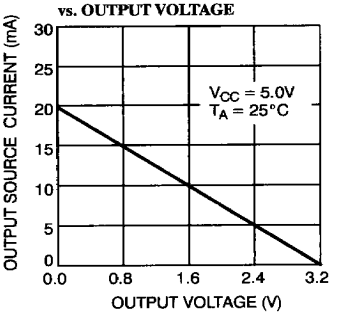
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



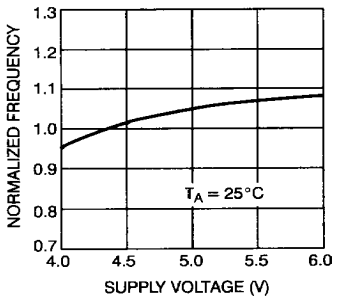
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



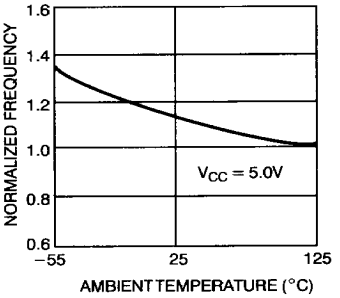
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



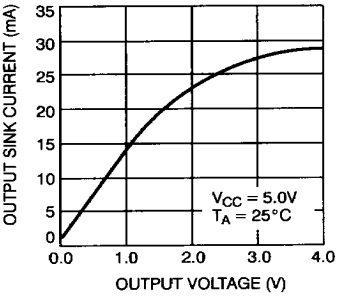
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



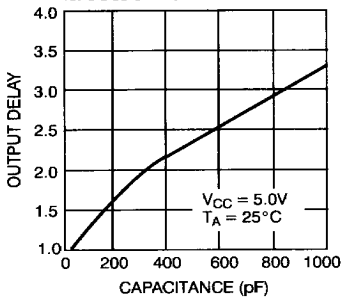
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



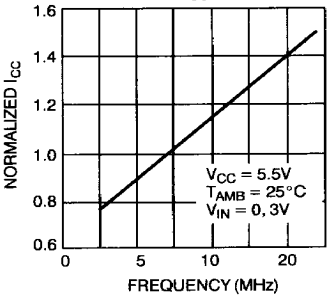
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



7C510-14

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LOGIC

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
45	CY7C510–45DC	D30	Commercial
	CY7C510–45GC	G68	
	CY7C510–45JC	J81	
	CY7C510–45LC	L81	
	CY7C510–45PC	P29	
55	CY7C510–55DC	D30	Commercial
	CY7C510–55GC	G68	
	CY7C510–55JC	J81	
	CY7C510–55LC	L81	
	CY7C510–55PC	P29	
	CY7C510–55DMB	D30	Military
	CY7C510–55GMB	G68	
	CY7C510–55LMB	L81	
65	CY7C510–65DC	D30	Commercial
	CY7C510–65GC	G68	
	CY7C510–65JC	J81	
	CY7C510–65LC	L81	
	CY7C510–65PC	P29	
	CY7C510–65DMB	D30	Military
	CY7C510–65GMB	G68	
	CY7C510–65LMB	L81	
75	CY7C510–75DC	D30	Commercial
	CY7C510–75GC	G68	
	CY7C510–75JC	J81	
	CY7C510–75LC	L81	
	CY7C510–75PC	P29	
	CY7C510–75DMB	D30	Military
	CY7C510–75GMB	G68	
	CY7C510–75LMB	L81	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
I_{IX}	1, 2, 3
I_I	1, 2, 3
I_{OS}	1, 2, 3
I_{OZL}	1, 2, 3
I_{OZH}	1, 2, 3
$I_{CC}(Q_1)$	1, 2, 3
$I_{CC}(Q_2)$	1, 2, 3
I_{CC}(Max.)	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{MA}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{PDP}	7, 8, 9, 10, 11
t_{PDY}	7, 8, 9, 10, 11
t_{PHZ}	7, 8, 9, 10, 11
t_{PLZ}	7, 8, 9, 10, 11
t_{PZH}	7, 8, 9, 10, 11
t_{PZL}	7, 8, 9, 10, 11
t_{HCL}	7, 8, 9, 10, 11

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