CS5340

101 dB, 192 kHz, Multi-Bit Audio A/D Converter

Features

- Advanced multi-bit Delta-Sigma architecture
- 24-bit conversion
- Supports all audio sample rates including 192 kHz
- 101 dB Dynamic Range at 5V
- -94 dB THD+N
- High pass filter to remove DC offsets
- Analog/digital core supplies from 3.3V to 5V
- Supports logic levels between 2.5V and 5V
- Linear phase digital anti-alias filtering
- Auto-mode selection
- Pin compatible with the CS5341

General Description

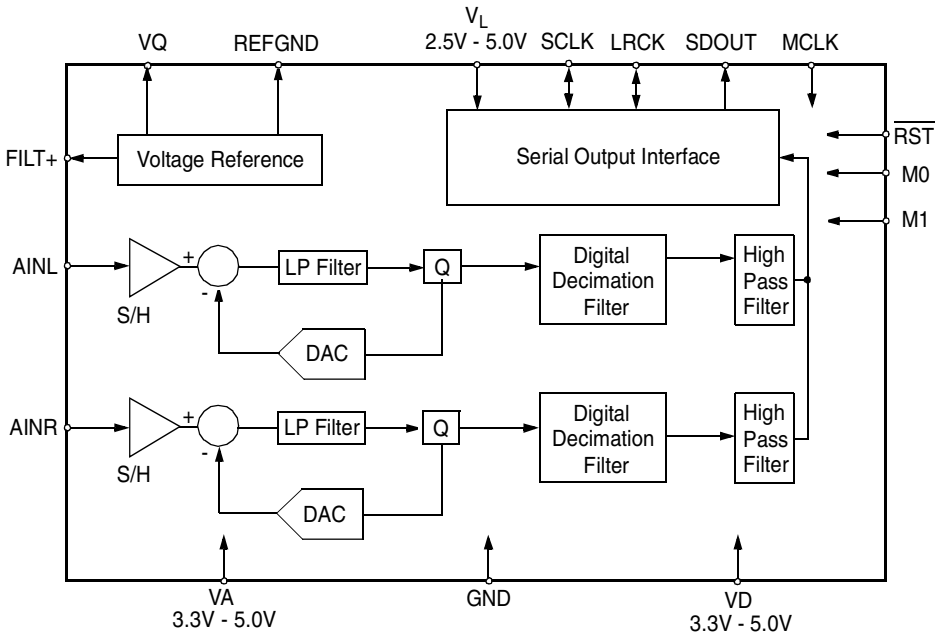
The CS5340 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 200 kHz per channel.

The CS5340 uses a 5th-order, multi-bit Delta-Sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5340 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as set-top boxes, DVD-karaoke players, DVD recorders, A/V receivers, and automotive applications.

ORDERING INFORMATION

CS5340-CZ	-10° to 70° C	16-pin TSSOP
CDB5340	Evaluation Board	



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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To find one nearest you go to **www.cirrus.com/**

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1 CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Analog	VA	3.1	(Note 1)	5.25	V
	Digital	VD	3.1	3.3	5.25	V
	Logic	VL	2.35	3.3	5.25	V
Ambient Operating Temperature	Commercial (-CZ)	T_{AC}	-10	-	70	°C

Notes: 1. This part is specified at typical analog voltages of 3.3 V and 5.0 V. See *Analog Characteristics (CS5340-CZ),* below, for details.

ABSOLUTE MAXIMUM RATINGS

(GND = 0V, All voltages with respect to ground.) (Note 4)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Logic	VL	-0.3	+6.0	V
	Digital	VD	-0.3	+6.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 3)	V_{IN}	GND-0.7	VA+0.7	V
Digital Input Voltage	(Note 3)	V_{IND}	-0.7	VL+0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

3. The maximum over/under voltage is limited by the input current.

4. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

ANALOG CHARACTERISTICS (CS5340-CZ) Test conditions (unless otherwise specified):

Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
VA = 3.3 V						
Single Speed Mode	**Fs = 48 kHz**					
Dynamic Range	A-weighted		92	98	-	dB
	unweighted		89	95	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N				
	-1 dB		-	-91	-85	dB
	-20 dB		-	-75	-	dB
	-60 dB		-	-35	-	dB
Double Speed Mode	**Fs = 96 kHz**					
Dynamic Range	A-weighted		92	98	-	dB
	unweighted		89	95	-	dB
40 kHz bandwidth	unweighted		-	92	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N				
	-1 dB		-	-91	-85	dB
	-20 dB		-	-75	-	dB
	-60 dB		-	-35	-	dB
40 kHz bandwidth	-1 dB		-	-85	-	dB
Quad Speed Mode	**Fs = 192 kHz**					
Dynamic Range	A-weighted		92	98	-	dB
	unweighted		89	95	-	dB
40 kHz bandwidth	unweighted		-	92	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N				
	-1 dB		-	-91	-85	dB
	-20 dB		-	-75	-	dB
	-60 dB		-	-35	-	dB
40 kHz bandwidth	-1 dB		-	-85	-	dB
VA = 5.0 V						
Single Speed Mode	**Fs = 48 kHz**					
Dynamic Range	A-weighted		95	101	-	dB
	unweighted		92	98	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N				
	-1 dB		-	-94	-88	dB
	-20 dB		-	-78	-	dB
	-60 dB		-	-38	-	dB
Double Speed Mode	**Fs = 96 kHz**					
Dynamic Range	A-weighted		95	101	-	dB
	unweighted		92	98	-	dB
40 kHz bandwidth	unweighted		-	95	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N				
	-1 dB		-	-94	-88	dB
	-20 dB		-	-78	-	dB
	-60 dB		-	-38	-	dB
40 kHz bandwidth	-1 dB		-	-91	-	dB
Quad Speed Mode	**Fs = 192 kHz**					

Dynamic Range A-weighted		95	101	-	dB
unweighted		92	98	-	dB
40 kHz bandwidth unweighted		-	95	-	dB
Total Harmonic Distortion + Noise (Note 5)	THD+N				
-1 dB		-	-94	-88	dB
-20 dB		-	-78	-	dB
-60 dB		-	-38	-	dB
40 kHz bandwidth -1 dB		-	-91	-	dB
Dynamic Performance for All Modes					
Interchannel Isolation		-	70	-	dB
Interchannel Phase Deviation		-	0.0001	-	Degree
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error			-	±5	%
Gain Drift		-	±100	-	ppm/°C
Analog Input Characteristics					
Full-scale Input Voltage		0.53*VA	0.56*VA	0.59*VA	Vpp
Input Impedance		18	-	-	kΩ

Note: 5. Referred to the typical full-scale input voltage

DIGITAL FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single Speed Mode (2 kHz to 50 kHz sample rates)					
Passband (-0.1 dB)		0	-	23.5	kHz
Passband Ripple		-	-	0.035	dB
Stopband		27.3	-	-	kHz
Stopband Attenuation		70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
Double Speed Mode (50 kHz to 100 kHz sample rates)					
Passband (-0.1 dB)		0	-	47	kHz
Passband Ripple		-	-	±0.025	dB
Stopband		53.8	-	-	kHz
Stopband Attenuation		69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
Quad Speed Mode (100 kHz to 200 kHz sample rates)					
Passband (-0.1 dB)		0	-	50	kHz
Passband Ripple		-	-	±0.025	dB
Stopband		96	-	-	kHz
Stopband Attenuation		60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
High Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 6)			20	-	Hz
Phase Deviation @ 20Hz (Note 6)		-	10	-	Deg
Passband Ripple		-	-	0	dB

Note: 6. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

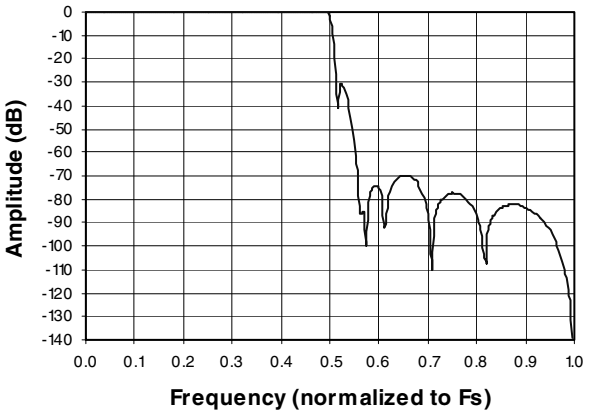


Figure 1. Single Speed Mode Stopband Rejection

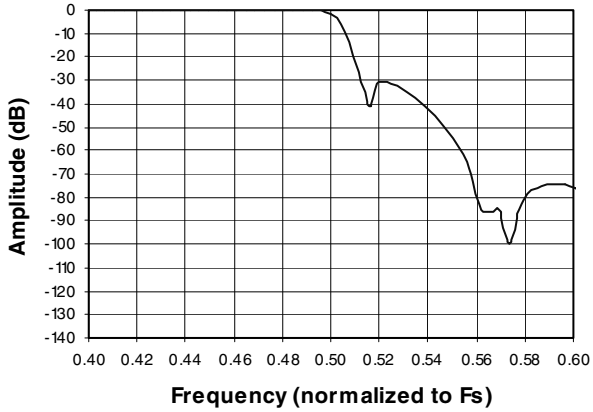


Figure 2. Single Speed Mode Stopband Rejection

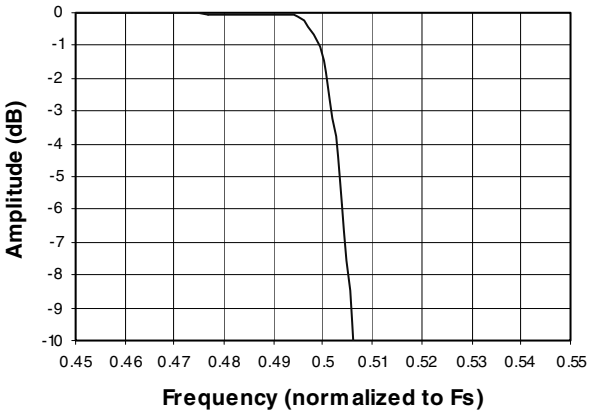


Figure 3. Single Speed Mode Transition Band (Detail)

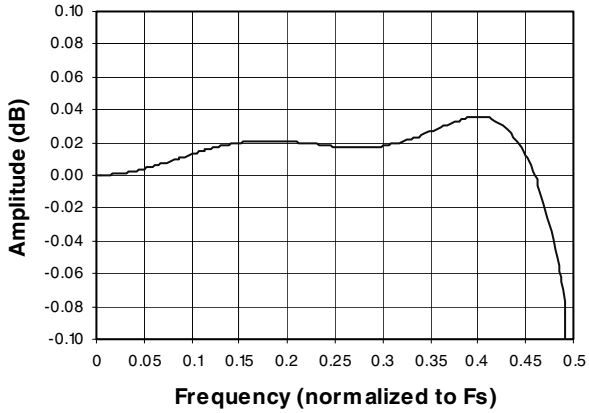


Figure 4. Single Speed Mode Passband Ripple

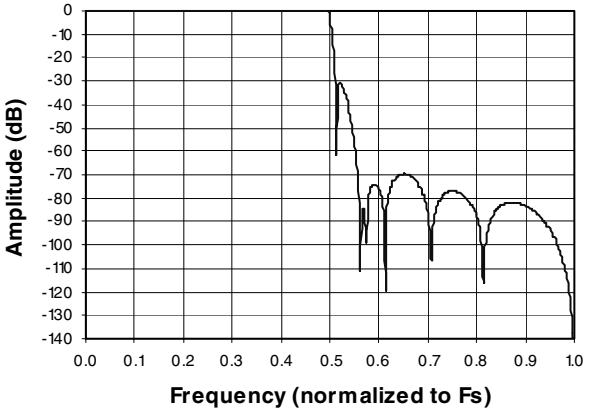


Figure 5. Double Speed Mode Stopband Rejection

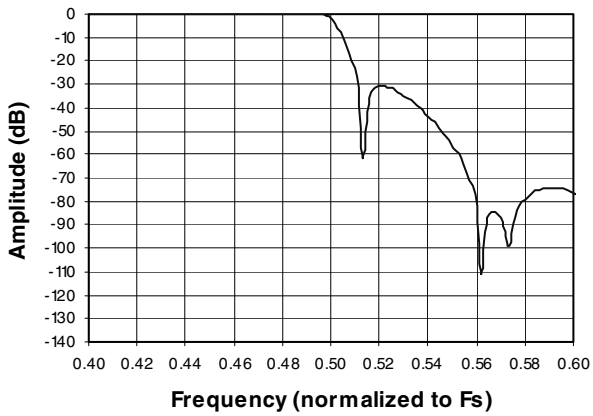


Figure 6. Double Speed Mode Stopband Rejection

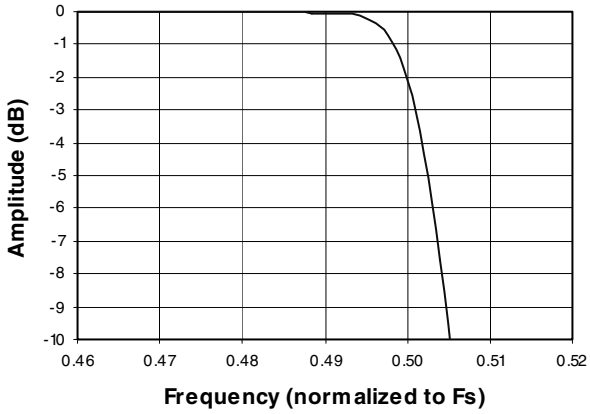


Figure 7. Double Speed Mode Transition Band (Detail)

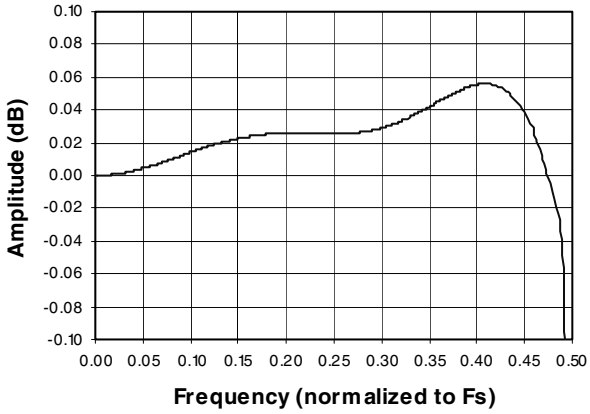


Figure 8. Double Speed Mode Passband Ripple

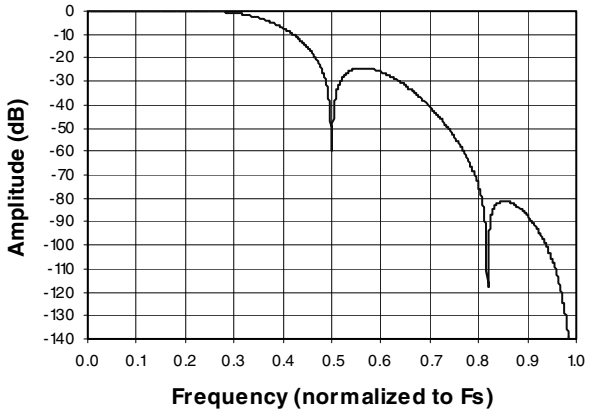


Figure 9. Quad Speed Mode Stopband Rejection

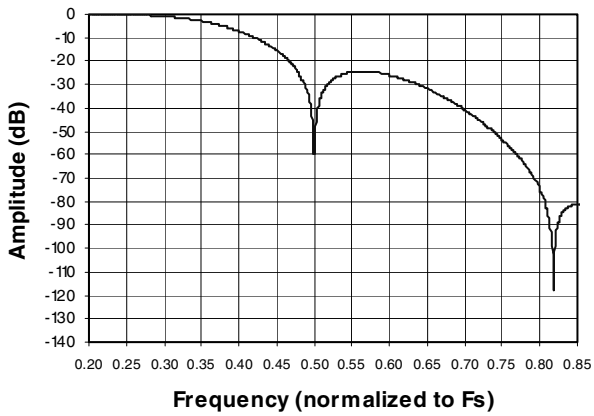


Figure 10. Quad Speed Mode Stopband Rejection

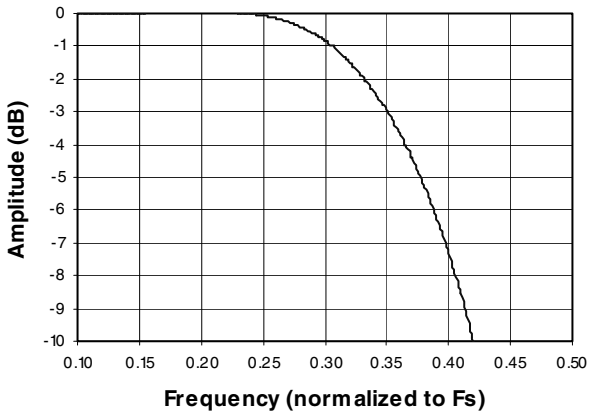


Figure 11. Quad Speed Mode Transition Band (Detail)

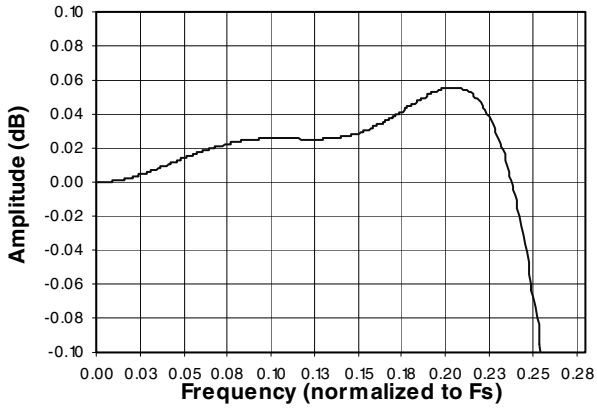


Figure 12. Quad Speed Mode Passband Ripple

DC ELECTRICAL CHARACTERISTICS (GND = 0 V, all voltages with respect to 0V. MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	3.1	-	5.25	V
	Positive Digital	VD	3.1	-	5.25	V
	Positive Logic	VL	2.35	-	5.25	V
Power Supply Current	VA = 5 V	I_A	-	21	23.1	mA
(Normal Operation)	VA = 3.3 V	I_A	-	18.2	20	mA
	VL,VD = 5 V	I_D	-	15	16.5	mA
	VL,VD = 3.3 V	I_D	-	9	10	mA
Power Supply Current	VA = 5 V	I_A	-	1.5	-	mA
(Power-Down Mode) (Note 7)	VL,VD=5 V	I_D	-	0.4	-	mA
Power Consumption	VL, VD, VA = 5 V	-	-	180	198	mW
(Normal Operation)	VL, VD, VA = 3.3 V	-	-	90	100	mW
	(Power-Down Mode)	-	-	9.5	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 8)	PSRR	-	65	-	dB
V_Q Nominal Voltage			-	VA÷2	-	V
Output Impedance			-	100	-	Ω
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	18	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

Notes: 7. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

8. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 100 µA	(% of VL)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_o =100 µA	(% of VL)	V_{OL}	-	-	15%	V
Input Leakage Current		I_{in}	-	-	±10	µA

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Junction to Ambient Thermal Impedance	θ_{JA}	-	75	-	°C/W
Ambient Operating Temperature (Power Applied)	T_A	-10	-	+70	°C

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (Logic "0" = GND = 0 V; Logic "1" = VL, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Output Sample Rate (Master Mode) Single Speed Mode	Fs	2	-	50	kHz
Double Speed Mode	Fs	50	-	100	kHz
Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications					
MCLK Period	t_{clkw}	39	-	1953	ns
MCLK Pulse Width High	t_{clkh}	15	-	-	ns
MCLK Pulse Width Low	t_{clkl}	15	-	-	ns
Master Mode					
SCLK falling to LRCK	t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid	t_{sdo}	0	-	32	ns
SCLK Duty Cycle		-	50	-	%
SCLK Output Frequency		-	50	-	%
Slave Mode					
Single Speed					
Output Sample Rate	Fs	4	-	50	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	156	-	-	ns
SCLK High/Low	t_{sclkhl}	32	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	32	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Double Speed					
Output Sample Rate	Fs	84	-	100	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	156	-	-	ns
SCLK High/Low	t_{sclkhl}	32	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	32	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Quad Speed					
Output Sample Rate	Fs	170	-	200	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	78	-	-	ns
SCLK High/Low	t_{sclkhl}	32	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	32	ns
SCLK falling to LRCK edge	t_{slrd}	-10	-	10	ns

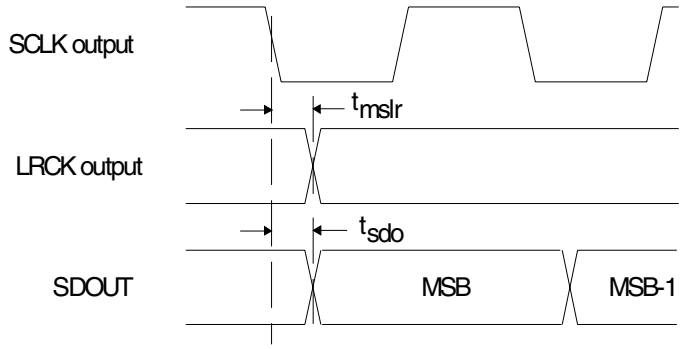


Figure 13. Master Mode, Left Justified SAI

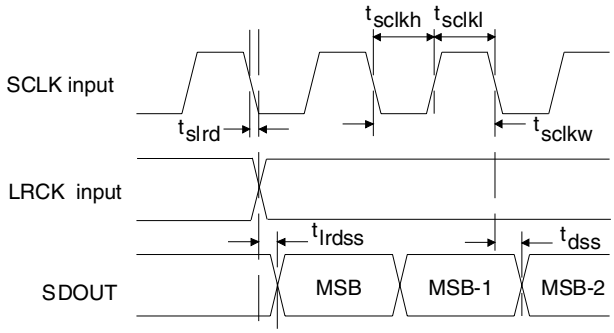


Figure 14. Slave Mode, Left Justified SAI

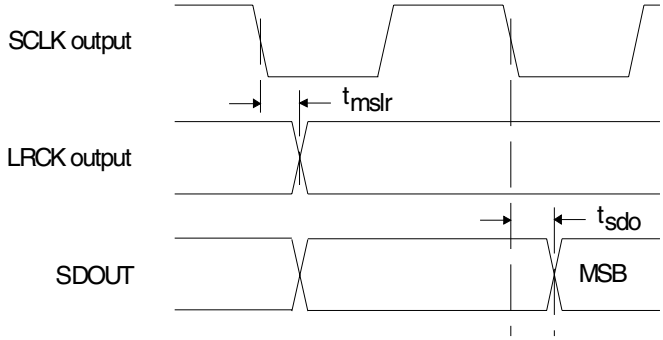


Figure 15. Master Mode, I²S SAI

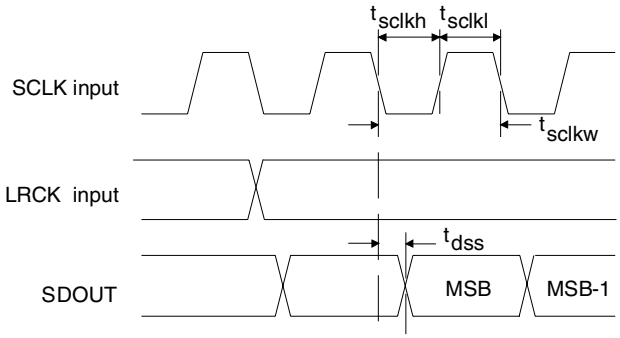
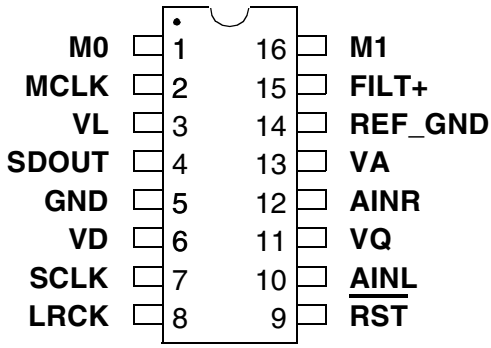


Figure 16. Slave Mode, I²S SAI

2 PIN DESCRIPTION



Pin Name	#	Pin Description
M0 **M1**	1 16	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MCLK	2	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VL	3	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	4	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
GND	5,14	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
SCLK	7	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
LRCK	8	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
$\overline{\text{RST}}$	9	**Reset** (*Input*) - The device enters a low power mode when low.
AINL **AINR**	10 12	**Analog Input** (*Input*) - The full scale analog input level is specified in the Analog Characteristics specification table.
VQ	11	**Quiescent Voltage** *(Output)* **-** Filter connection for the internal quiescent reference voltage.
VA	13	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
FILT+	15	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

3 TYPICAL CONNECTION DIAGRAM

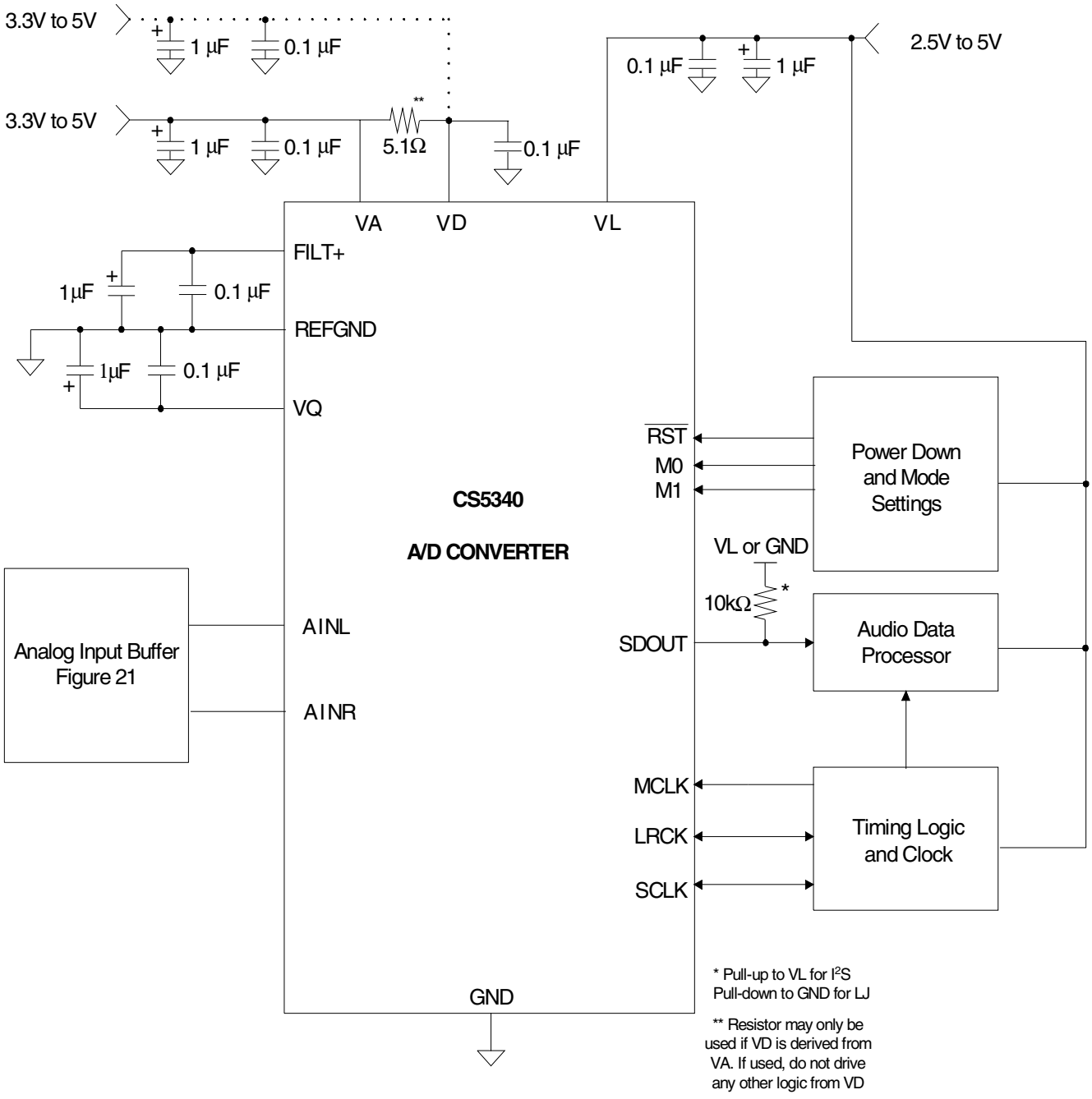


Figure 17. Typical Connection Diagram

4 APPLICATIONS

4.1 Single, Double, and Quad Speed Modes

The CS5340 can support output sample rates from 2 kHz to 200 kHz when operating as a clock master (see Section 4.2 for more information). By definition, Single Speed mode is defined as output sample rates between 2 kHz and 50 kHz. Double Speed mode is defined as output sample rates between 50 kHz and 100 kHz, and Quad Speed mode is defined as output sample rates between 100 kHz and 200 kHz.

The output sample rate ranges listed above are how the speed modes are defined, and do not imply an absolute sample rate specification. If the absolute frequency of the sample rate is increased above that defined for a given speed mode, the analog performance will degrade. This is due to the fact that the analog input is sampling faster than designed and therefore does not have as much time to settle, which adds distortion.

4.2 Operation as Either a Clock Master or Slave

The CS5340 supports operation as either a clock master or slave. As a clock master, the LRCK and SCLK pins are outputs with the left/right and serial clocks synchronously generated on-chip. As a clock slave, the LRCK and SCLK pins are inputs and require the left/right and serial clocks to be externally generated. The selection of clock master or slave is made via the Mode pins as shown in Table 1.

M1(Pin 16)	M0(Pin 1)	MODE	Output Sample Rate (Fs)
0	0	Clock Master, Single Speed Mode	2 kHz - 50 kHz
0	1	Clock Master, Double Speed Mode	50 kHz - 100 kHz
1	0	Clock Master, Quad Speed Mode	100 kHz - 200 kHz
1	1	Clock Slave, All Speed Modes	Refer to Table 2

Table 1. CS5340 Mode Control

4.2.1 Operation as a Clock Master

As a clock master, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 18.

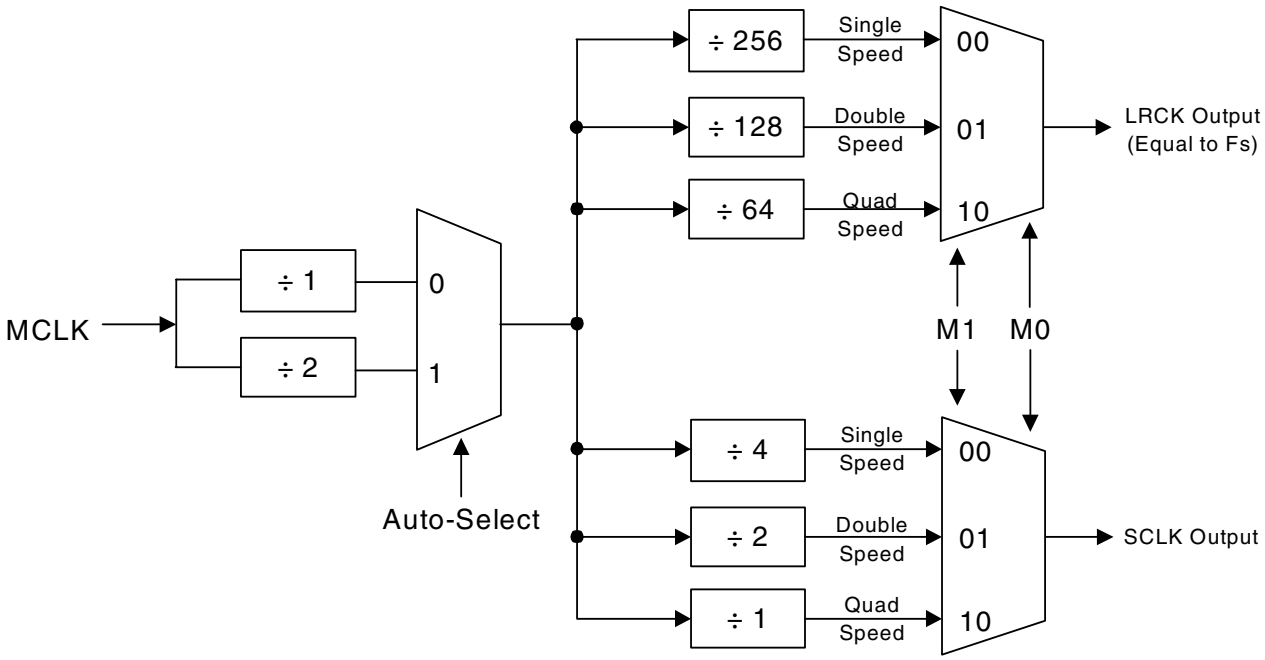


Figure 18. CS5340 Master Mode Clocking

4.2.2 Operation as a Clock Slave

LRCK and SCLK operate as inputs in clock slave mode. It is recommended that the left/right clock be synchronously derived from the master clock and must be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance.

A unique feature of the CS5340 is the automatic selection of either Single, Double or Quad speed mode when operating as a clock slave. The auto-mode select feature negates the need to configure the Mode pins to correspond to the desired mode. The auto-mode selection feature supports all standard audio sample rates from 32 to 200 kHz. However, there are ranges of non-standard audio sample rates that are not supported when operated as a clock slave. Please refer to Table 2.

Output Sample Rate (Fs)	MODE
4 kHz - 50 kHz	Single Speed Mode
84 kHz - 100 kHz	Double Speed Mode
170 kHz - 200 kHz	Quad Speed Mode

Table 2. CS5340 Auto-Detect

4.2.3 Master Clock

The CS5340 requires a Master clock (MCLK) which runs the internal sampling circuits and digital filters. There is also an internal MCLK divider which is automatically activated based on the speed mode and frequency of the MCLK. Table 3 shows a listing of the external MCLK/LRCK ratios that are required. Table 4 lists some common audio output sample rates and the required MCLK frequency. Please note that not all of the listed sample rates are supported in clock slave mode. Refer to Section 4.2.2 for details.

	Single Speed Mode	Double Speed Mode	Quad Speed Mode
MCLK/LRCK Ratio	256x, 512x	128x, 256x	128x

Table 3. Master Clock (MCLK) Ratios

SAMPLE RATE (kHz)	MCLK (MHz)
32	8.192 16.384
44.1	11.2896 22.5792
48	12.288 24.576
64	8.192 16.384
88.2	11.2896 22.5792
96	12.288 24.576
192	12.288 24.576

Table 4. Master Clock (MCLK) Frequencies for Standard Audio Sample Rates

4.3 Serial Audio Interface

The CS5340 supports both I^2S and Left Justified serial audio formats. Upon start-up, the CS5340 will detect the logic level on SDOUT (pin 4). A 10k pull-up to VL is needed to select I^2S format, and a 10k pull-down to GND is needed to select Left Justified format. Please see Figures 13 through 16 on page 12, for more information on the required timing for the two serial audio interface formats.

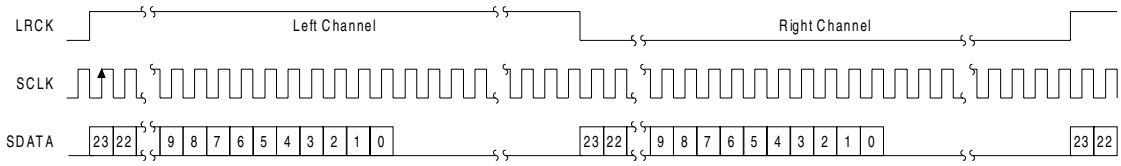


Figure 19. Left-Justified Serial Audio Interface

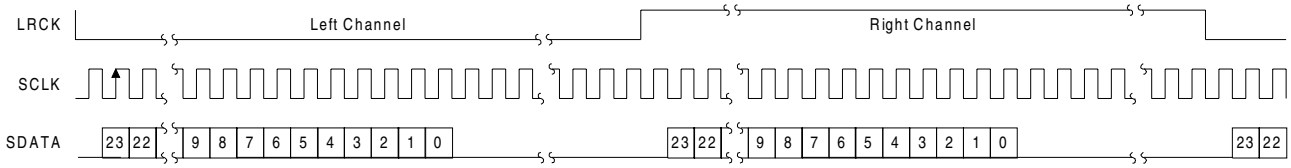


Figure 20. I²S Serial Audio Interface

4.4 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

4.5 Analog Connections

The analog modulator samples the input at 6.144 MHz. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the input sampling frequency (n * 6.144 MHz), where n=0,1,2,... Refer to Figure 21 on page 19 which shows the suggested filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

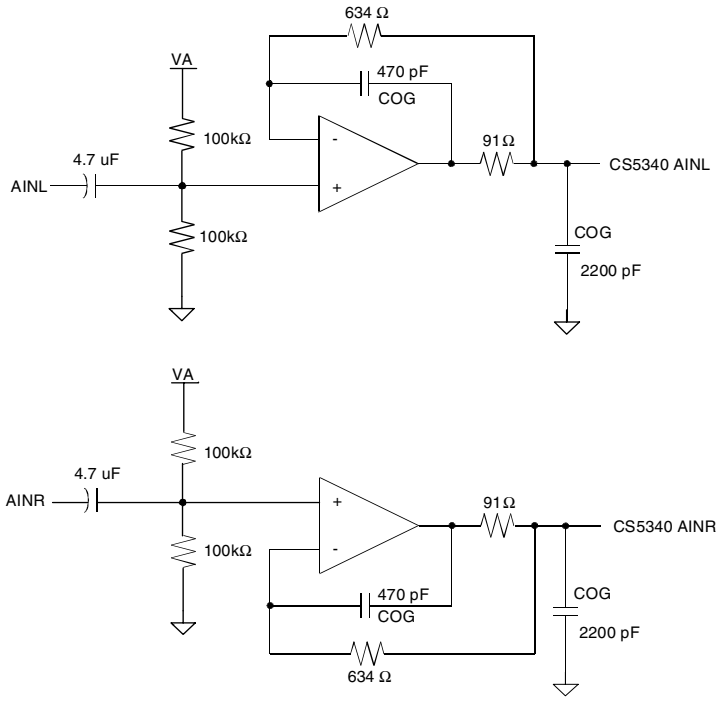


Figure 21. CS5340 Recommended Analog Input Buffer

4.6 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5340 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 17 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REF_GND. The CDB5340 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

4.7 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS5340's in the system. If only one master clock source is needed, one solution is to place one CS5340 in Master mode, and slave all of the other CS5340's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5340 reset with the inactive (falling) edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

5 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

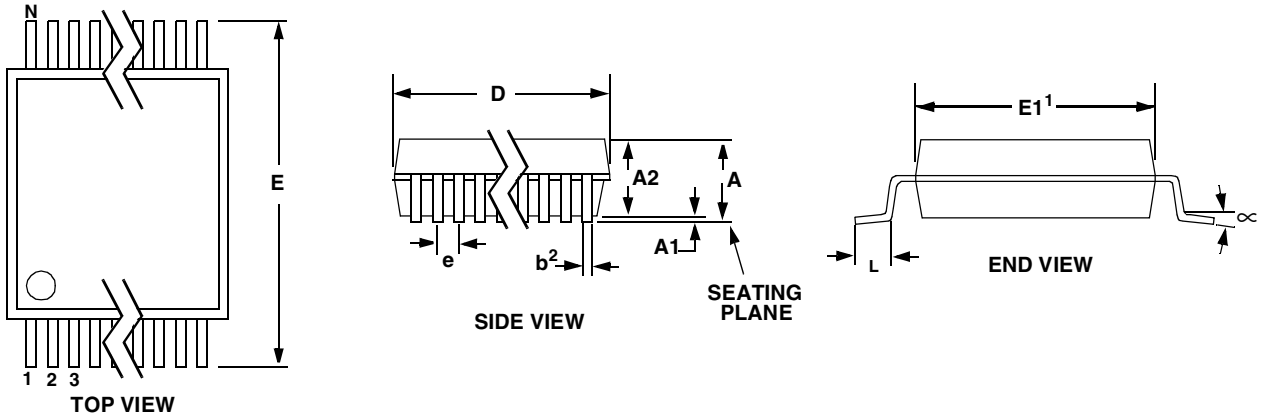
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

6 PACKAGE DIMENSIONS

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.065 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.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