

# DATA SHEET

## **BSS83**

**MOSFET N-channel enhancement  
switching transistor**

Product specification  
File under Discrete Semiconductors, SC07

April 1991

**MOSFET N-channel enhancement switching transistor**

**BSS83**

**DESCRIPTION**

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type. The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

**Marking code:**

BSS83 = M74

**APPLICATIONS**

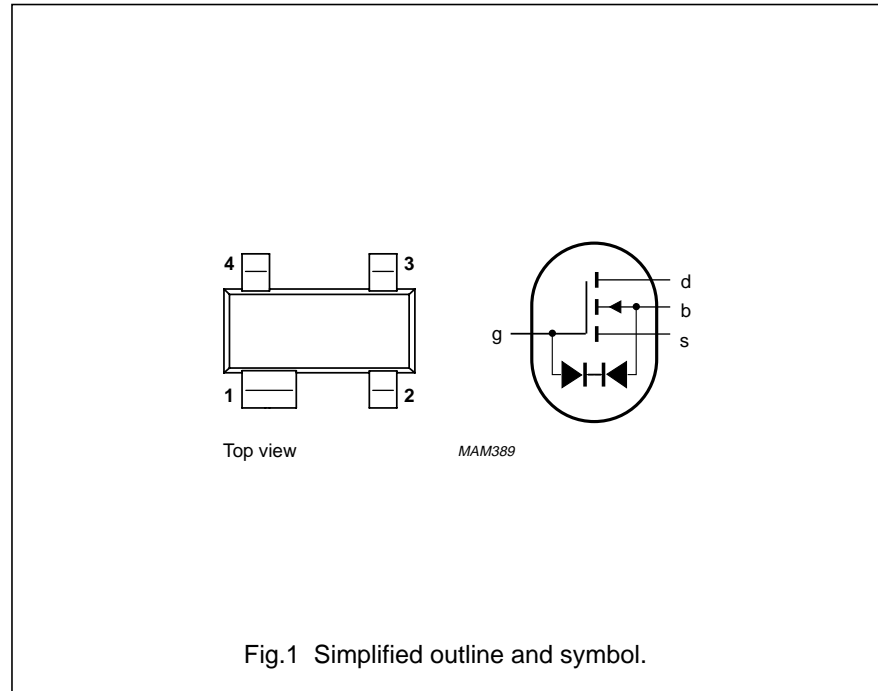
- analog and/or digital switch
- switch driver

**PINNING**

- 1 = substrate (b)
- 2 = source
- 3 = drain
- 4 = gate

**Note**

1. Drain and source are interchangeable.



**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	10 V
Source-drain voltage	$V_{SD}$	max.	10 V
Drain-substrate voltage	$V_{DB}$	max.	15 V
Source-substrate voltage	$V_{SB}$	max.	15 V
Drain current (DC)	$I_D$	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ °C}$	$P_{tot}$	max.	230 mW
Gate-source threshold voltage			
$V_{DS} = V_{GS}; V_{SB} = 0;$			
$I_D = 1\text{ }\mu\text{A}$	$V_{GS(th)}$	>	0.1 V
		<	2.0 V
Drain-source ON-resistance			
$V_{GS} = 10\text{ V}; V_{SB} = 0; I_D = 0.1\text{ mA}$	$R_{DSon}$	<	45 $\Omega$
Feed-back capacitance			
$V_{GS} = V_{BS} = -15\text{ V};$			
$V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	$C_{rss}$	typ.	0.6 pF

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	10 V
Source-drain voltage	$V_{SD}$	max.	10 V
Drain-substrate voltage	$V_{DB}$	max.	15 V
Source-substrate voltage	$V_{SB}$	max.	15 V
Drain current (DC)	$I_D$	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ °C}^{(1)}$	$P_{tot}$	max.	230 mW
Storage temperature range	$T_{stg}$		-65 to + 150 °C
Junction temperature	$T_j$	max.	125 °C

**THERMAL RESISTANCE**

From junction to ambient in free air <sup>(1)</sup>	$R_{th\ j-a}$	=	430 K/W
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**CHARACTERISTICS** $T_{amb} = 25\text{ °C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = V_{BS} = -5\text{ V}; I_D = 10\text{ nA}$

$V_{(BR)DSX} > 10\text{ V}$

Source-drain breakdown voltage

$V_{GD} = V_{BD} = -5\text{ V}; I_D = 10\text{ nA}$

$V_{(BR)SDX} > 10\text{ V}$

Drain-substrate breakdown voltage

$V_{GB} = 0; I_D = 10\text{ nA}; \text{open source}$

$V_{(BR)DBO} > 15\text{ V}$

Source-substrate breakdown voltage

$V_{GB} = 0; I_D = 10\text{ nA}; \text{open drain}$

$V_{(BR)SBO} > 15\text{ V}$

Drain-source leakage current

$V_{GS} = V_{BS} = -2\text{ V}; V_{DS} = 6,6\text{ V}$

$I_{D\text{Soff}} < 10\text{ nA}$

Source-drain leakage current

$V_{GD} = V_{BD} = -2\text{ V}; V_{SD} = 6,6\text{ V}$

$I_{S\text{Doff}} < 10\text{ nA}$

Forward transconductance at  $f = 1\text{ kHz}$ 

$V_{DS} = 10\text{ V}; V_{SB} = 0; I_D = 20\text{ mA}$

$g_{fs} > 10\text{ mS}$   
 $g_{fs} \text{ typ. } 15\text{ mS}$

Gate-source threshold voltage

$V_{DS} = V_{GS}; V_{SB} = 0; I_D = 1\text{ }\mu\text{A}$

$V_{GS(th)} > 0,1\text{ V}$   
 $V_{GS(th)} < 2,0\text{ V}$

Drain-source ON-resistance

$I_D = 0,1\text{ mA};$

$V_{GS} = 5\text{ V}; V_{SB} = 0$

$R_{DSon} < 70\text{ }\Omega$

$V_{GS} = 10\text{ V}; V_{SB} = 0$

$R_{DSon} < 45\text{ }\Omega$

$V_{GS} = 3,2\text{ V}; V_{SB} = 6,8\text{ V (see Fig.4)}$

$R_{DSon} \text{ typ. } 80\text{ }\Omega$

$R_{DSon} < 120\text{ }\Omega$

Gate-substrate zener voltages

$V_{DB} = V_{SB} = 0; -I_G = 10\text{ }\mu\text{A}$

$V_{Z(1)} > 12,5\text{ V}$

$V_{DB} = V_{SB} = 0; +I_G = 10\text{ }\mu\text{A}$

$V_{Z(2)} > 12,5\text{ V}$

Capacitances at  $f = 1\text{ MHz}$ 

$V_{GS} = V_{BS} = -15\text{ V}; V_{DS} = 10\text{ V}$

Feed-back capacitance

$C_{rss} \text{ typ. } 0,6\text{ pF}$

Input capacitance

$C_{iss} \text{ typ. } 1,5\text{ pF}$

Output capacitance

$C_{oss} \text{ typ. } 1,0\text{ pF}$

Switching times (see Fig.2)

$V_{DD} = 10\text{ V}; V_i = 5\text{ V}$

$t_{on} \text{ typ. } 1,0\text{ ns}$

$t_{off} \text{ typ. } 5,0\text{ ns}$

**Note**

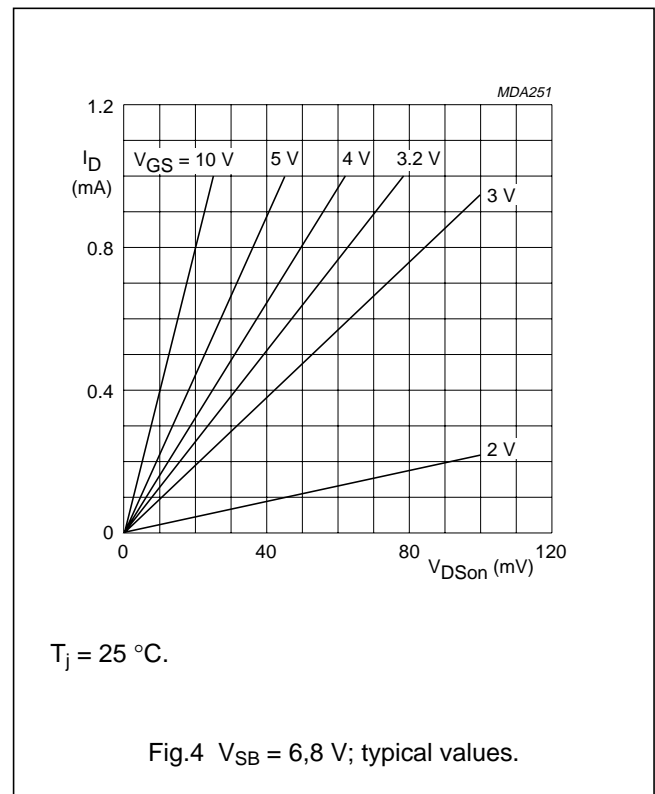
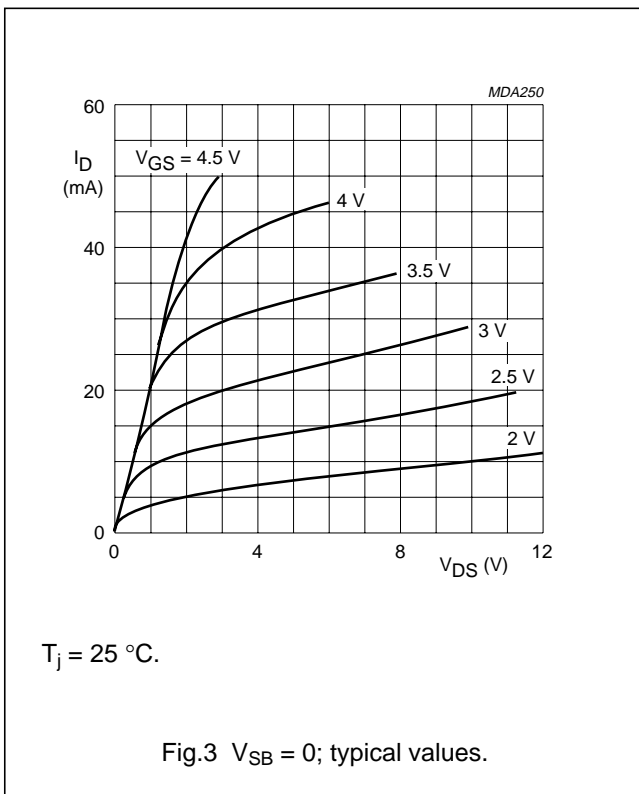
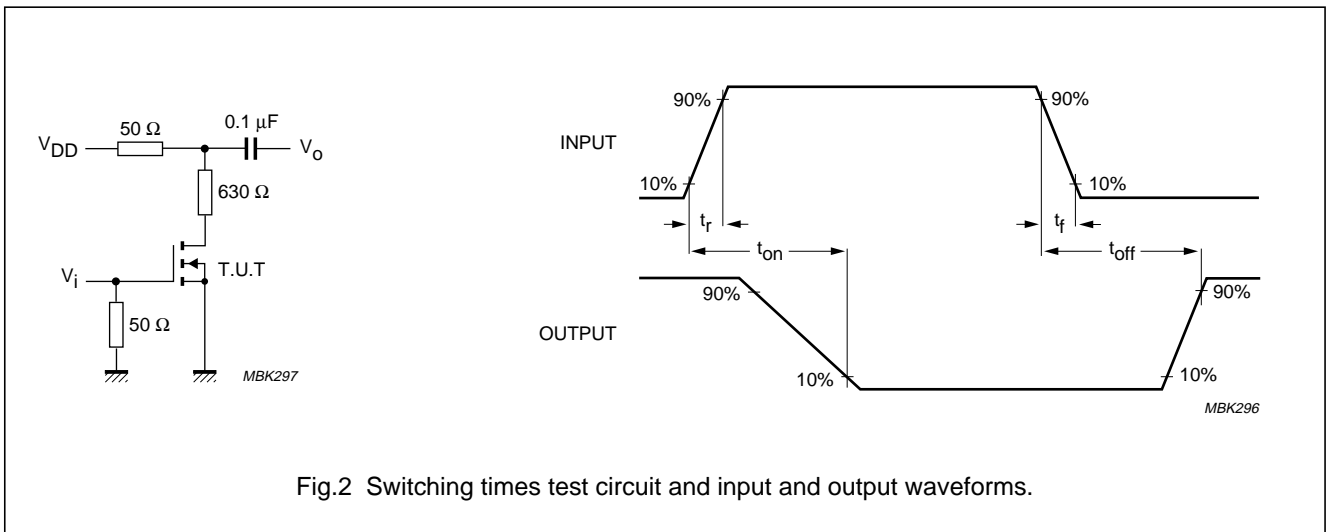
1. Device mounted on a ceramic substrate of  $8\text{ mm} \times 10\text{ mm} \times 0,7\text{ mm}$ .

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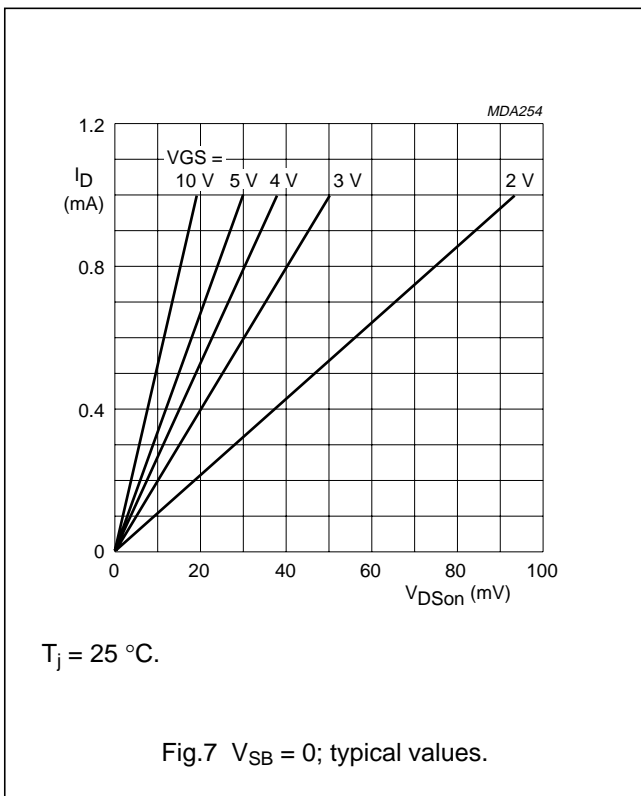
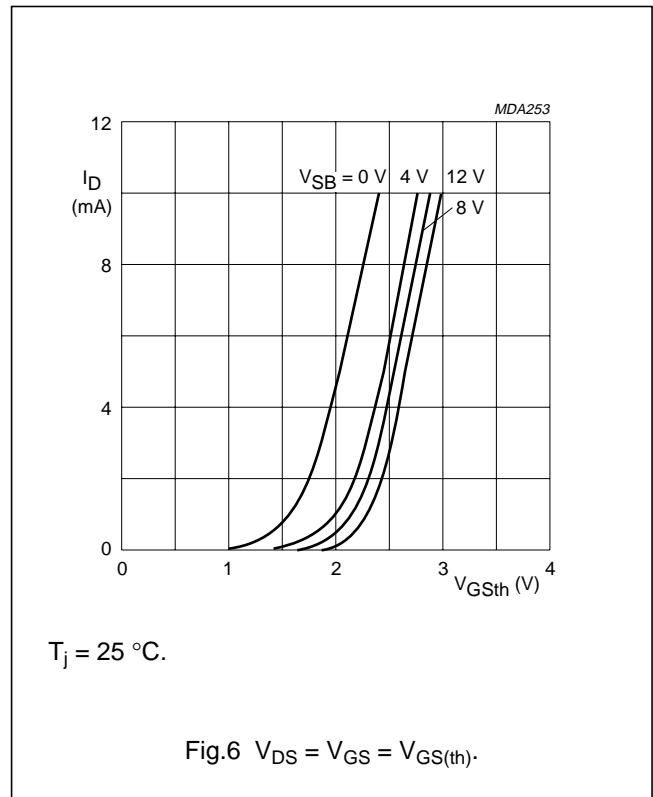
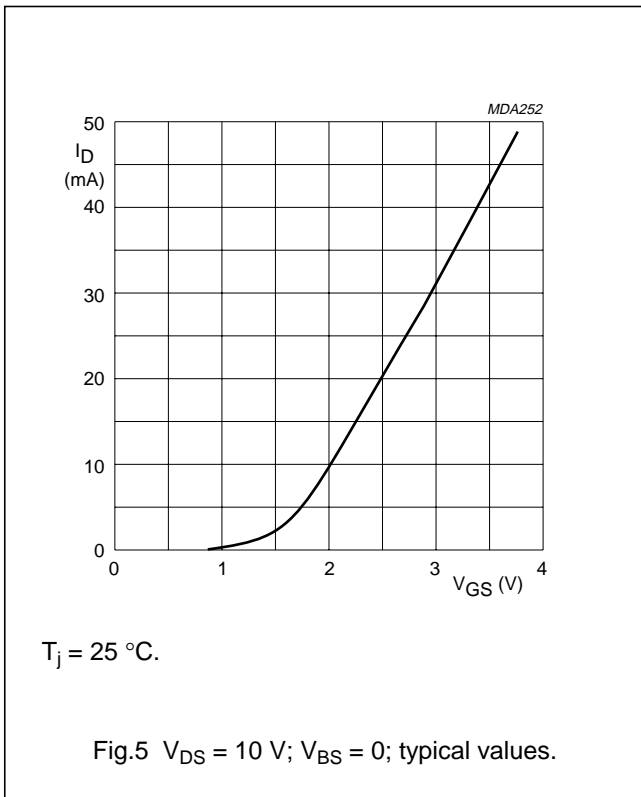
Pulse generator:

- $R_i = 50 \Omega$
- $t_r < 0,5 \text{ ns}$
- $t_f < 1,0 \text{ ns}$
- $t_p = 20 \text{ ns}$
- $\delta < 0,01$



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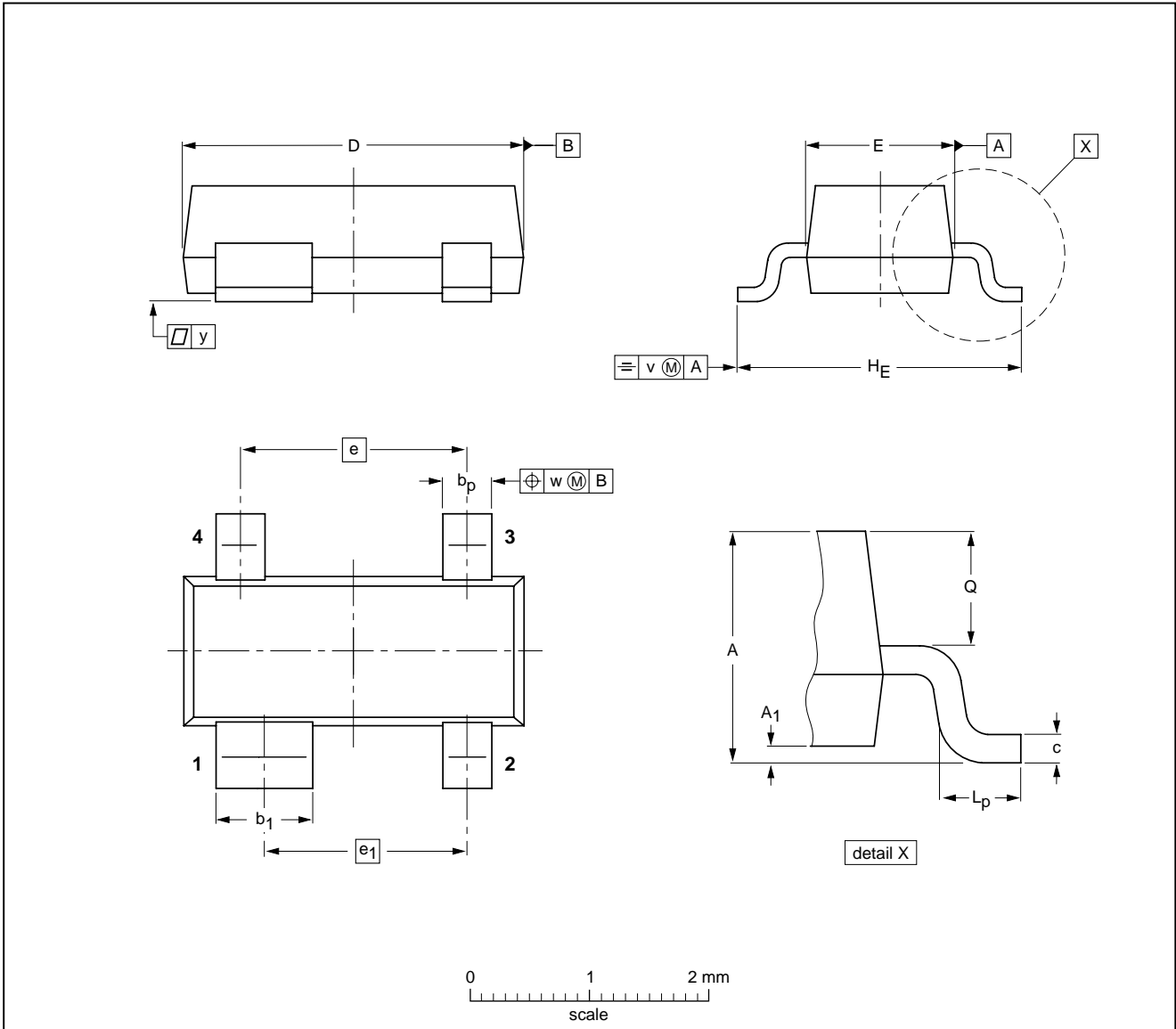
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PACKAGE OUTLINE

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

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