1MSPS, 12- / 10-/ 8-Bit ADCs in 6 Lead SC70

Preliminary Technical Data AD7476A/AD7477A/AD7478A

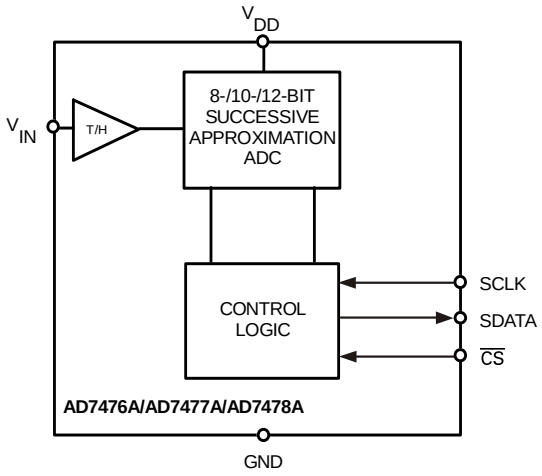
FEATURES

Fast Throughput Rate: 1MSPS
Specified for V_{DD} of 2.35 V to 5.25 V
Low Power:
3 mW typ at 1MSPS with 3V Supplies
12.5mW typ at 1MSPS with 5V Supplies
Wide Input Bandwidth:
70dB SNR at 100kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface
SPI™/QSPI™/MICROWIRE™/DSP Compatible
Standby Mode: 1µA max
6-Lead SC70 Package

APPLICATIONS

Battery-Powered Systems
Personal Digital Assistants
Medical Instruments
Mobile Communications
Instrumentation and Control Systems
Data Acquisition Systems
High-Speed Modems
Optical Sensors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7476A/AD7477A/AD7478A are 12-bit, 10-bit and 8-bit, high speed, low power, successive-approximation ADCs respectively. The parts operate from a single 2.35 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 6MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7476A/AD7477A/AD7478A use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus the analog input range for the part is 0 to V_{DD}. The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. First 8-/10-/12-Bit ADCs in a SC70 package.
2. High Throughput with Low Power Consumption.
3. Flexible Power/Serial Clock Speed Management.

   The conversion rate is determined by the serial clock allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced when a power-down mode is used while not converting. The part also features a Power Down mode to maximize power efficiency at lower throughput rates. Current consumption is 1µA max when in Power Down mode.
4. Reference derived from the power supply.
5. No Pipeline Delay.
   The parts feature a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

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MICROWIRE is a trademark of National Semiconductor Corporation.

REV. PrE (03/02)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD7476A-SPECIFICATIONS[1] (V_{DD}=+2.35 V to +5.25 V, f_{SCLK}=20 MHz, f_{SAMPLE}=1 MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[1,2]	B Grade[1,2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[3]	70	70	dB min	V_{DD}= 2.35V to 3.6V
	69	69	dB min	V_{DD}= 4.75V to 5.25V
Signal-to-Noise Ratio (SNR)[3]	71	71	dB min	V_{DD}= 2.35V to 3.6V
	70	70	dB min	V_{DD}= 4.75V to 5.25V
Total Harmonic Distortion (THD)[3]	-82	-82	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	-84	-84	dB typ	
Intermodulation Distortion (IMD)[3]				
Second Order Terms	–84	-84	dB typ	fa= 100.73 kHz, fb= 90.72 kHz
Third Order Term	–84	-84	dB typ	fa= 100.73 kHz, fb= 90.72 kHz
Aperture Delay	10	10	ns max	
Aperture Jitter	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	TBD	MHz typ	@ 0.1dB
DC ACCURACY				B Grade, See Note 4
Resolution	12	12	Bits	
Integral Nonlinearity[3]		±1	LSB max	
	±0.75		LSB typ	
Differential Nonlinearity		±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits
	±0.9		LSB typ	
Offset Error[3]		±1.5	LSB max	
	±1.5		LSB typ	
Gain Error[3]		±1.5	LSB max	
	±1.5		LSB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	Volts	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	30	30	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
	1.8	1.8	V min	V_{DD}= 2.35V
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD}= 3.6 to 5.25V
	0.4	0.4	V max	V_{DD}= 2.35 to 3.6V
Input Current, I_{IN},SCLK Pin	±1	±1	µA max	Typically 10 nA, V_{IN}= 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	±1	µA typ	
Input Capacitance, C_{IN}[5]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} - 0.2	V_{DD} - 0.2	V min	I_{SOURCE}= 200 µA;V_{DD}= 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK}=200 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[5]	10	10	pF max	
Output Coding	Straight (Natural)		Binary	
CONVERSION RATE				
Conversion Time	800	800	ns max	16 SCLK Cycles
Track/Hold Acquisition Time[3]	400	400	ns max	Full-scale step input
	200	200	ns max	Sine wave input <= 100 KHz
Throughput Rate	1	1	MSPS max	See Serial Interface Section
POWER REQUIREMENTS				
V_{DD}	2.35/5.25	2.35/5.25	V min/max	
I_{DD}				Digital I/Ps= 0V or V_{DD}.
Normal Mode (Static)	2.5	2.5	mA typ	V_{DD}= 4.75V to 5.25V,SCLK On or Off.
	1.25	1.25	mA typ	V_{DD}= 2.35V to 3.6V,SCLK On or Off.
Normal Mode (Operational)	3.5	3.5	mA max	V_{DD}= 4.75V to 5.25V, f_{SAMPLE}=1MSPS
	1.8	1.8	mA max	V_{DD}= 2.35V to 3.6V, f_{SAMPLE}=1MSPS

AD7476A–SPECIFICATIONS[1]

(V_{DD}=+2.35 V to +5.25 V, f_{SCLK}=20 MHz, f_{SAMPLE}=1 MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[1,2]	B Grade[1,2]	Units	Test Conditions/Comments
POWER REQUIREMENTS *(continued)*				
Full Power-Down Mode	1	1	µA max	
Power Dissipation[6]				
Normal Mode (Operational)	17.5	17.5	mW max	V_{DD}= 5V, f_{SAMPLE}= 1MSPS
	5.4	5.4	mW max	V_{DD}= 3V, f_{SAMPLE}= 1MSPS
Full Power-Down	5	5	µW max	V_{DD}= 5 V
	3	3	µW max	V_{DD}= 3 V

NOTES
[1]Temperature ranges from –40°C to +85°C.
[2]Operational from V_{DD}= 2.0V, with input low voltage (V_{INL}) 0.35V max.
[3]See Terminology.
[4]B Grade, maximum specs apply as typical figures when V_{DD} = 4.75V to 5.25V.
[5]Sample tested @ +25°C to ensure compliance.
[6]See Power Versus Throughput Rate section.
Specifications subject to change without notice.

AD7477A–SPECIFICATIONS[1]

(V_{DD}=+2.35 V to +5.25 V, f_{SCLK}=20 MHz, f_{SAMPLE}=1 MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[1,2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[3]	61	dB min	
Total Harmonic Distortion (THD)[3]	-73	dB max	
Peak Harmonic or Spurious Noise (SFDR)[3]	-74	dB max	
Intermodulation Distortion (IMD)[3]			
Second Order Terms	-78	dB typ	fa= 103.5 kHz, fb= 113.5 kHz
Third Order Terms	-78	dB typ	fa= 103.5 kHz, fb= 113.5 kHz
Aperture Delay	10	ns max	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	6.5	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits.
Offset Error	±1	LSB max	
Gain Error	±1	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	Volts	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	V_{DD}= 5V
	0.4	V max	V_{DD}= 3V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN}= 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[4]	10	pF max	

AD7477A-SPECIFICATIONS[1] (V_{DD}=+2.35 V to +5.25 V, f_{SCLK}=20 MHz, f_{SAMPLE}=1 MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[1,2]	Units	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} - 0.2	V min	I_{SOURCE}= 200 µA,V_{DD}= 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK}= 200µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[4]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	700	ns max	14 SCLK cycles with SCLK at 20 MHz
Track/Hold Acquisition Time[3]	TBD	ns max	
Throughput Rate	1	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.35/5.25	V min/max	
I_{DD}			Digital I/Ps = 0V or V_{DD}
Normal Mode(Static)	2	mA typ	V_{DD}= 4.75V to 5.25V, SCLK On or Off.
	1	mA typ	V_{DD}= 2.35V to 3.6V, SCLK On or Off.
Normal Mode (Operational)	3.5	mA max	V_{DD}= 4.75V to 5.25V, f_{SAMPLE} = 1MSPS
	1.6	mA max	V_{DD}= 2.35V to 3.6V, f_{SAMPLE} = 1MSPS
Full Power-Down Mode	1	µA max	
Power Dissipation[5]			
Normal Mode (Operational)	17.5	mW max	V_{DD}= 5V, f_{SAMPLE} = 1MSPS
	4.8	mW max	V_{DD}= 3V, f_{SAMPLE} = 1MSPS
Full Power-Down	5	µW max	V_{DD}= 5 V

NOTES
[1]Temperature ranges from –40°C to +85°C.
[2]Operational from V_{DD}= 2.0V, with input high voltage (V_{INH})1.8 V min.
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
[5]See Power Versus Throughput Rate section.
Specifications subject to change without notice.

AD7478A-SPECIFICATIONS[1] (V_{DD}= +2.35 V to +5.25 V, f_{SCLK}= 20MHz, f_{SAMPLE}=1 MSPS unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[1,2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN}= 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[3]	49	dB min	
Total Harmonic Distortion (THD)[3]	-65	dB max	
Peak Harmonic or Spurious Noise (SFDR)[3]	-65	dB max	
Intermodulation Distortion (IMD)[3]			
Second Order Terms	-68	dB typ	fa= 498.7kHz, fb= 508.7kHz
Third Order Terms	-68	dB typ	fa= 498.7kHz, fb= 508.7kHz
Aperture Delay	10	ns max	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	6.5	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1dB
DC ACCURACY			
Resolution	8	Bits	
Integral Nonlinearity[3]	±0.5	LSB max	
Differential Nonlinearity[3]	±0.5	LSB max	Guaranteed No Missed Codes to 8 Bits.
Offset Error[3]	±0.5	LSB max	
Gain Error[3]	±0.5	LSB max	
Total Unadjusted Error (TUE)[3]	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	Volts	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	

AD7478A–SPECIFICATIONS[1]

(V_{DD}=+2.35 V to +5.25 V, f_{SCLK}=20 MHz, f_{SAMPLE}=1 MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[1,2]	Units	Test Conditions/Comments
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	V_{DD}= 5V
	0.4	V max	V_{DD}= 3V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN}= 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} - 0.2	V min	I_{SOURCE}= 200 µA,V_{DD}= 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK}= 200µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[4]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	600	ns max	12 SCLK Cycles with SCLK at 20 MHz
Track/Hold Acquisition Time[3]	TBD	ns max	
Throughput Rate	1	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.35/5.25	Vmin/max	
I_{DD}			Digital I/Ps= 0V or V_{DD}.
Normal Mode(Static)	2	mA typ	V_{DD}= 4.75V to 5.25V, SCLK On or Off.
	1	mA typ	V_{DD}= 2.35V to 3.6V, SCLK On or Off.
Normal Mode (Operational)	3.5	mA max	V_{DD}= 4.75V to 5.25V
	1.6	mA max	V_{DD}= 2.35V to 3.6V
Full Power-Down Mode	1	µA max	
Power Dissipation[5]			
Normal Mode (Operational)	17.5	mW max	V_{DD}= 5V
	4.8	mW max	V_{DD}= 3V
Full Power-Down	5	µW max	V_{DD}= 5 V

NOTES

[1]Temperature ranges from –40°C to +85°C.

[2]Operational from V_{DD}= 2.0V, with input high voltage (V_{INH})1.8 V min.

[3]See Terminology.

[4]Sample tested @ +25°C to ensure compliance.

[5]See Power Versus Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD}= +2.35 V to +5.25 V; T_A= T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7476A/AD7477A/AD7478A	Units	Description
f_{SCLK} [2]	10	KHz min	
	20	KMHz max	
$t_{CONVERT}$	16 x t_{SCLK}		AD7476A
	14 x t_{SCLK}		AD7477A
	12 x t_{SCLK}		AD7478A
t_{QUIET}	50	ns min	Minimum Quiet Time required between Bus Relinquish and start of Next Conversion
t_1	10	ns min	Minimum $\overline{CS}$ Pulse Width
t_2	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3 [3]	20	ns max	Delay from $\overline{CS}$ Until SDATA Three-State Disabled
t_4 [3]	20	ns max	Data Access Time After SCLK Falling Edge.
t_5	0.4t_{SCLK}	ns min	SCLK Low Pulse Width
t_6	0.4t_{SCLK}	ns min	SCLK High Pulse Width
t_7	10	ns min	SCLK to Data Valid Hold Time
t_8 [4]	10	ns min	SCLK Falling Edge to SDATA High Impedance
	25	ns max	SCLK Falling Edge to SDATA High Impedance
$t_{power-up}$ [5]	1	µs typ	Power Up Time from Full Power-down.

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr=tf=5ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.
[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.
[3]Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4]t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[5]See Power-up Time section.

Specifications subject to change without notice.

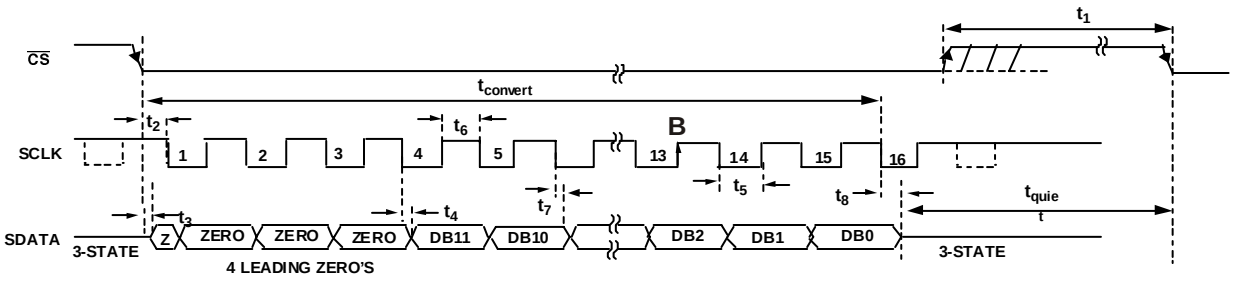


Figure 1. AD7476A Serial Interface Timing Diagram

Timing Example 1

Having f_{SCLK} = 20 MHz and a throughput of 1 MSPS, gives a cycle time of t_2 + 12.5(1/f_{SCLK}) + t_{ACQ} = 1 µs. With t_2 = 10 ns min, this leaves t_{ACQ} to be 365 ns. This 365 ns satisfies the requirement of 200 ns for t_{ACQ}. From Figure 2, t_{ACQ} comprises of 2.5(1/f_{SCLK}) + t_8 + t_{QUIET}, where t_8 = 25 ns max. This allows a value of 215 ns for t_{QUIET} satisfying the minimum requirement of 50 ns.

Timing Example 2

Having f_{SCLK} = 5 MHz and a throughput of 315 KSPS, gives a cycle time of t_2 + 12.5(1/f_{SCLK}) + t_{ACQ} = 3.174 µs. With t_2 = 10 ns min, this leaves t_{ACQ} to be 664 ns. This 664 ns satisfies the requirement of 200 ns for t_{ACQ}. From Figure 2, t_{ACQ} comprises of 2.5(1/f_{SCLK}) + t_8 + t_{QUIET}, t_8 = 25 ns max. This allows a values of 139 ns for t_{QUIET} satisfying the minimum requirement of 50 ns. As in this example and with other slower clock values, the signal may already be acquired before the conversion is complete, but it is still necessary to leave 50 ns minimum t_{QUIET} between conversions. In Example 2 the signal should be fully acquired at approximately point C in Figure 2.

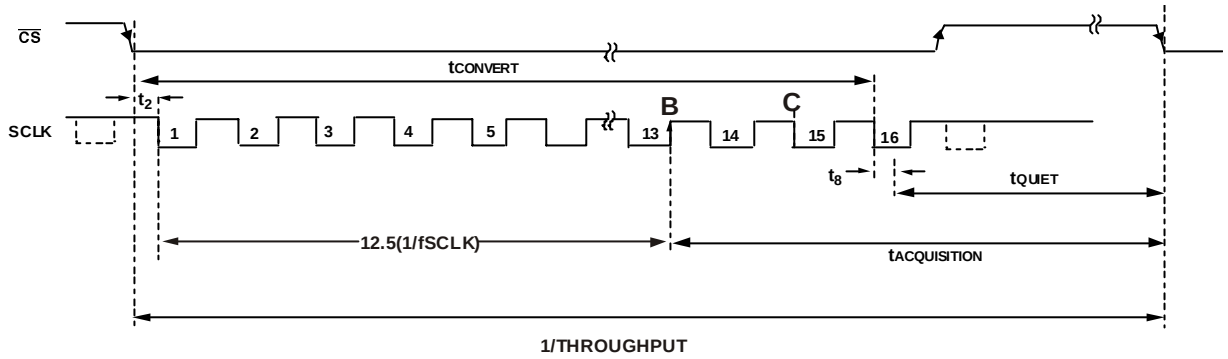


Figure 2. Serial Interface Timing Example

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

V_{DD} to GND.....-0.3 V to 7 V
Analog Input Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND.....–0.3 V to 7 V
Digital Output Voltage to GND....–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2].....±10 mA
Operating Temperature Range
  Commercial (A, B Grade).....–40°C to +85°C
  Storage Temperature Range.....–65°C to +150°C
Junction Temperature.....150°C
SC70 Package
  θ_{JA} Thermal Impedance.....332°C/W
  θ_{JC} Thermal Impedance.....120°C/W
Lead Temperature, Soldering
  Vapor Phase (60 secs)..... +215°C
  Infrared (15 secs)..... +220°C
ESD..... 4 KV

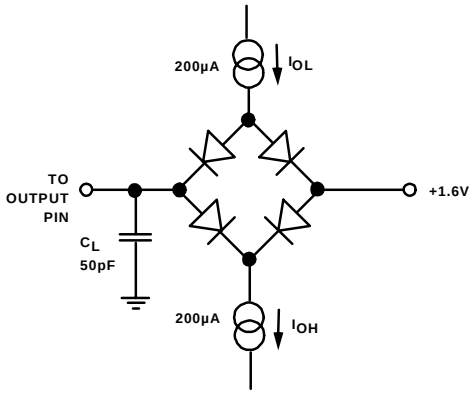
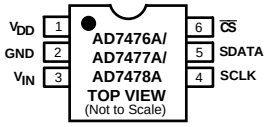


Figure 3. Load Circuit for Digital Output Timing Specifications

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

PIN CONFIGURATION
AD7476A/AD7477A/AD7478A



6 Lead SC70

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476A/AD7477A/AD7478A and also frames the serial data transfer.
V_{DD}	Power Supply Input. The V_{DD} range for the AD7476A/AD7477A/AD7478A is from +2.35V to +5.25V.
GND	Analog Ground. Ground reference point for all circuitry on the AD7476A/AD7477A/ AD7478A. All analog input signals should be referred to this GND voltage.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{DD}.
SDATA	Data Out. Logic Output. The conversion result from the AD7476A/AD7477A/AD7478A is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7476A consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first. The data stream from the AD7477A consists of four leading zeros followed by the 10 bits of conversion data. The data stream from the AD7478A consists of four leading zeros followed by the 8 bits of conversion data.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476A/AD7477A/AD7478A's conversion process.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option[2]	Branding
AD7476AAKS	-40°C to +85°C	±0.75 typ	KS-6	CEZ
AD7476ABKS	-40°C to +85°C	±1 max	KS-6	CEY
AD7477AAKS	-40°C to +85°C	±1 max	KS-6	CFZ
AD7478AAKS	-40°C to +85°C	±0.5 max	KS-6	CJZ
EVAL-AD7476ACB[3]				
EVAL-AD7477ACB[3]				
EVAL-CONTROL BRD2[4]				

NOTES
[1]Linearity Error here refers to Integral Nonlinearity.
[2]KS = SC70.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demostration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7476A and AD7477A, the endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition. For the AD7478A, the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e, AGND + 0.5LSB. For the AD7478A, this is the desviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e, AGND + 1LSB.

Gain Error

For the AD7476A and AD7477A, this is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal, i.e, V_{REF} – 1.5LSB after the offset error has been adjusted out. For the AD7478A, this is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal, i.e, V_{REF} – 1LSB after the offset error has been adjusted out.

Track/Hold Acquisition Time

The track/hold amplifier returns into track mode at the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See serial interface timing section for more details.

Signal-to- (Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\,N + 1.76)\,dB$$

Thus, for a 12-bit converter this is 74 dB, for a 10-bit converter this is 62dB and for an 8-bit converter it is 50dB.

Total Unadjusted Error

This is a comprehensive specification which includes gain error, linearity error and offset error.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. It is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7476A/AD7477A/AD7478A are tested using the CCIF standard where two input frequencies are used (see fa and fb in the specification page). In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PERFORMANCE CURVES

Figure 4 shows a typical FFT plot for the AD7476A at 1MHz sample rate and 100kHz input frequency.

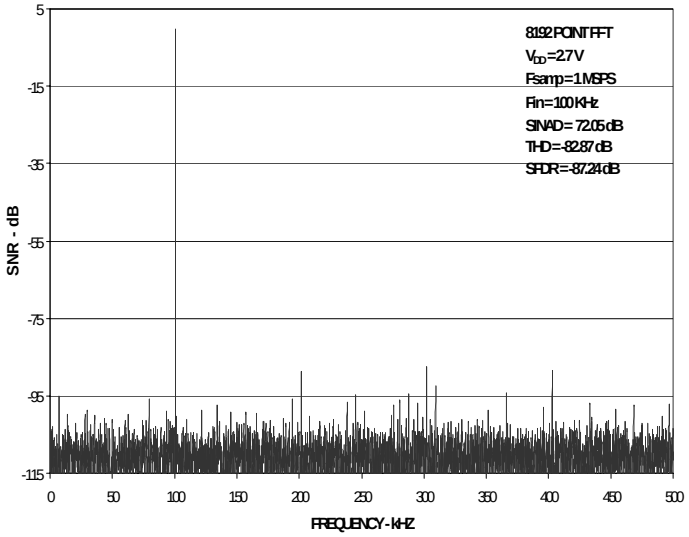


Figure 4. AD7476A Dynamic Performance at 1MSPS

Figure 5 shows a typical FFT plot for the AD7477A at 1MHz sample rate and 100kHz input frequency.

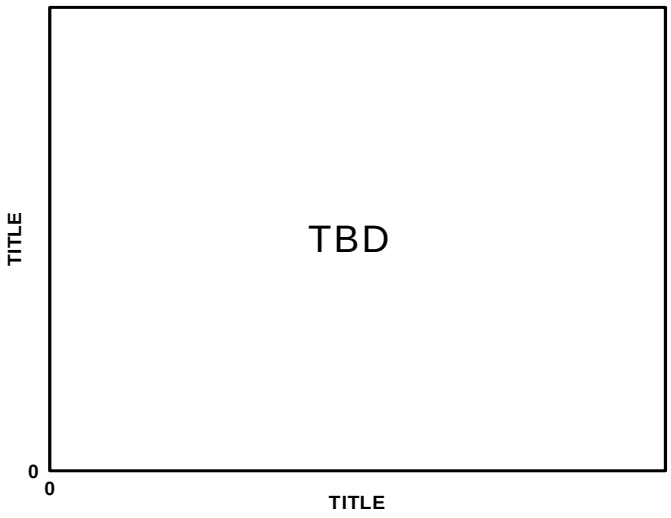


Figure 5. AD7477A Dynamic Performance at 1MSPS

Figure 6 shows a typical FFT plot for the AD7478A at 1MHz sample rate and 100kHz input frequency.

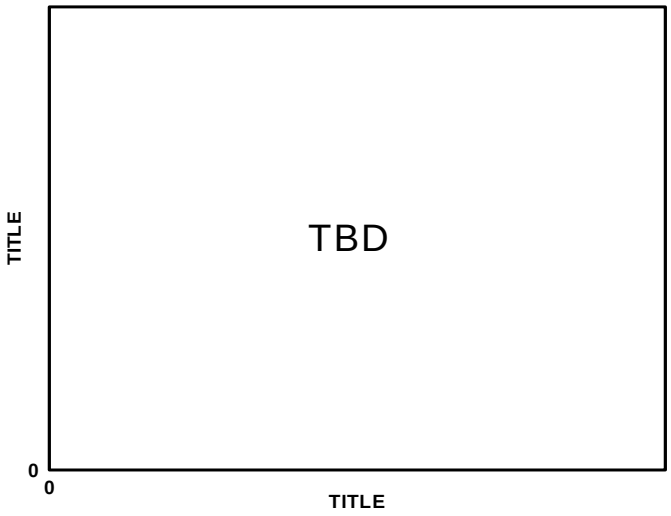


Figure 6. AD7478A Dynamic Performance at 1MSPS

Figure 7 shows the signal to (noise+distortion) ratio performance versus input frequency for various supply voltages while sampling at 1 MSPS with a SCLK frequency of 20MHz for the AD7476A.

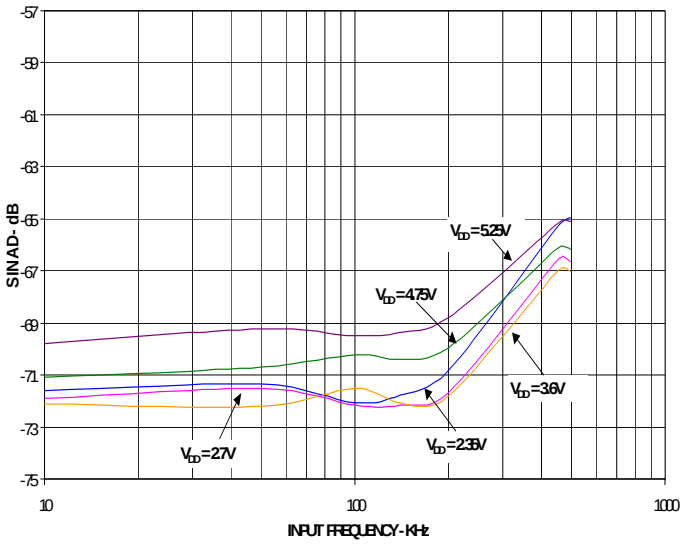


Figure 7. AD7476A SINAD vs Input Frequency at 1 MSPS

Figure 8 shows the INL performance for the AD7476A.

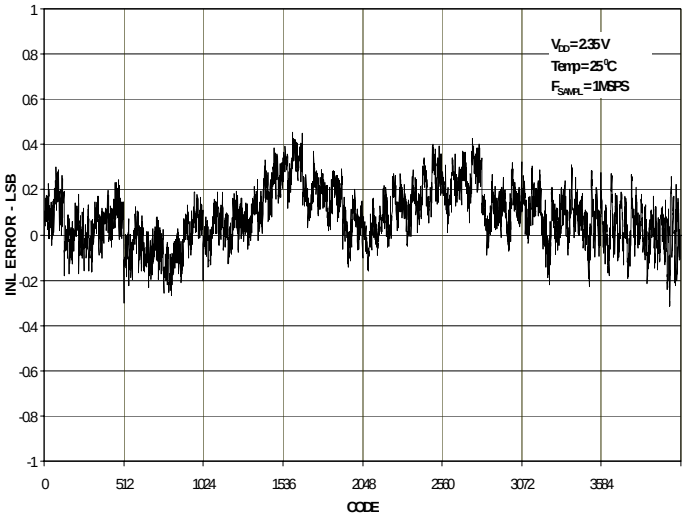


Figure 8. AD7476A INL performance.

Figure 9 shows the DNL performance for the AD7476A.

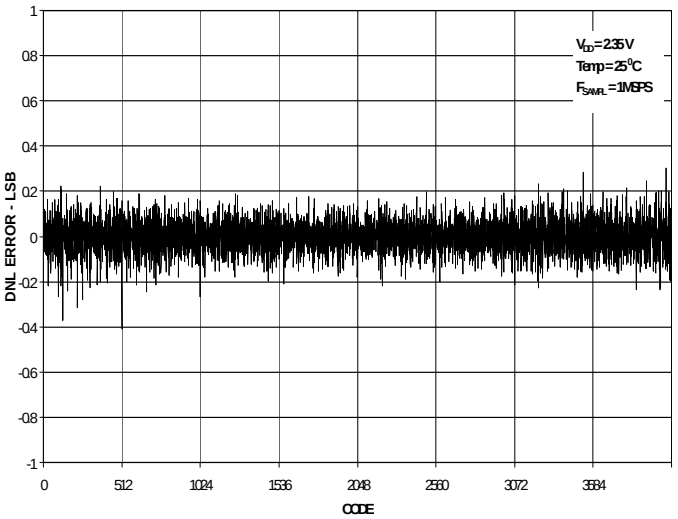


Figure 9. AD7476A DNL performance.

CIRCUIT INFORMATION

The AD7476A/AD7477A/AD7478A are fast, micro-power, 12-/10-/8-Bit, single supply, A/D converters respectively. The parts can be operated from a +2.35V to +5.25V supply. When operated from either a 5 V supply or a 3 V supply, the AD7476A/AD7477A/AD7478A are capable of throughput rates of 1MSPS when provided with a 20MHz clock.

The AD7476A/AD7477A/AD7478A provide the user with an on-chip track/hold, A/D converter, and a serial interface housed in a tiny 6-lead SC70 package, which offers the user considerable space saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 to V_{DD} . An external reference is not required for the ADC and neither is there a reference on-chip. The reference for the AD7476A/AD7477A/AD7478A is derived from the power supply and thus gives the widest dynamic input range.

The AD7476A/AD7477A/AD7478A also feature a power-down option to allow power saving between conversions. The power-down feature is implemented across the standard serial interface as described in the "Modes of Operation" section.

CONVERTER OPERATION

The AD7476A/AD7477A/AD7478A is a successive-approximation analog-to-digital converter based around a charge redistribution DAC. Figures 10 and 11 show simplified schematics of the ADC. Figure 10 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

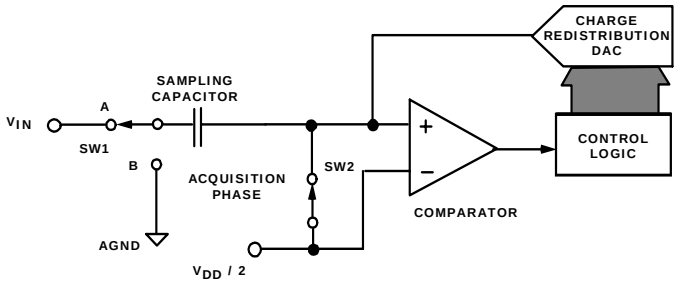


Figure 10. ADC Acquisition Phase

When the ADC starts a conversion, see Figure 11, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 12 and 13 show the ADC transfer function.

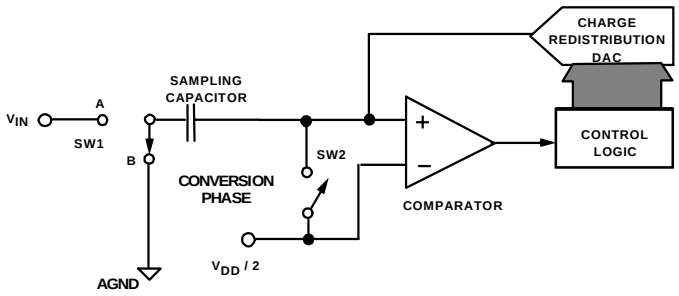


Figure 11. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7476A/AD7477A/AD7478A is straight binary. For the AD7476A/AD7477A, the designed code transitions occur midway between successive integer LSB values, i.e, 0.5LSB, 1.5LSBs, etc. The LSB size is V_{DD}/4096 for the AD7476A and V_{DD}/1024 for the AD7477A . The ideal transfer characteristic for the AD7476A/AD7477A is shown in Figure 12.

For the AD7478A, the designed code transitions occur at the succesive integer LSB values, i.e, 1LSB, 2LSBs, etc. The LSB size is in this case V_{DD}/256. The ideal transfer characteristic for the AD7478A is shown in Figure 13.

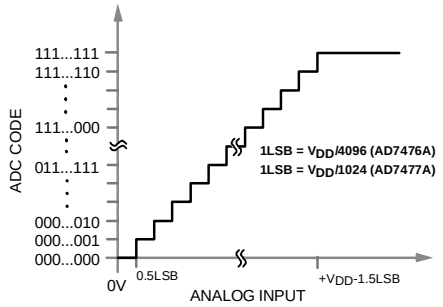


Figure 12. AD7476A/AD7477A Transfer Characteristic

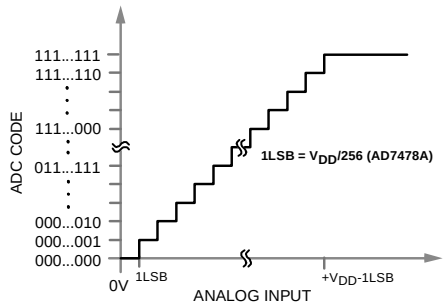


Figure 13. AD7478A Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 14 shows a typical connection diagram for the AD7476A/AD7477A/AD7478A. V_{REF} is taken internally from V_{DD} and as such V_{DD} should be well decoupled. This provides an analog input range of 0V to V_{DD}. For the AD7476A the conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result. Likewise, for the AD7477A and AD7478A the conversion result consists of four leading zeros followed by the MSB of the 10-bit result and 8-bit result respectively.

Alternatively, because the supply current required by the AD7476A/AD7477A/AD7478A is so low, a presision reference can be used as the supply source to the AD7476A/AD7477A/AD7478A. A REF19x voltage reference (REF195 for 5V or REF193 for 3V) can be used to supply the required voltage to the ADC - see Figure 14. This configuration is especially useful if your power supply is quite noisy or if the system supply voltages are at some value other than 5V or 3V (e.g. 15V). The REF19x will output a steady voltage to the AD7476A/AD7477A/AD7478A. If the low dropout REF193 is used, the current it needs to supply to the AD7476A/AD7477A/AD7478A is typically 1mA. When the ADC is converting at a rate of 1MSPS the REF193 will need to supply a maximum of 1.6mA to the AD7476A/AD7477A/AD7478A. The load regulation of the REF193 is typically 10 ppm/mA (REF193, V_S= 5V), which results in an error of 16ppm (48µV) for the 1.6mA drawn from it. This corresponds to a 0.065 LSB error for the AD7476A with V_{DD}= 3V from the REF193, a 0.016 LSB error for the AD7477A, and a 0.0041 LSB error for the AD7478A. For applications where power consumption is of concern, the power-down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See Modes of Operation section.

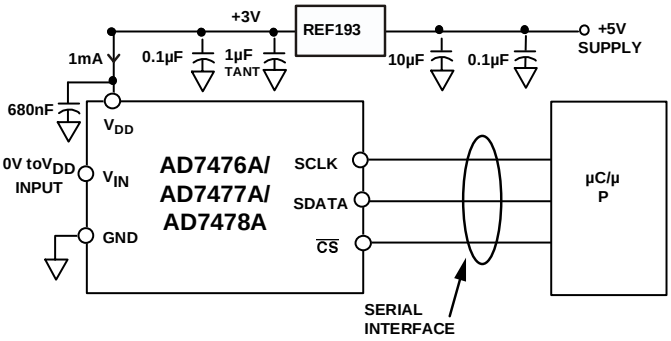


Figure 14. REF193 as Power Supply to AD7476A/ AD7477A/AD7478A

Table I provides some typical performance data with various references used as a V_{DD} source with a low frequency analog input. Under the same set-up conditions the references were compared and the TBD proved the optimum reference.

Table I

Reference Tied To V_{DD}	AD7476A SNR Performance 1kHz Input
AD780@3V	TBD dB
REF193	TBD dB
AD780@2.5V	TBD dB
REF192	TBD dB
AD1582	TBD dB

Analog Input

Figure 15 shows an equivalent circuit of the analog input structure of the AD7476A/AD7477A/AD7478A. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 20mA is the maximum current these diodes can conduct without causing irreversable damage to the part. The capacitor C1 in Figure 15 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 30 pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of a bandpass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

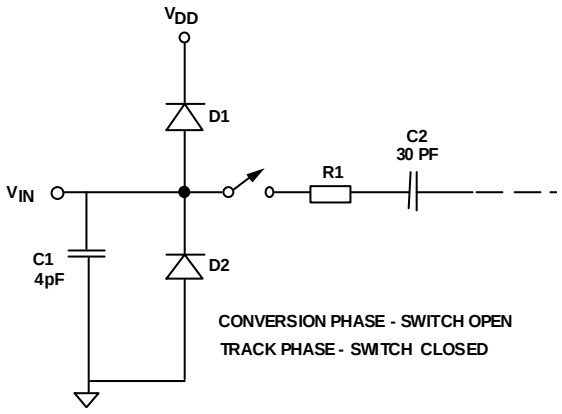


Figure 15. Equivalent Analog Input Circuit

Table II provides some typical performance data with various op amps used as the input buffer with a low frequency analog input. Under the same set-up conditions the op amps were compared and the TBD proved the optimum op amp.

Table II

Op amp in the input buffer	AD7476A SNR Performance 1kHz Input
AD711	TBD dB
AD797	TBD dB
AD845	TBD dB

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 16 shows a graph of the Total Harmonic Distortion versus Analog input frequency for different source impedances when using a supply voltage of 2.7V and sampling at a rate of 1 MSPS. Figure 17 shows a graph of the Total Harmonic Distortion versus Analog Input Signal Frequency for various supply voltages while sampling at 1 MSPS with a SCLK frequency of 20 MHz.

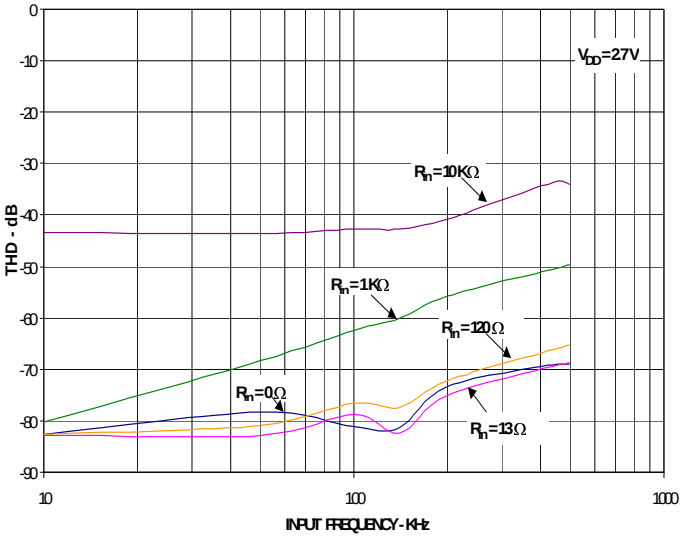


Figure 16. THD vs. Analog Input Frequency for various Source Impedance

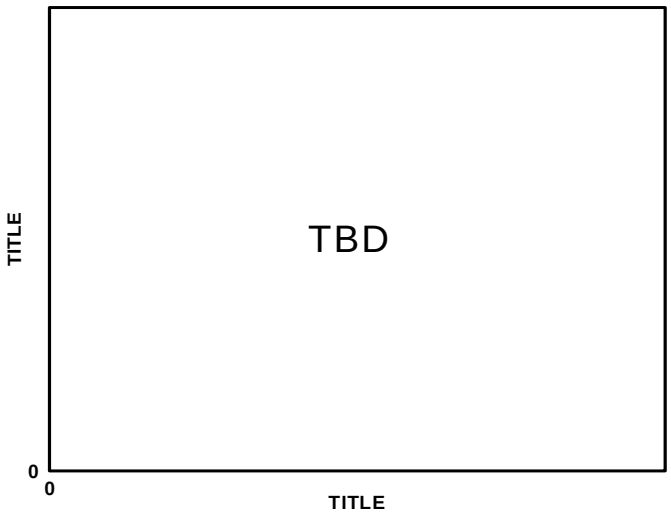


Figure 17. THD vs. Analog Input Frequency, Fs = 1 MSPS

Digital Inputs

The digital inputs applied to the AD7476A/AD7477A/AD7478A are not limited by the maximum ratings which limit the analog inputs. Instead, the digitals inputs applied can go to 7V and are not restricted by the V_{DD} + 0.3V limit as on the analog inputs. For example, if the AD7476A/AD7477A/AD7478A were operated with a V_{DD} of 3V then 5V logic levels could be used on the digital inputs. However it is important to note that the data output on SDATA will still have 3V logic levels when V_{DD}= 3V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3V was applied prior to V_{DD}.

MODES OF OPERATION

The mode of operation of the AD7476A/AD7477A/AD7478A is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, Normal Mode and Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether the AD7476A/AD7477A/AD7478A will enter Power-Down Mode or not. Similarly, if already in Power-Down then $\overline{CS}$ can control whether the device will return to Normal operation or remain in Power-Down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7476A/AD7477A/AD7478A remaining fully-powered all the time. Figure 18 shows the general diagram of the operation of the AD7476A/AD7477A/AD7478A in this mode.

The conversion is iniated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the end of the $t_{CONVERT}$ the part will remain powered up but the conversion will be terminated and SDATA will go back into three-state.

For the AD7476A sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. For the AD7477A and AD7478A fourteen and twelve serial clock cycles are required to complete the conversion and access the complete conversion result, respectively.

$\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7476A/AD7477A/AD7478A is in power down, all analog circuitry is powered down.

To enter Power-Down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK as shown in Figure 19. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will enter Power-Down and the conversion that was intiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, then the part will remain in Normal Mode and will not Power-Down. This will avoid accidental Power-Down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7476A/AD7477A/AD7478A up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up once 16 SCLKs have elapsed and valid data will result from the next conversion as shown in Figure 20. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, then the AD7476A/AD7477A/AD7478A will go back into Power-Down again. This avoids accidental power up due to glitches on the $\overline{CS}$ line or an inadvertent burst of 8 SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

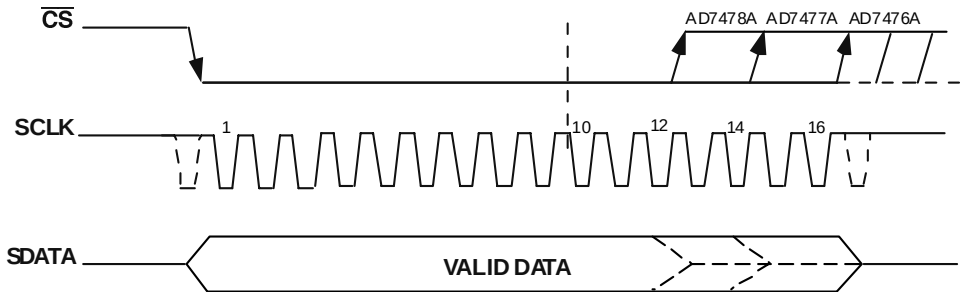


Figure 18. Normal Mode Operation

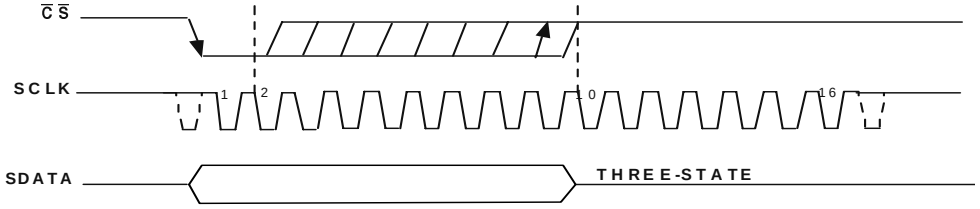


Figure 19. Entering Power Down Mode

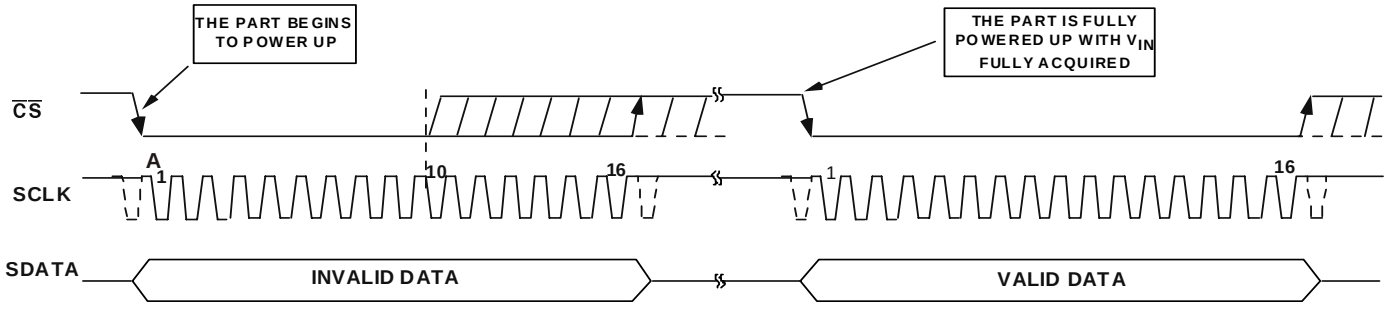


Figure 20. Exiting Power Down Mode

Power-up Time

The power-up time of the AD7476A/AD7477A/AD7478A is typically 1µs, which means that with any frequency of SCLK up to 20MHz, one dummy cycle will always be sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. The quite time t_{QUIET} must still be allowed from the point where the bus goes back into three-state after the dummy conversion, to the next falling edge of $\overline{CS}$. When running at 1MSPS throughput rate, the AD7476A/AD7477A/AD7478A will power up and acquire a signal within +/- 0.5 LSB in one dummy cycle, i.e. 1µs.

When powering up from the Power-Down mode with a dummy cycle, as in Figure 18, the track and hold which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as point A in Figure 20. Although at any SCLK frequency one dummy cycle is sufficient to power the device up and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; 1µs will be sufficient to power the device up and acquire the input signal. If, for example, a 5MHz SCLK frequency was applied to the ADC, the cycle time would be 3.2µs. In one dummy cycle, 3.2µs, the part would be powered up and V_{IN} acquired fully. However after 1 µs with a 5MHz SCLK only 5 SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case the $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time t_{QUIET} to initiate the conversion.

When power supplies are first applied to the AD7476A/AD7477A/AD7478A, the ADC may either power up in the Power-Down mode or in Normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the Power-Down mode while not in use and the user wishes the part to power up in Power-Down mode, then the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as that shown in Figure 19. Once supplies are applied to the AD7476A/AD7477A/AD7478A, the power up time is the same as that when powering up from the Power-Down mode. It takes approximately 1µs to power up fully if the part powers up in Normal mode. It is not necessary to wait 1 µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed. As mentioned earlier, when powering up from the Power-Down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However when the ADC powers up initially after supplies are applied, the track and hold will already be in track. This means, assuming one has the facility to monitor the ADC supply current, if the ADC powers up in the desired mode of operation and thus a dummy cycle is not required to change mode, then neither is a dummy cycle required to place the track and hold into track.

POWER VERSUS THROUGHPUT RATE

By using the Power-Down mode on the AD7476A/AD7477A/AD7478A when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 21 shows how as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

For example, if the AD7476A/AD7477A/AD7478A is operated in a continuous sampling mode with a throughput rate of 100 kSPS and a SCLK of 20MHz (V_{DD}= 5V), and the device is placed in the Power-Down mode between conversions, then the power consumption is calculated as follows. The power dissipation during normal operation is 17.5 mW (V_{DD}= 5V). If the power up time is one dummy cycle, i.e. 1µs, and the remaining conversion time is another cycle, i.e. 1µs, then the AD7476A/AD7477A/AD7478A can be said to dissipate 17.5mW for 2µs during each conversion cycle.If the throughput rate is 100 kSPS, the cycle time is 10µs and the average power dissipated during each cycle is (2/10) x (17.5 mW)= 3.5 mW. If V_{DD}= 3V, SCLK= 20MHz and the device is again in Power-Down mode between conversions, then the power dissipation during normal operation is 5.4 mW. The AD7476A/AD7477A/AD7478A can now be said to dissipate 5.4 mW for 2µs during each conversion cycle. With a throughput rate of 100 kSPS, the average power dissipated during each cycle is (2/10) x (5.4 mW)= 1.08 mW. Figure 21 shows the Power vs. Throughput Rate when using the Power-Down mode between conversions with both 5V and 3V supplies.

The Power-Down mode is intended for use with throughput rates of approximately 333 kSPS and under as at higher sampling rates there is no power saving made by using the power-down mode.

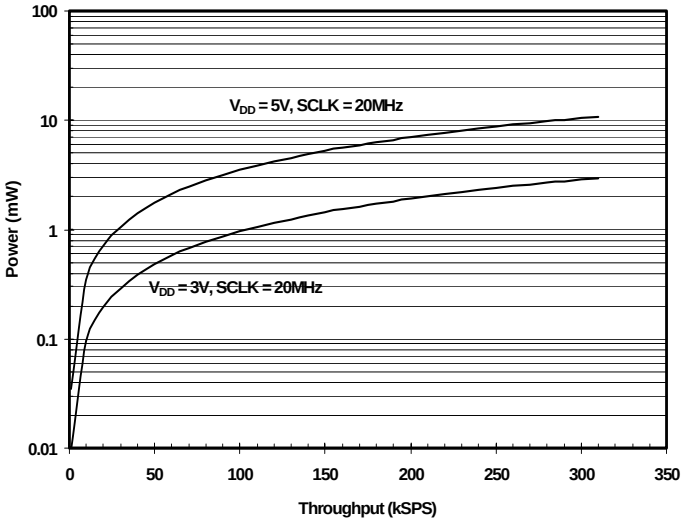


Figure 21. Power vs Throughput

SERIAL INTERFACE

Figures 22, 23 and 24 show the detailed timing diagram for serial interfacing to the AD7476A, AD7477A and AD7478A respectively. The serial clock provides the conversion clock and also controls the transfer of information from the AD7476A/AD7477A/AD7478A during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of three-state and the analog input is sampled at this point. The conversion is also initiated at this point, for the AD7476A it will require 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed the track and hold will go back into track on the next SCLK rising edge as shown in Figure 22 at point B. On the 16th SCLK falling edge the SDATA line will go back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into three-state; otherwise, SDATA returns to three-state on the 16th SCLK falling edge as shown in Figure 22. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7476A.

For the AD7477A, the 14th SCLK falling edge will cause the SDATA line to go back into three-state. If the rising edge of $\overline{CS}$ occurs before 14 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into three-state; otherwise, SDATA returns to three-state on the 14th SCLK falling edge as shown in Figure 23. The track and hold will go back into track on the rising edge after the 13th falling, as shown in Figure 23 at point B. Fourteen serial clock cycles are required to perform the conversion process and to access data from the AD7477A.

For the AD7478A, the 12th SCLK falling edge will cause the SDATA line to go back into three-state. If the rising edge of $\overline{CS}$ occurs before 12 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into three-state; otherwise, SDATA returns to three-state on the 12th SCLK falling edge as shown in Figure 24. The track and hold will go back into track on the rising edge after the 11th falling, as shown in Figure 24 at point B. Twelve serial clock cycles are required to perform the conversion process and to access data from the AD7478A.

$\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero. Thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. For the AD7476A the final bit in the data transfer is valid on the 16th falling edge, having being clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge, i.e, the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the first leading zero provided and the 15th rising SCLK edge would have DB0 provided.

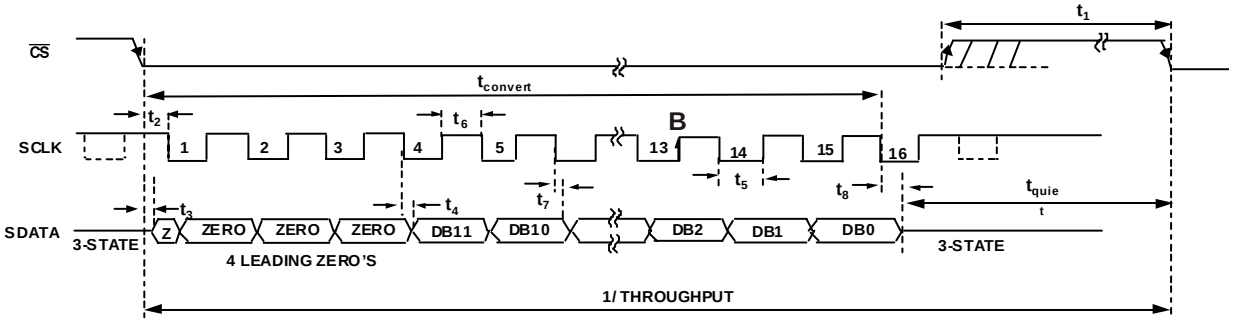


Figure 22. AD7476A Serial Interface Timing Diagram

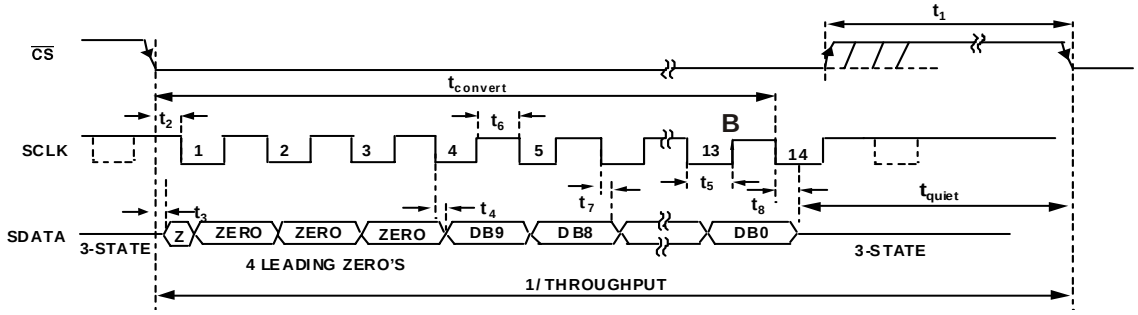


Figure 23. AD7477A Serial Interface Timing Diagram

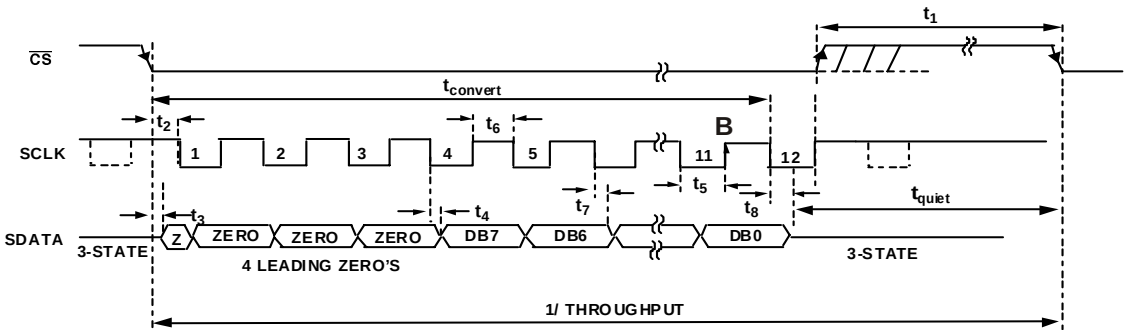


Figure 24. AD7478A Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7476A/AD7477A/AD7478A allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7476A/AD7477A/AD7478A with some of the more common microcontroller and DSP serial interface protocols.

AD7476A/AD7477A/AD7478A to TMS320C541 Interface

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7476A/AD7477A/AD7478A. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7476A/AD7477A/AD7478A without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode (FSM=1 in the Serial Port Control register, SPC) with internal serial clock CLKX (MCM=1 in SPC register) and internal frame signal (TXM=1 in the SPC), so both pins are configured as an outputs. For the AD7476A the word length should be set to 16 bits (FO=0 in the SPC register). This DSP only allows frames with a word length of 16 or 8 bits. Therefore, in the case of the AD7477A and AD7478A where 14 and 12 bits would be required, the FO bit will be set up to 16 bits also. This means to obtain the conversion result 16 SCLKs will be needed. In both situations, the remaining SCLKs will clock out trailing zeros. For the AD7477A two trailing zeros will be clocked out in the two last clock cycles, for the AD7478A 4 trailing zeros will be clocked out.

To summarise, the values in the SPC register are:

FO=0
FSM=1
MCM=1
TXM=1

The format bit, FO, may be set to 1 to set the word length to 8-bits, in order to implement the Power-Down mode on the AD7476A/AD7477A/AD7478A.

The connection diagram is shown in Figure 25. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the TMS320C541 will provide equidistant sampling.

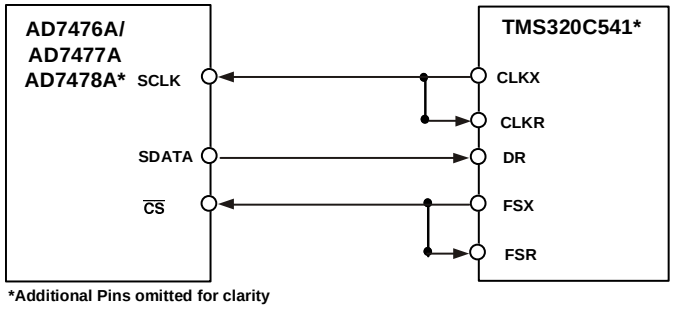


Figure 25. Interfacing to the TMS320C541

AD7476A/AD7477A/AD7478A to ADSP218x

The ADSP218x family of DSPs are interfaced directly to the AD7476A/AD7477A/AD7478A without any glue logic required. The SPORT control register should be set up as follows:

TFSW= RFSW= 1, Alternate Framing
INVRFS= INVTFS= 1, Active Low Frame Signal
DTYPE= 00, Right Justify Data
ISCLK= 1, Internal Serial Clock
TFSR= RFSR= 1, Frame Every Word
IRFS= 0, it sets up RFS as an Input
ITFS= 1, it sets up TFS as an Output
SLEN= 1111, 16 bits for the AD7476A
SLEN= 1101, 14 bits for the AD7477A
SLEN= 1011, 12 bits for the AD7478A

To implement the Power-Down mode SLEN should be set to 1001 to issue an 8-bit SCLK burst. The connection diagram is shown in Figure 26. The ADSP218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates

in Alternate Framing Mode and the SPORT control register is set up as described. The frame synchronisation signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

The timer registers etc., are loaded with a value which will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, i.e. AX0= TX0, the state of the SCLK is checked. The DSP will wait until the SCLK has gone high, low and high before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP2111 has a master clock frequency of 16MHz. If the SCLKDIV register is loaded with the value 3 then a SCLK of 2MHz is obtained, and 8 master clock periods will elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occuring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N then equidistant sampling will be implemented by the DSP.

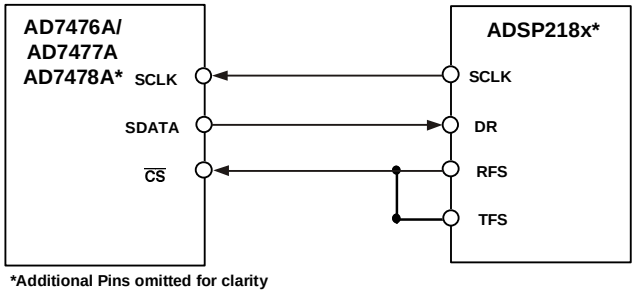


Figure 26. Interfacing to the ADSP-218x

AD7476A/AD7477A/AD7478A to DSP563xx Interface
The connection diagram in Figure 27 shows how the AD7476A/AD7477A/AD7478A can be connected to the SSI (Synchronous Serial Interface) of the DSP563xx family of DSPs from Motorola. The SSI is operated in Synchronous and Normal Mode (SYN=1 and MOD=0 in the Control Register B, CRB) with internally generated 1-bit clock period frame sync for both Tx and Rx (bits FSL1=1 and FSL0=0 in the CRB). Set the word length in the Control Register A (CRA) to 16 by setting bits WL2=0, WL1=1 and WL0=0 for the AD7476A. The word length for the AD7478A will be set to 12 bits (WL2=0, WL1=0 and WL0=1). This DSP does not offer the option for a 14 bits word length, so the AD7477A word length will be set up to 16 bits like the AD7476A. For the AD7477A the conversion process will use 16 SCLKs cycles, with the last two clock periods clocking out two trailing zeros to fill the 16 bits word.
To implement the Power-Down mode on the AD7476A/AD7477A/AD7478A, the word length can be changed to 8 bits by setting bits WL2=0, WL1=0 and WL0=0 in CRA. The FSP bit in the CRB register can be set to 1, that means that the frame goes low and a conversion starts. Likewise, by means of the bits SCD2, SCKD and SHFD in the CRB register, it will be established that the pin SC2 (the frame sync signal) and SCK in the serial port will be configured as outputs and the MSB will be shifted first. To sum up,

MOD=0
SYN=1
WL2, WL1, WL0 depend on the word length
FSL1=1, FSL0=0
FSP=1, negative frame sync
SCD2=1
SCKD=1
SHFD=0

It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the DSP563xx will provide equidistant sampling.

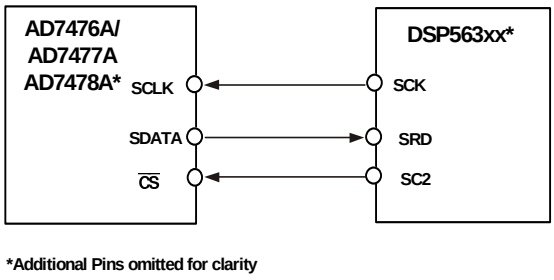


Figure 27. Interfacing to the DSP563xx

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead SC70 (KS)