





2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-87713
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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C 4.5 V < V <sub>CC</sub> < 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input low voltage	V <sub>IL</sub>	1/	1, 2, 3	-0.5	0.8	V
Input high voltage	V <sub>IH</sub>	1/	1, 2, 3	2.2	V <sub>CC</sub> +0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA	1, 2, 3		0.45	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -200 μA	1, 2, 3	2.4		V
Input leakage current	I <sub>IL</sub>	V <sub>IN</sub> = V <sub>CC(max)</sub> to 0 V (pin 10 is guaranteed but not tested)	1, 2, 3		±10	μA
Output float leakage current	I <sub>OFL</sub>	V <sub>OUT</sub> = V <sub>CC(max)</sub> to 4.5 V data bus	1, 2, 3		±10	μA
V <sub>CC</sub> supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	1, 2, 3		240	mA
Input capacitance	C <sub>IN</sub>	See 4.3.1c	4		10	pF
Output capacitance	C <sub>OUT</sub>	See 4.3.1c	4		15	pF
Input/output capacitance	C <sub>I/O</sub>	See 4.3.1c	4		20	pF
Functional tests		See 4.3.1d	7,8			
Clock period	t <sub>CY</sub>	2/	9,10,11	250	4000	ns
CLK low time	t <sub>CL</sub>	2/	9,10,11	105	2000	ns
CLK high time	t <sub>CH</sub>	2/	9,10,11	105	2000	ns
CLK rise time	t <sub>r</sub>	1/ 2/	9,10,11	0	30	ns
Clock fall time	t <sub>f</sub>	2/	9,10,11	0	30	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C 4.5 V < V <sub>CC</sub> < 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
A <sub>0</sub> , A <sub>1</sub> setup to $\overline{RD}$ neg. edge	t <sub>AR</sub>	<u>2/</u>	9,10,11	0		ns
A <sub>0</sub> , A <sub>1</sub> data output delay	t <sub>AD</sub>	C <sub>L</sub> = 150 pF <u>2/</u>	9,10,11		200	ns
A <sub>0</sub> , A <sub>1</sub> hold after $\overline{RD}$ neg. edge	t <sub>RA</sub>	<u>2/</u>	9,10,11	70		ns
$\overline{RD}$ neg. edge to data output delay	t <sub>RD</sub>	C <sub>L</sub> = 150 pF <u>2/</u>	9,10,11		245	ns
$\overline{RD}$ pulse width	t <sub>RR</sub>	<u>2/</u>	9,10,11	250		ns
Output float delay	t <sub>DF</sub>	<u>2/</u>	9,10,11		120	ns
$\overline{CS}$ , A <sub>0</sub> , A <sub>1</sub> setup to $\overline{WR}$ neg. edge	t <sub>AW</sub>	<u>2/</u>	9,10,11	0		ns
$\overline{CS}$ , A <sub>0</sub> , A <sub>1</sub> hold after $\overline{WR}$ pos. edge	t <sub>WA</sub>	<u>2/</u>	9,10,11	0		ns
$\overline{WR}$ pulse width	t <sub>WW</sub>	<u>2/</u>	9,10,11	320		ns
Data setup to $\overline{WR}$ pos. edge	t <sub>DW</sub>	<u>2/</u>	9,10,11		150	ns
Data hold after $\overline{WR}$ pos. edge	t <sub>WD</sub>	<u>2/</u>	9,10,11	0		ns
IPI setup top INTA neg. edge	t <sub>PI</sub>	<u>2/</u>	9,10,11	0		ns
IPI hold after INTA pos. edge	t <sub>IP</sub>	<u>2/</u>	9,10,11	10		ns
INTA pulse width	t <sub>II</sub>	<u>2/</u>	9,10,11	250		ns
IPI neg. edge to IPO delay	t <sub>PIPO</sub>	<u>2/</u>	9,10,11		100	ns
INTA neg. edge to data output delay	t <sub>ID</sub>	<u>2/</u>	9,10,11		245	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V < V <sub>CC</sub> < 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
R <sub>D</sub> or $\overline{W}$ R to DRQ neg. edge	t <sub>CQ</sub>	<u>2/</u>	9,10,11		150	ns
Recovery time between controls	t <sub>RV</sub>	<u>2/</u>	9,10,11	300		ns
$\overline{CS}$ , A <sub>0</sub> , A <sub>1</sub> to RDY <sub>A</sub> or RDY <sub>B</sub> delay	t <sub>CW</sub>	<u>2/</u>	9,10,11		140	ns
Data clock cycle	t <sub>DCY</sub>	<u>2/</u>	9,10,11	4.5		t <sub>CY</sub>
Data clock low time	t <sub>DCL</sub>	<u>2/</u>	9,10,11	180		ns
Data clock high time	t <sub>DCH</sub>	<u>2/</u>	9,10,11	180		ns
$\overline{Tx}$ C to TxD delay	t <sub>TD</sub>	<u>2/</u>	9,10,11		300	ns
RxD setup to $\overline{Rx}$ C pos. edge	t <sub>DS</sub>	<u>2/</u>	9,10,11	0		ns
RxD hold after $\overline{Rx}$ C pos. edge	t <sub>DH</sub>	<u>2/</u>	9,10,11	140		ns
$\overline{Tx}$ C to INT delay	t <sub>ITD</sub>	<u>1/ 2/</u>	9,10,11	4	6	t <sub>CY</sub>
RxC to INT delay	t <sub>IRD</sub>	<u>1/ 2/</u>	9,10,11	7	10	t <sub>CY</sub>
$\overline{CTS}$ , $\overline{CD}$ , SYNDET low time	t <sub>PL</sub>	<u>2/</u>	9,10,11	200		ns
$\overline{CTS}$ , $\overline{CD}$ , SYNDET high time	t <sub>PH</sub>	<u>2/</u>	9,10,11	200		ns
Ext. INT from $\overline{CTS}$ , $\overline{CD}$ , SYNDET	t <sub>IPD</sub>	<u>2/</u>	9,10,11		500	ns

1/ Guaranteed if not tested.

2/ AC test conditions (See figure 3):

Input high level: V<sub>IH</sub> = 2.4 V

Input low level: V<sub>IL</sub> = 0.45 V

Output voltage high: V<sub>OH</sub> = 2.0 V

Output voltage low: V<sub>OL</sub> = 0.8 V

Input rise/fall times: t<sub>r</sub>/t<sub>f</sub> < 10.0 ns

Timing measurements are made at 2.0 V for logic "1" and 0.8 V for logic "0".

Output load = 100 pF including test jig.

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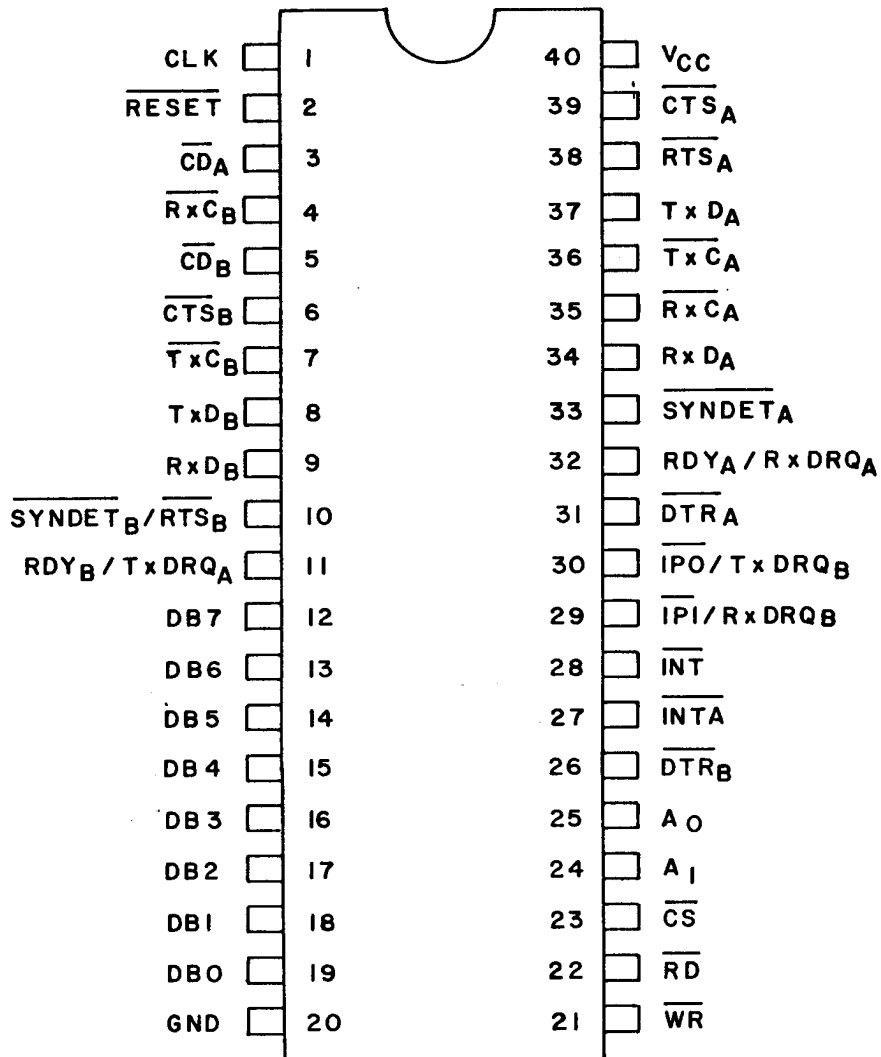


FIGURE 1. Terminal connections.

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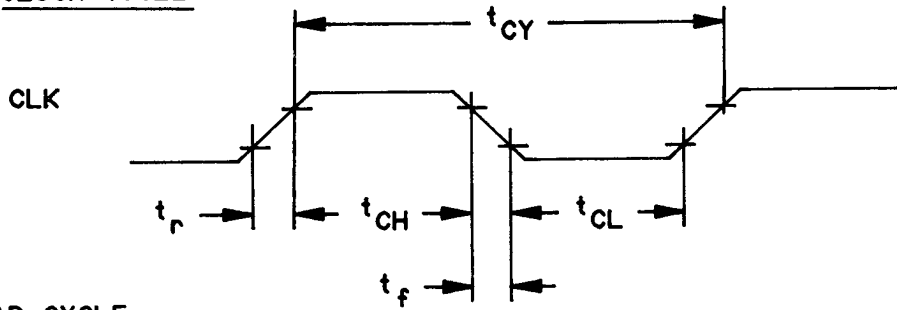
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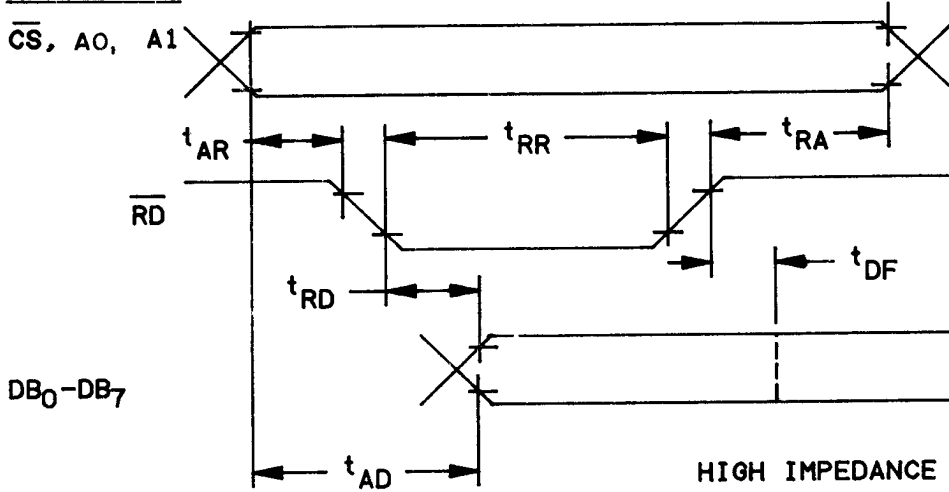




CLOCK CYCLE



READ CYCLE



WRITE CYCLE

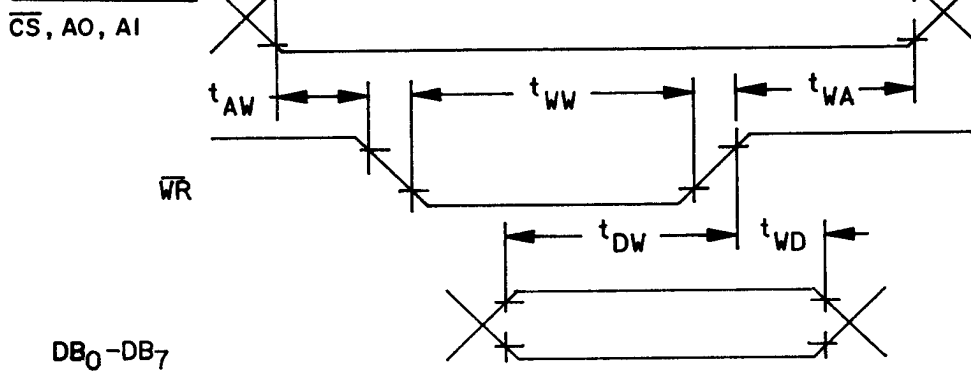
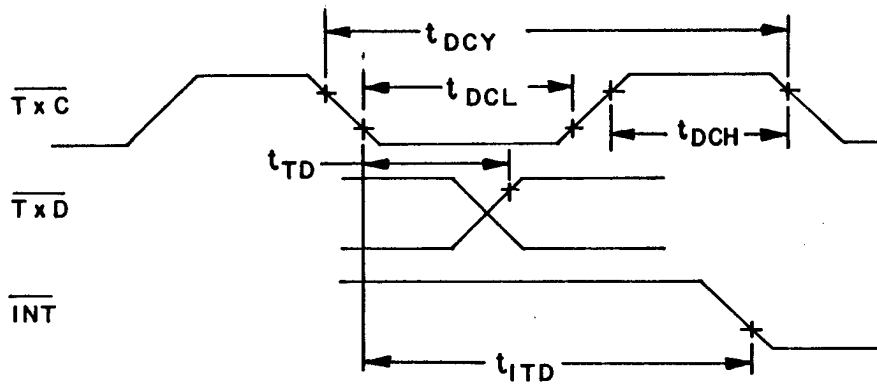


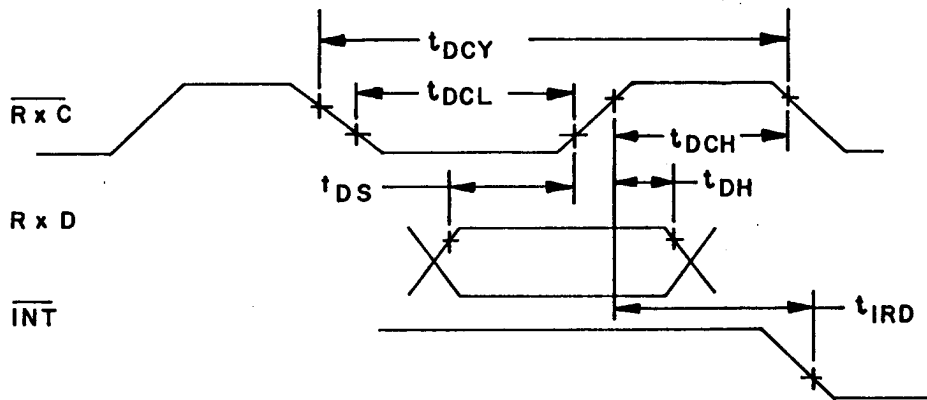
FIGURE 3. Timing diagram.

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**TRANSMIT DATA CYCLE**



**RECEIVE DATA CYCLE**



**OTHER TIMING**

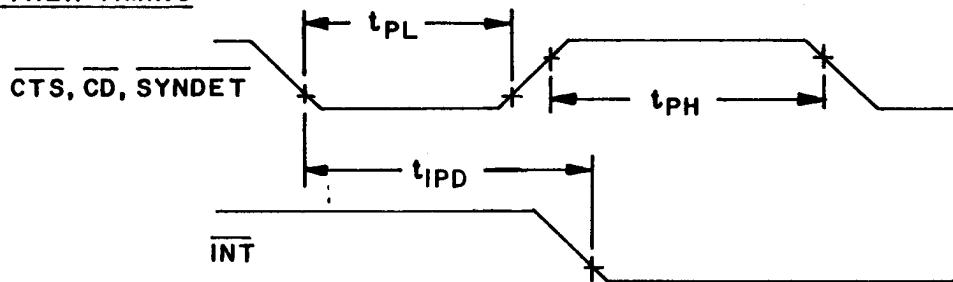


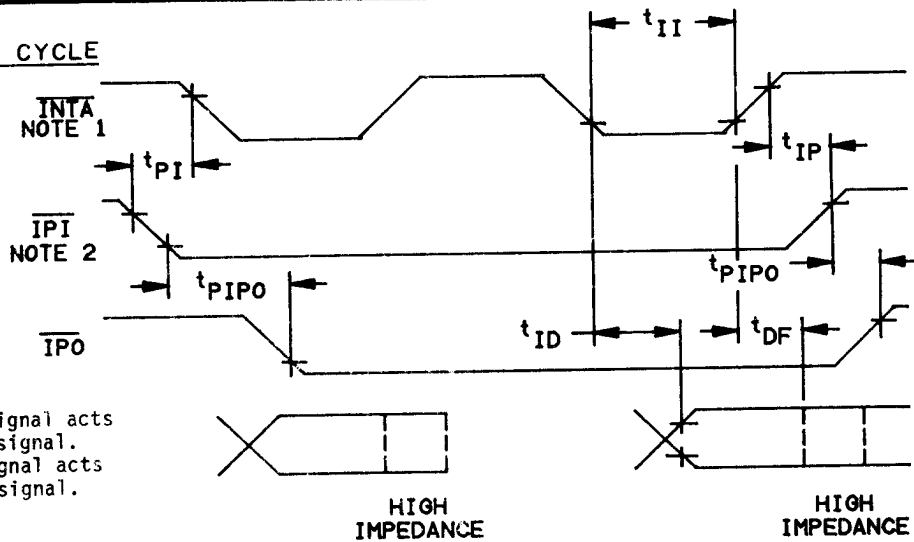
FIGURE 3. Timing diagram - Continued.

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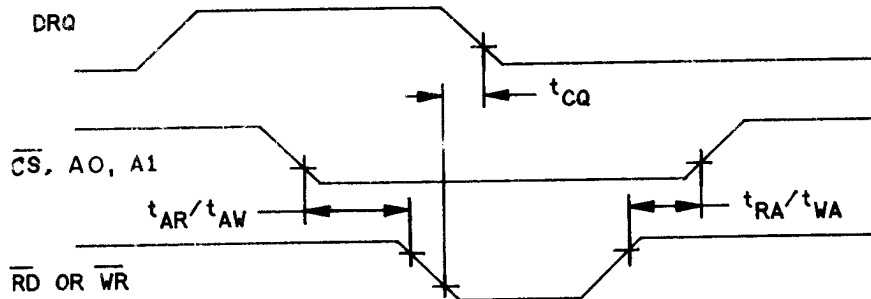
**INTA CYCLE**



**NOTES:**

1. INTA signal acts as RD signal.
2. TPI signal acts as CS signal.

**DMA CYCLE**



**READ/WRITE CYCLE (SOFTWARE POLLED MODE)**

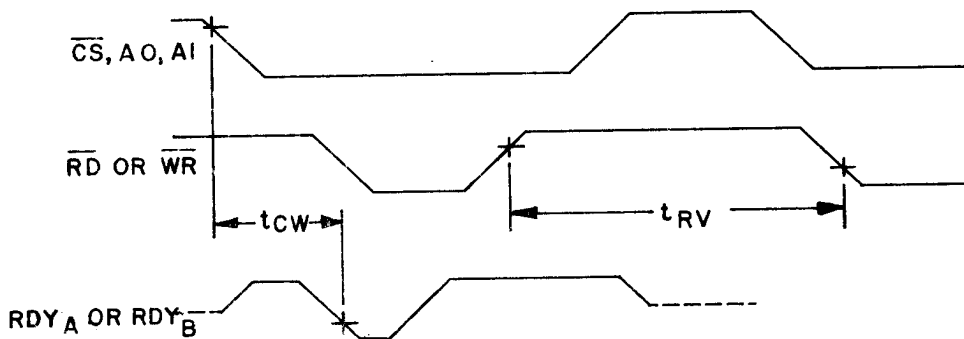


FIGURE 3. Timing diagram - Continued.

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3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
  - (1) Test condition A, B, C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$ ,  $C_{OUT}$  and  $C_{I/O}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.
- d. Subgroups 7 and 8 tests shall verify the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
  - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8(hot),10
Additional electrical subgroups for group C periodic inspections	---

\* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>	Replacement military specification part number
5962-8771301QX	34649	MD8274/B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

34649

Vendor name and address

Intel Corporation  
5000 W. Williams Field Road  
Chandler, AZ 85224

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