FUJITSU SEMICONDUCTOR
DATA SHEET

Version 4.0

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90460/5 Series

MB90462/467/F462/F462A/F463A/V460

■ DESCRIPTION

The MB90460/5 series is a line of general-purpose, Fujitsu 16-bit microcontrollers designed for process control applications which require high-speed real-time processing, such as consumer products.

While inheriting the AT architecture of the F²MC*1 family, the instruction set for the F²MC-16LX CPU core of the MB90460/5 series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90460/5 series has an on-chip 32-bit accumulator which enables processing of long-word data.

The peripheral resources integrated in the MB90460/5 series include: an 8/10-bit A/D converter, UARTs (SCI) 0 to 1, 16-bit PPG timer, multi-functional timer (16-bit free-running timer, input capture units (ICUs) 0 to 3, output compare units (OCUs) 0 and 5, 16-bit PPG timer, waveform generator), multi-pulse generator (16-bit PPG timer*2, 16-bit reload timer, waveform sequencer*2), PWC*2 0 to 1, 16-bit reload timer and DTP/external interrupt.

Notes: *1: F²MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.
*2: Multi-pulse generator and PWC 0 exist only in MB90460 series, ie, 16-bit PPG timer 1, waveform sequencer and PWC 0 are not present in MB90465 series (See section "■ BLOCK DIAGRAM").

■ FEATURES

- Minimum execution time: 62.5 ns / 4 MHz oscillation (uses PLL clock multiplication) maximum multiplier = 4
- Maximum memory space
  16 Mbyte
  Linear/bank access

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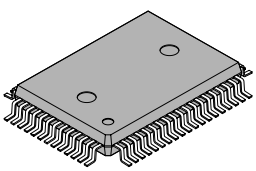
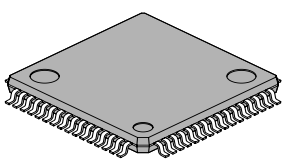
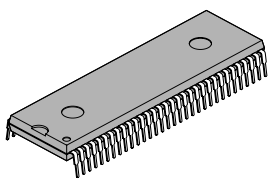
■ PACKAGES

64-pin plastic QFP	64-pin plastic LQFP	64-pin plastic SH-DIP
		
(FPT-64P-M06)	(FPT-64P-M09)	(DIP-64P-M01)

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- Instruction set optimized for controller applications
  Supported data types : bit, byte, word, and long-word types
  Standard addressing modes : 23 types
  32-bit accumulator enhancing high-precision operations
  Signed multiplication/division and extended RETI instructions
- Enhanced high level language (C) and multi-tasking support instructions
  Use of a system stack pointer
  Symmetrical instruction set and barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed : 4 byte instruction queue
- Enhanced interrupt function
  Up to eight priority levels programmable
  External interrupt inputs : 8 lines
- Automatic data transmission function independent of CPU operation
  Up to 16 channels for the extended intelligent I/O service
  DTP request inputs : 8 lines
- Internal ROM
  FLASH : 64 Kbyte with flash security (MB90F462/F462A), 128Kbyte with flash security (MB90F463A)
  MASKROM : 64 Kbyte
- Internal RAM
  EVA : 8 Kbyte
  FLASH : 2 Kbyte
  MASKROM : 2 Kbyte
- General-purpose ports
  Up to 51 channels (input pull-up resistor settable for : 16 channels)
- A/D Converter (RC) : 8 channels
  8/10-bit resolution selectable
  Conversion time : Min. 6.13 μs, 16 MHz operation
- UART : 2 channels
- 16-bit PPG : 3 channels (MB90460 series), 2 channels (MB90465 series)
  Mode switching function provided (PWM mode or one-shot mode)
  Can be worked with multi-functional timer, multi-pulse generator (MB90460 series only) or individually
- 16-bit reload timer : 2 channels
  Can be worked with multi-pulse generator (MB90460 series only) or individually
- 16-bit PWC timer : 2 channels (MB90460 series), 1 channel (MB90465 series)
- Multi-functional timer
  Input capture : 4 channels
  Output compare with selectable buffer : 6 channels
  Free-running timer with up or up-down mode selection and selectable buffer: 1 channel
  16-bit PPG : 1 channel
  Waveform generator : (16-bit timer : 3 channels, 3-phase waveform or dead time)
- Multi-pulse generator
  16-bit PPG : 1 channel (MB90460 series only)
  16-bit reload timer : 1 channel
  Waveform sequencer : (16-bit timer with buffer and compare clear function) (MB90460 series only)
- Timebase counter/watchdog timer : 18-bit

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- Low-power consumption mode :
  Sleep mode
  Stop mode
  CPU intermittent operation mode
- Package :
  LQFP-64 (FPT-64P-M09 : 0.65 mm pitch)
  QFP-64 (FPT-64P-M06 : 1.00 mm pitch)
  SDIP-64 (DIP-64P-M01 : 1.78 mm pitch)
- CMOS technology

■ PRODUCT LINEUP

Part number / Item	MB90V460	MB90F462	MB90F462A	MB90F463A	MB90462	MB90467
Classification	Development / evaluation product	Mass-produced products (Flash ROM with flash security)			Mass-produced products (Mask ROM)	
ROM size	—	64K Bytes		128K Bytes	64K Bytes	
RAM size	8K Bytes	2K Bytes				
CPU function	Number of instruction : 351 Minimum execution time : 62.5 ns / 4 MHz (PLL x 4) Addressing mode : 23 Data bit length : 1, 8, 16 bits Maximum memory space : 16 MBytes					
I/O port	I/O port (CMOS) : 51					
PWC	Pulse width counter timer : 2 channels					1 channel
	Timer function (select the counter timer from three internal clocks) Various pulse width measuring function (H pulse width, L pulse width, rising edge to falling edge period, falling edge to rising edge period, rising edge to rising edge period and falling edge to falling edge period)					
UART	UART : 2 channels With full-duplex double buffer (8-bit length) Clock asynchronized or clock synchronized transmission (with start and stop bits) can be selectively used Transmission can be one-to-one (bidirectional commuication) or one-to-n (master-slave communication)					
16-bit reload timer	Reload timer : 2 channels Reload mode, single-shot mode or event count mode selectable Can be worked with multi-pulse generator or individually (MB90460 series only)					
16-bit PPG timer	PPG timer : 3 channels					2 channels
	PWM mode or single-shot mode selectable Can be worked with multi-functional timer, multi-pulse generator (MB90460 series only) or individually					

Part number / Item	MB90V460	MB90F462	MB90F462A	MB90F463A	MB90462	MB90467
Multi-functional timer (for AC/DC motor control)	16-bit free-running timer with up or up-down mode selection and buffer: 1 channel 16-bit output compare : 6 channels 16-bit input capture : 4 channels 16-bit PPG timer : 1 channel Waveform generator (16-bit timer: 3 channels, 3-phase waveform or dead time)					
Multi-pulse generator (for DC motor control)	16-bit PPG timer : 1 channel Waveform sequencer (includes 16-bit timer with buffer and compare clear function)					Not present
	16-bit reload timer operation (toggle output, one-shot output selectable) Event counter function : 1 channel built-in					
8/10-bit A/D converter	8/10-bit resolution (8 channels) Conversion time : Min. 6.13 µs (16 MHz internal clock)					
DTP/External interrupt	8 independent channels Selectable causes : Rising edge, falling edge, “L” level or “H” level					
Low-power consumption	Stop mode / Sleep mode / CPU intermittent operation mode					
Package	PGA256	LQFP-64 (FPT-64P-M09 : 0.65 mm pitch) QFP-64 (FPT-64P-M06 : 1.00 mm pitch) SDIP-64 (DIP-64P-M01 : 1.78 mm pitch)				
Power supply voltage for operation*	4.5 V to 5.5 V*					
Process	CMOS					

* : Varies with conditions such as the operating frequency (See section “■ ELECTRICAL CHARACTERISTICS”). Assurance for the MB90V460 is given only for operation with a tool at a power supply voltage of 4.5 V to 5.5 V, an operating temperature of 0 to +25 °C, and an operating frequency of 1 MHz to 16 MHz.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90V460	MB90F462	MB90F462A	MB90F463A	MB90462	MB90467
PGA256	○	X	X	X	X	X
FPT-64P-M09	X	○	○	○	○	○
FTP-64P-M06	X	○	○	○	○	○
DIP-64P-M01	X	○	○	○	○	○

○ : Available
X : Not available

Note: For more information about each package, see section “■ PACKAGE DIMENSIONS”.

■ DIFFERENCES AMONG PRODUCTS

Memory Size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V460 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V460, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF3FFF_H$ are mapped to bank FF only. (This setting can be changed by configuring the development tool.)
- In the MB90462/467/F462/F462A/F463A, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FF0000_H$ to $FF3FFF_H$ are mapped to bank FF only.

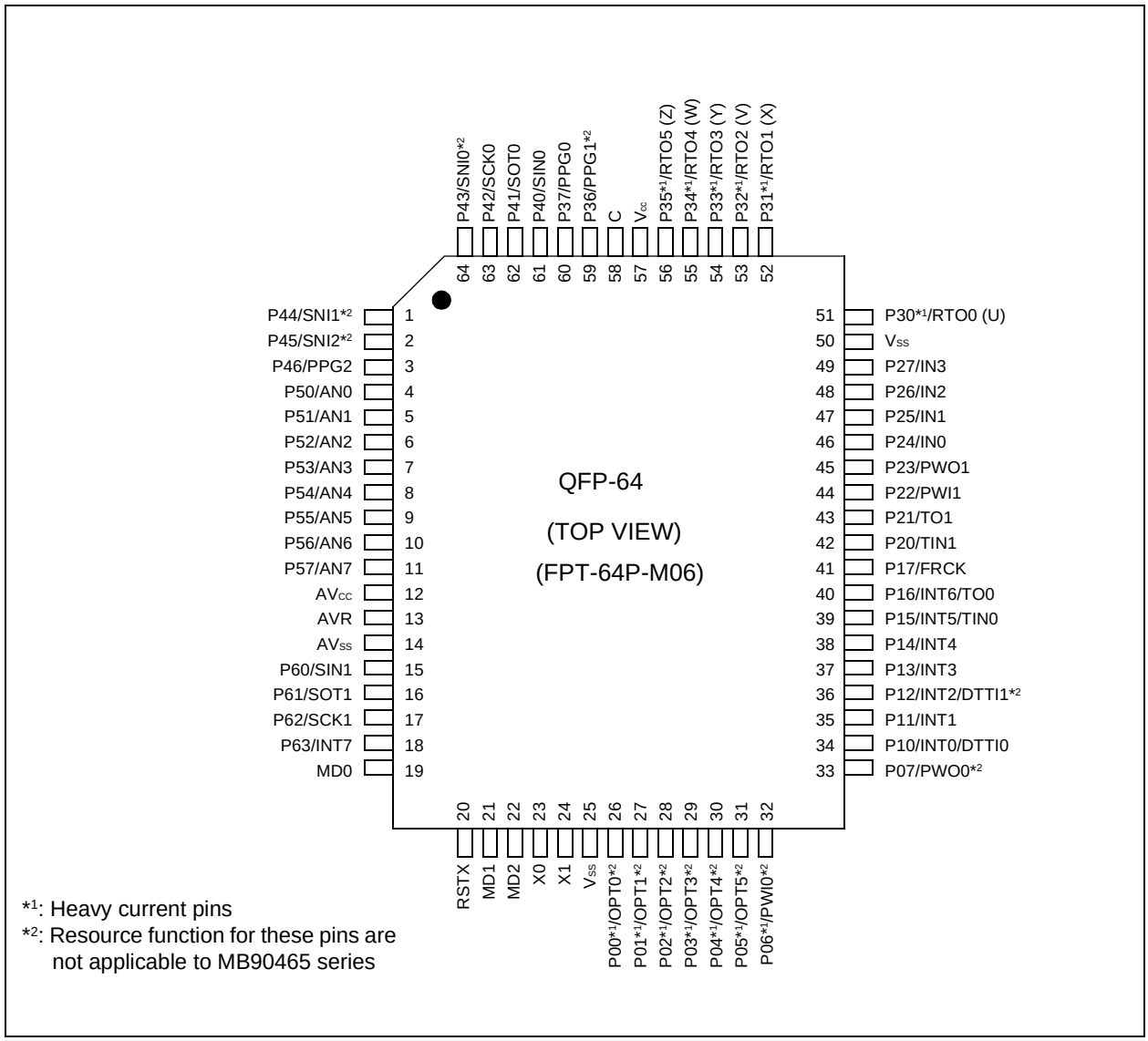
Difference between MB90460 series and MB90465 series

- Waveform sequencer, 16-bit PPG timer 1, and PWC 0 are not present in MB90465 series.

Difference between MB90F462, MB90F462A and MB90F463A

- 64Kbytes flash ROM is avaliable in MB90F462 and MB90F462A while 128Kbytes flash ROM is avaliable in MB90F463A.

■ PIN ASSIGNMENT



*1: Heavy current pins
*2: Resource function for these pins are not applicable to MB90465 series

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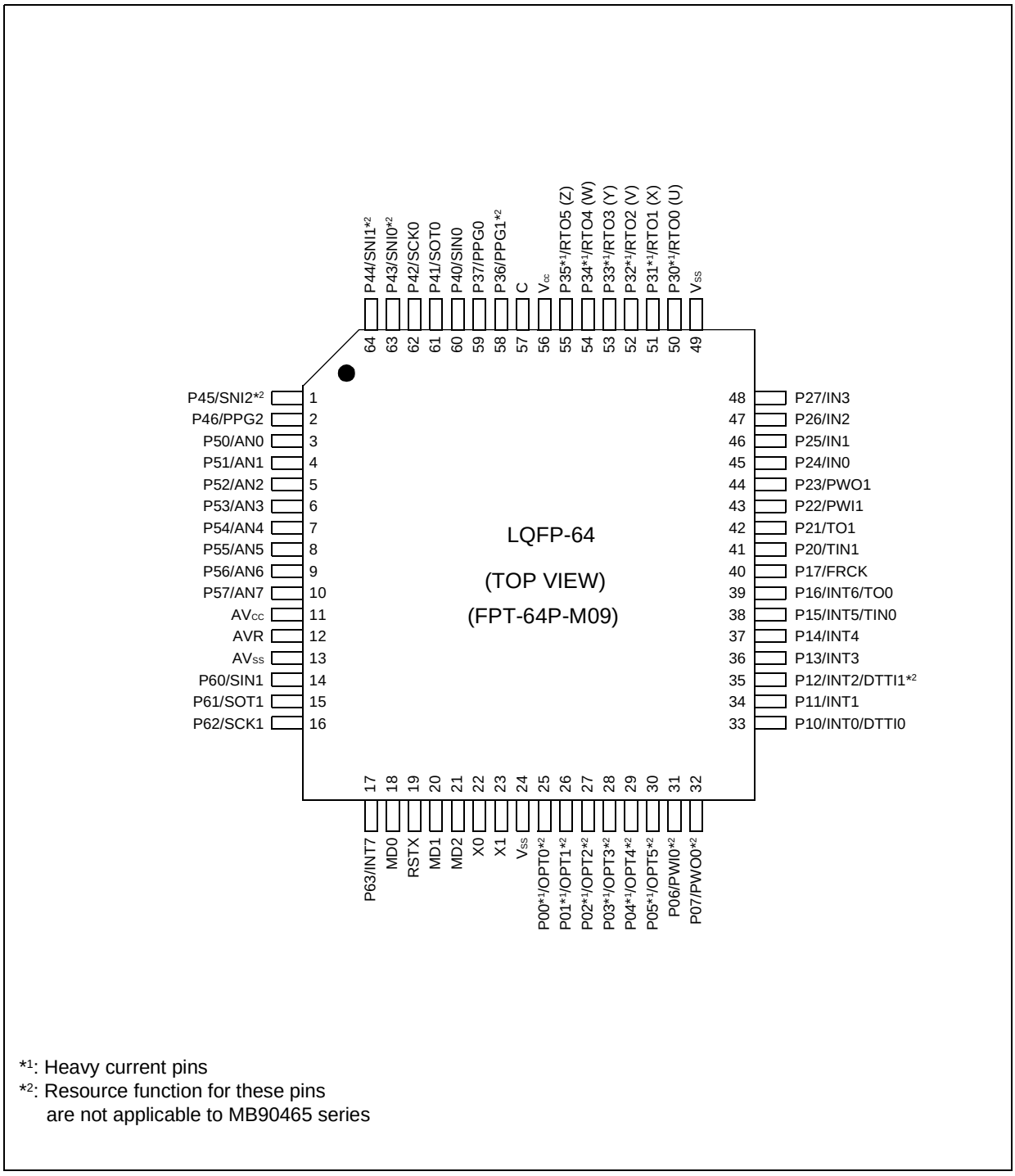

*1: Heavy current pins
*2: Resource function for these pins
are not applicable to MB90465 series

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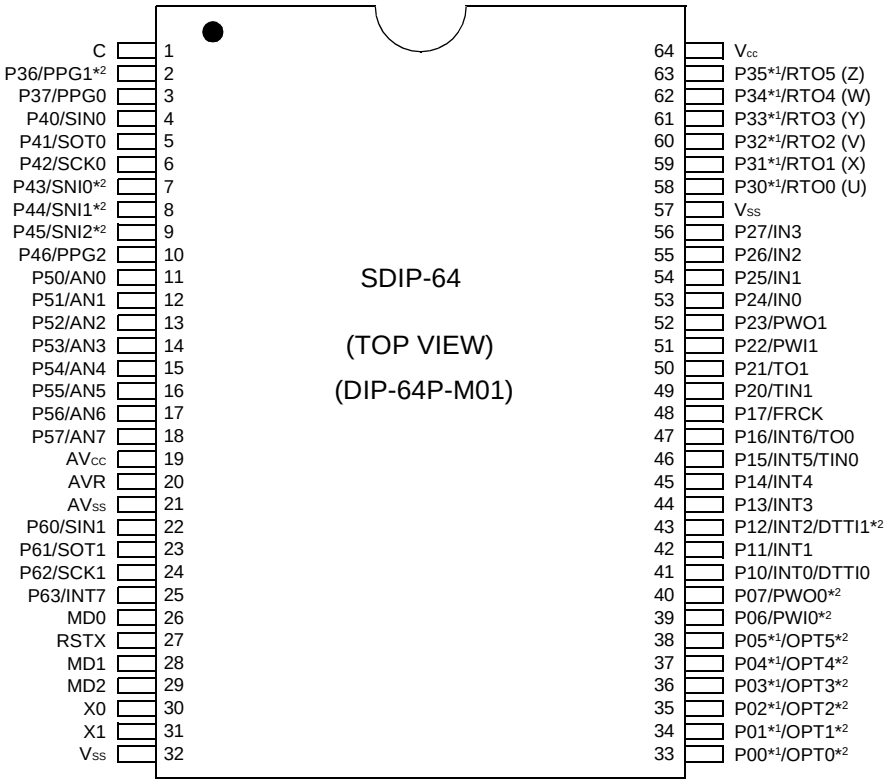


*1: Heavy current pins
*2: Resource function for these pins
are not applicable to MB90465 series

■ PIN DESCRIPTION

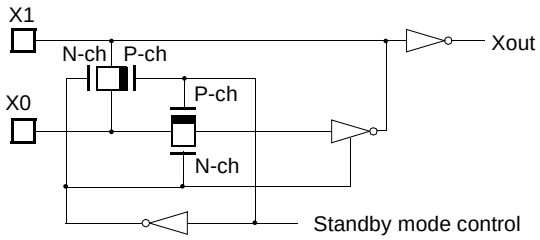
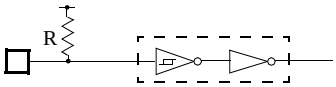
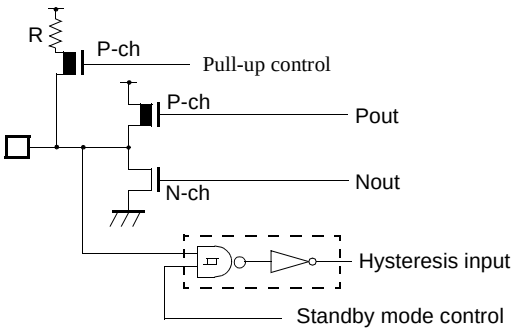
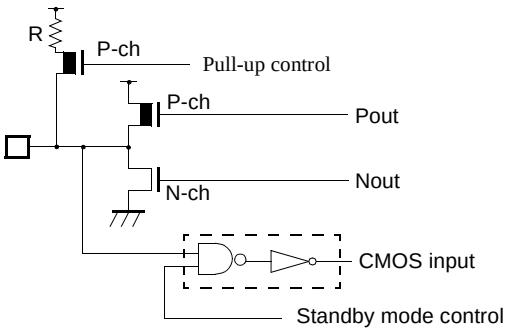
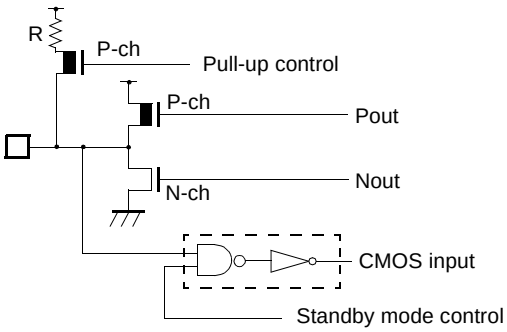
Pin no.			Pin name	I/O circuit	Pin status during reset	Function
LQFP-M09*1	QFP-M06*2	SDIP*3				
22,23	23,24	30,31	X0,X1	A	Oscillating	Oscillation input pins.
19	20	27	RSTX	B	Reset input	External reset input pin.
25~30	26~31	33~38	P00 ~ P05	D	Port input	General-purpose I/O ports.
			OPT0 ~ OPT5*4			Output terminals OPT0~5 of the waveform sequencer. These pins output the waveforms specified at the output data registers of the waveform sequencer circuit. Output is generated when OPE0~5 of OPCR is enabled.
31	32	39	P06	E		General-purpose I/O ports.
			PWI0*4			PWC 0 signal input pin.
32	33	40	P07	E		General-purpose I/O ports.
			PWO0*4			PWC 0 signal output pin.
33	34~35	41~42	P10	C		General-purpose I/O ports.
			INT0			Can be used as interrupt request input channels 0. Input is enabled when 1 is set in EN0 in standby mode.
			DTTI0			RTO0~5 pins for fixed-level input. This function is enabled when the waveform generator enables its input bits.
34	35	42	P11	C		General-purpose I/O ports.
			INT1			Can be used as interrupt request input channels 1. Input is enabled when 1 is set in EN1 in standby mode.
35	36	43	P12	C		General-purpose I/O ports.
			INT2			Can be used as interrupt request input channels 2. Input is enabled when 1 is set in EN2 in standby mode.
			DTTI1*4			OPT0~5 pins for fixed-level input. This function is enabled when the waveform sequencer enables its input bit.
36~37	37~38	44~45	P13 ~ P14	C		General-purpose I/O ports.
			INT3 ~ INT4			Can be used as interrupt request input channels 3 to 4. Input is enabled when 1 is set in EN3 to EN4 in standby mode.
38	39	46	P15	C		General-purpose I/O ports.
			INT5			Can be used as interrupt request input channel 5. Input is enabled when 1 is set in EN5 in standby mode.
			TIN0			External clock input pin for reload timer 0.
39	40	47	P16	C		General-purpose I/O ports.
			INT6			Can be used as interrupt request input channels 6. Input is enabled when 1 is set in EN6 in standby mode.
			TO0			Event output pin for reload timer 0.
40	41	48	P17	C		General-purpose I/O ports.
			FRCK			External clock input pin for free-running timer.
41	42	49	P20	F		General-purpose I/O ports.
			TIN1			External clock input pin for reload timer 1.

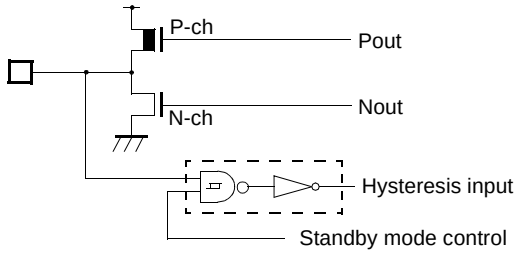
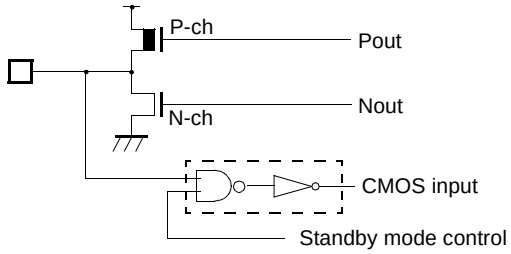
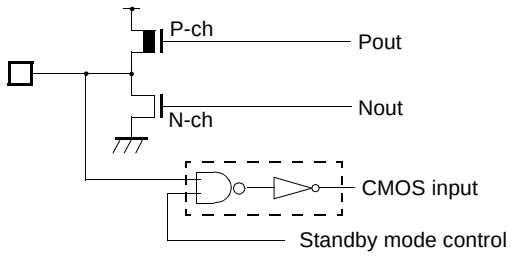
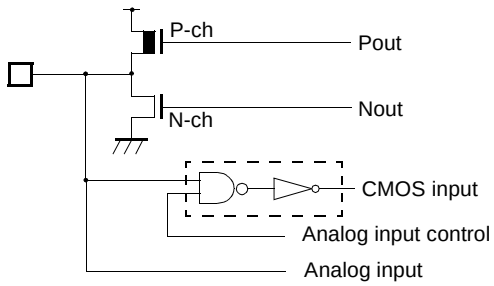
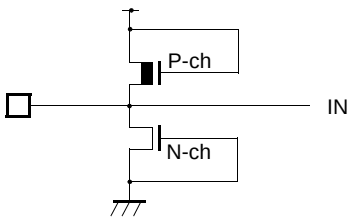
Pin no.			Pin name	I/O circuit	Pin status during reset	Function
LQFP-M09*1	QFP-M06*2	SDIP*3				
42	43	50	P21	F	Port input	General-purpose I/O ports.
			TO1			Event output pin for reload timer 1.
43	44	51	P22	F		General-purpose I/O ports.
			PWI1			PWC 1 signal input pin.
44	45	52	P23	F		General-purpose I/O ports.
			PWO1			PWC 1 signal output pin.
45~48	46~49	53~56	P24 ~ P27	F		General-purpose I/O ports.
			IN0 ~ IN3			Trigger input pins for input capture channels 0 to 3. When input capture channels 0 to 3 are used for input operation, these pins are enabled as required and must not be used for any other I/P.
50~55	51~56	58~63	P30 ~ P35	G		General-purpose I/O ports.
			RTO0 ~ RTO5			Waveform generator output pins. These pins output the waveforms specified at the waveform generator. Output is generated when waveform generator output is enabled.
58~59	59~60	2~3	P36 ~ 37	H		General-purpose I/O ports.
			PPG1*4, PPG0			Output pins for PPG channels 1, 0. This function is enabled when PPG channels 1, 0 enable output.
60	61	4	P40	F		General-purpose I/O ports.
			SIN0			Serial data input pin for UART channel 0. While UART channel 0 is operating for input, the input of this pin is used as required and must not be used for any other input.
61	62	5	P41	F		General-purpose I/O ports.
			SOT0			Serial data output pin for UART channel 0. This function is enabled when UART channel 0 enables data output.
62	63	6	P42	F		General-purpose I/O ports.
			SCK0			Serial clock I/O pin for UART channel 0. This function is enabled when UART channel 0 enables clock output.
63	64	7	P43	F		General-purpose I/O ports.
			SNI0*4			Trigger input pins for position detection of the waveform sequencer. When this pin is used for input operation, it is enabled as required and must not be used for any other I/P.
64	1	8	P44	F		General-purpose I/O ports.
			SNI1*4			Trigger input pins for position detection of the Multi-pulse generator. When this pin is used for input operation, it is enabled as required and must not be used for any other I/P.
1	2	9	P45	F		General-purpose I/O ports.
			SNI2*4			Trigger input pins for position detection of the Multi-pulse generator. When this pin is used for input operation, it is enabled as required and must not be used for any other I/P.
2	3	10	P46	F		General-purpose I/O ports.
			PPG2			Output pins for PPG channel 2. This function is enabled when PPG channel 2 enables output.

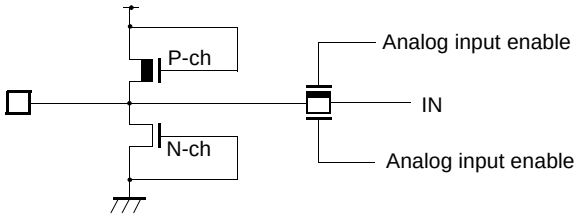
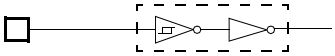
Pin no.			Pin name	I/O circuit	Pin status during reset	Function
LQFP-M09*1	QFP-M06*2	SDIP*3				
3~10	4~11	11~18	P50 ~ P57	I	Analog input	General-purpose I/O ports.
			AN0 ~ AN7			A/D converter analog input pins. This function is enabled when the analog input specification is enabled (ADER).
11	12	19	AVCC	J	Power input	Vcc power input pin for analog circuits.
12	13	20	AVR	K		Vref+ input pin for the A/D converter. This voltage must not exceed AVcc. Vref- is fixed to AVss.
13	14	21	AVSS	J		Vss power input pin for analog circuits.
14	15	22	P60	F	Port Input	General-purpose I/O ports.
			SIN1			Serial data input pin for UART channel 1. While UART channel 1 is operating for input, the input of this pin is used as required and must not be used for any other input.
15	16	23	P61	F		General-purpose I/O ports.
			SOT1			Serial data output pin for UART channel 1. This function is enabled when UART channel 1 enables data output.
16	17	24	P62	F		General-purpose I/O port.
			SCK1			Serial clock I/O pin for UART channel 1. This function is enabled when UART channel 1 enables clock output.
17	18	25	P63	F		General-purpose I/O port.
			INT7			Usable as interrupt request input channel 7. Input is enabled when 1 is set in EN7 in standby mode.
18	19	26	MD0	L	Mode input	Input pin for operation mode specification. Connect this pin directly to Vcc or Vss.
20,21	21,22	28,29	MD1,MD2	L		Input pin for operation mode specification. Connect this pin directly to Vcc or Vss.
24,49	25,50	32,57	Vss	–	Power input	Power (0 V) input pin.
56	57	64	Vcc	–		Power (5 V) input pin.

*1: FPT-64P-M09
*2: FPT-64P-M06
*3: DIP-64P-M01
*4: Pin names not applicable to MB90465 series

■ I/O CIRCUIT TYPE

Classification	Type	Remarks
A		Main clock (main clock crystal oscillator) • At an oscillation feedback resistor of approximately 1 MΩ
B		• Hysteresis input • Resistor approximately 50 kΩ
C		• CMOS output • Hysteresis input • Selectable pull-up resistor approximately 50 kΩ • I_{OL} = 4 mA
D		• CMOS output • CMOS input • Selectable pull-up resistor approximately 50 kΩ • I_{OL} = 12 mA
E		• CMOS output • CMOS input • Selectable pull-up resistor approximately 50 kΩ • I_{OL} = 4 mA

Classification	Type	Remarks
F		• CMOS output • Hysteresis input • I_{OL} = 4 mA
G		• CMOS output • CMOS input • I_{OL} = 12 mA
H		• CMOS output • CMOS input • I_{OL} = 4 mA
I		• CMOS output • CMOS input • Analog input • I_{OL} = 4 mA
J		• Power supply input protection circuit

Classification	Type	Remarks
K		• A/D converter reference voltage (AVR) input pin with protection circuit
L		• Hysteresis input

■ HANDLING DEVICES

1. Preventing latch-up

CMOS ICs may cause latch-up in the following situations:

- When a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins.
- When a voltage exceeding the rating is applied between V_{CC} and V_{SS}.
- When AV_{CC} power is supplied prior to the V_{CC} voltage.

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let it occur.

For the same reason, also be careful not to let the analog power-supply voltage exceed the digital power-supply voltage.

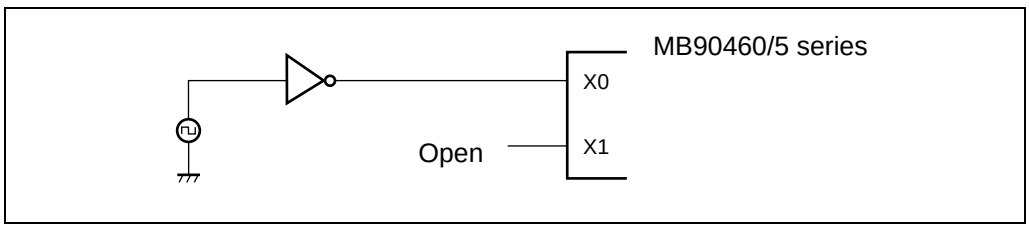
2. Handling unused input pins

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

3. Use of the external clock

When the device uses an external clock, drive only the X0 pin while leaving the X1 pin open (See the illustration below).



4. Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pin near the device.

5. Crystal oscillator circuit

Noise around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with an ground area for stabilizing the operation.

6. Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AV_{SS}, AVR) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage of AVR dose not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

7. Connection of unused pins of A/D converter

Connect unused pin of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$.

8. N.C. pin

The N.C. (internally connected) pin must be opened for use.

9. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more.

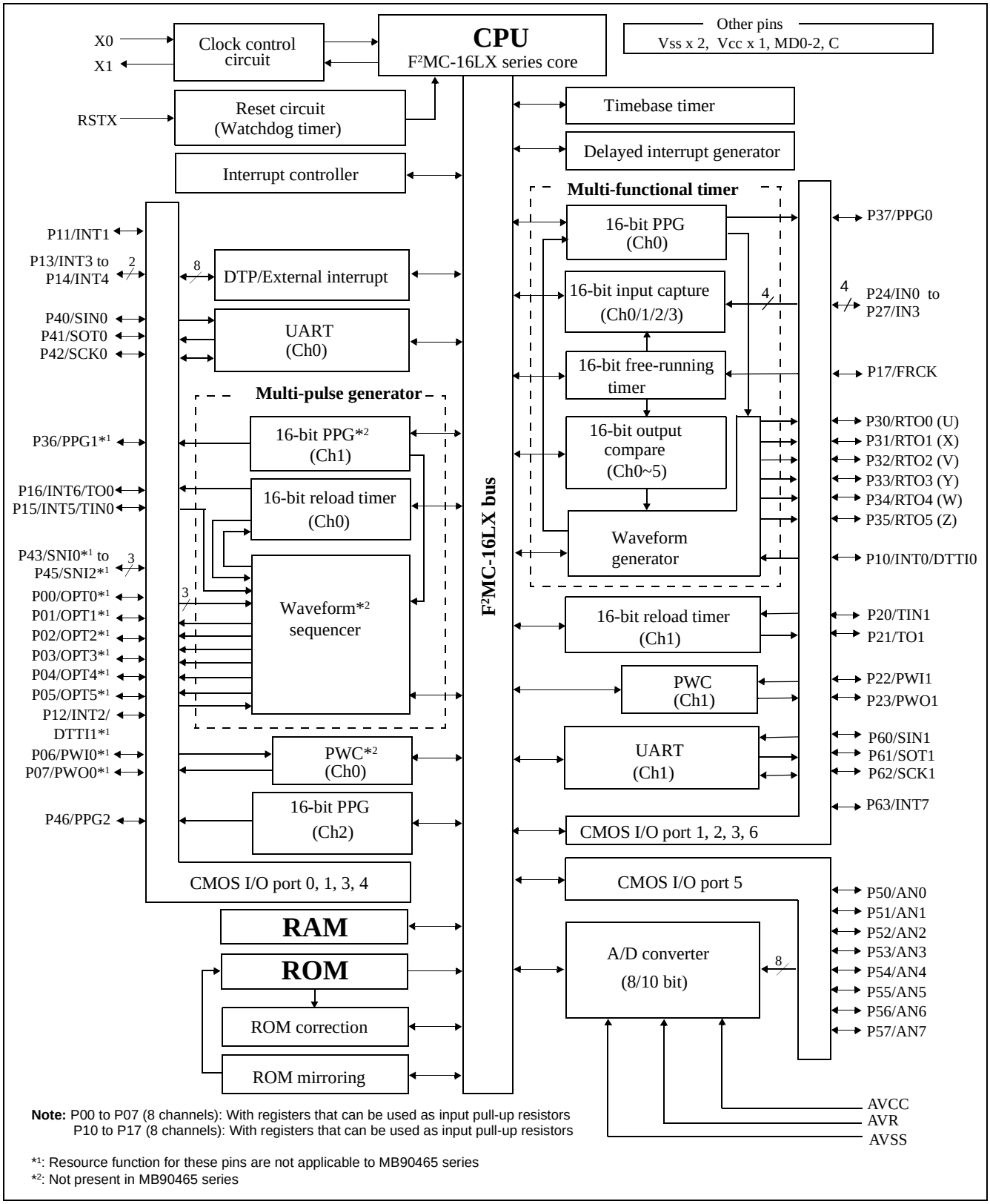
10. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers turning on the power again.

11. Return from standby state

If the power supply voltage goes below the standby RAM holding voltage in the standby state, the device may fail to return from the standby state. In this case, reset the device via the external reset pin to return to the normal state.

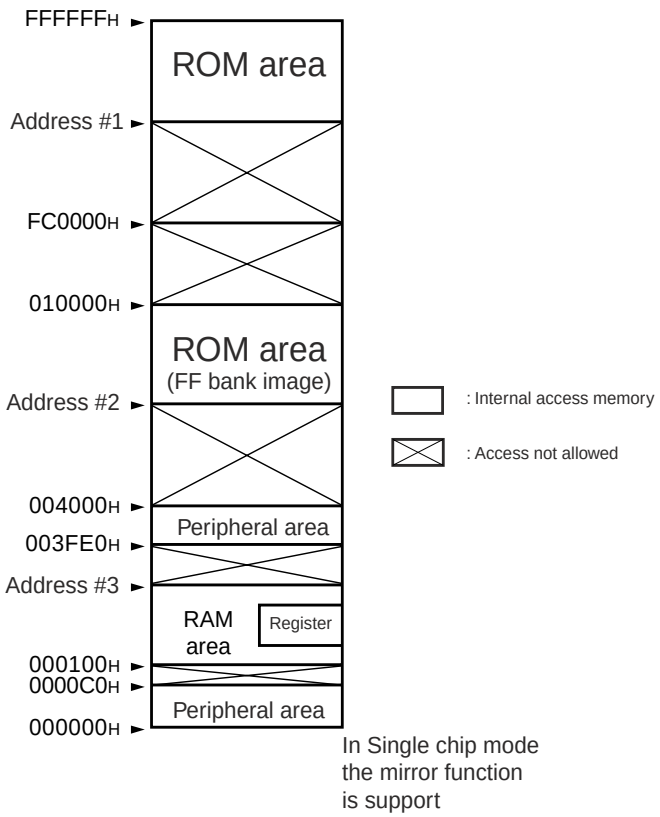
■ BLOCK DIAGRAM



Note: P00 to P07 (8 channels): With registers that can be used as input pull-up resistors
P10 to P17 (8 channels): With registers that can be used as input pull-up resistors

*1: Resource function for these pins are not applicable to MB90465 series
*2: Not present in MB90465 series

■ MEMORY MAP

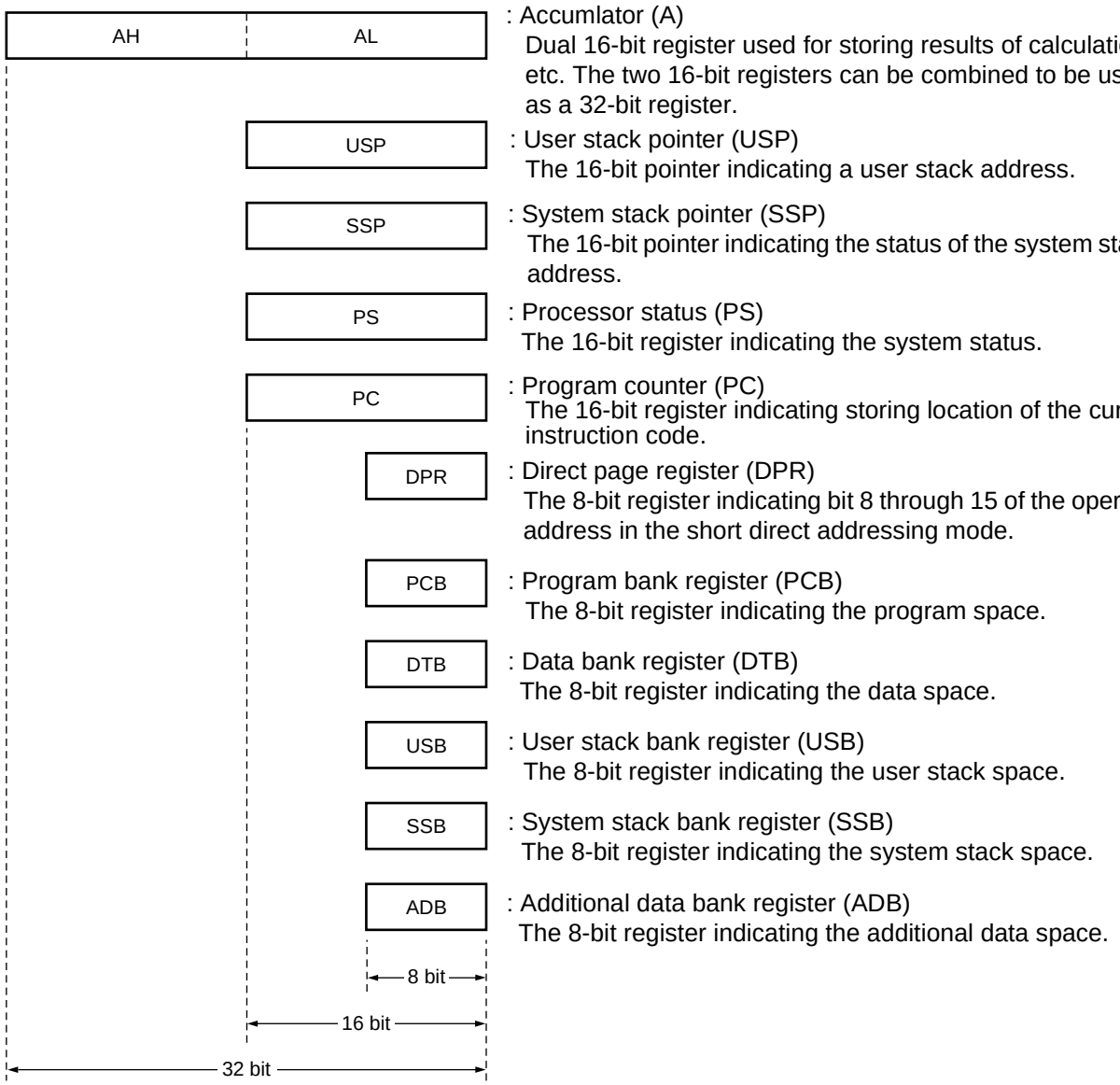


Parts no.	Address#1	Address#2	Address#3
MB90462	FF0000H	004000H	000900H
MB90467	FF0000H	004000H	000900H
MB90F462	FF0000H	004000H	000900H
MB90F462A	FF0000H	004000H	000900H
MB90F463A	FE0000H	004000H	000900H
MB90V460	(FF0000H)	004000H	002100H

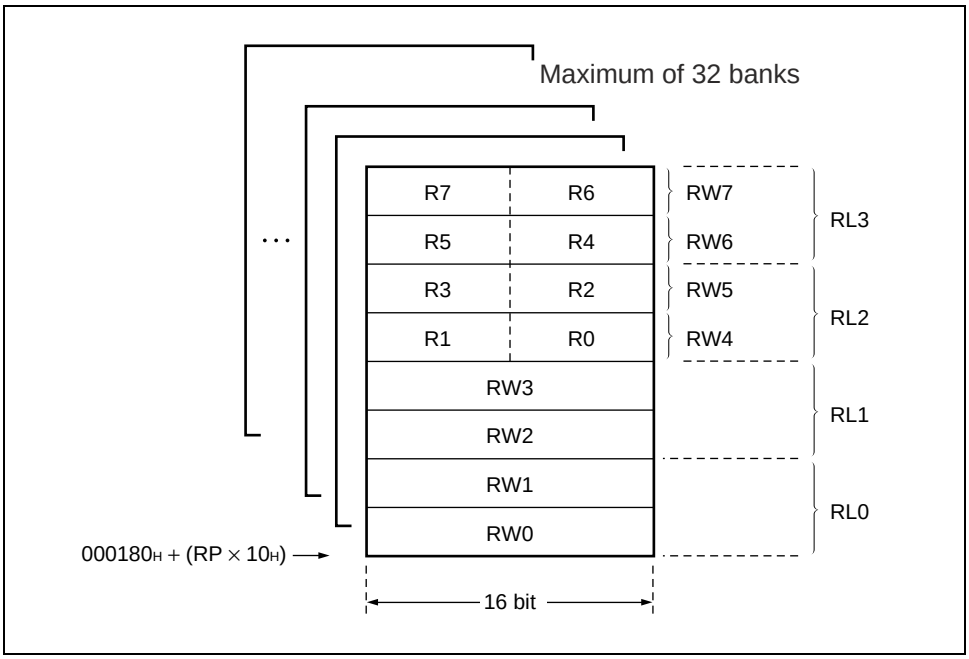
Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit is assigned to the same address, enabling reference of the table on the ROM without stating “far”. For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed actually. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

■ F²MC-16LX CPU PROGRAMMING MODEL

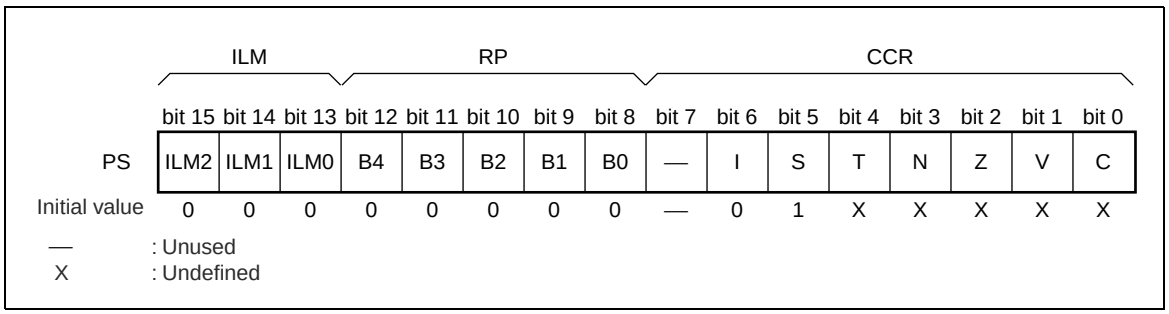
- Dedicated registers



- General-purpose registers



- Processor status (PS)



■ I/O MAP

MB90460/5 series I/O map

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000000H	PDR0	Port 0 data register	R/W	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	R/W	Port 4	-XXXXXXXB
000005H	PDR5	Port 5 data register	R/W	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	R/W	Port 6	----XXXXB
000007H	Prohibited area					
000008H	PWCSL0	PWC control status register CH0	R/W	R/W	PWC timer (CH0)*	00000000B
000009H	PWCSH0		R/W	R/W		00000000B
00000AH	PWC0	PWC data buffer register CH0	-	R/W		XXXXXXXXB
00000BH						XXXXXXXXB
00000CH	DIV0	Divide ratio control register CH0	R/W	R/W		------00B
00000DH ~ 0FH	Prohibited area					
000010H	DDR0	Port 0 direction register	R/W	R/W	Port 0	00000000B
000011H	DDR1	Port 1 direction register	R/W	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction register	R/W	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction register	R/W	R/W	Port 3	00000000B
000014H	DDR4	Port 4 direction register	R/W	R/W	Port 4	-0000000B
000015H	DDR5	Port 5 direction register	R/W	R/W	Port 5	00000000B
000016H	DDR6	Port 6 direction register	R/W	R/W	Port 6	----0000B
000017H	ADER	Analog input enable register	R/W	R/W	Port 5, A/D	11111111B
000018H	Prohibited area					
000019H	CDCR0	Clock division control register 0	R/W	R/W	Communication prescaler 0	0---0000B
00001AH	Prohibited area					
00001BH	CDCR1	Clock division control register 1	R/W	R/W	Communication prescaler 1	0---0000B
00001CH	RDR0	Port 0 pull-up resistor setting register	R/W	R/W	Port 0	00000000B
00001DH	RDR1	Port 1 pull-up resistor setting register	R/W	R/W	Port 1	00000000B
00001EH ~ 1FH	Prohibited area					
000020H	SMR0	Serial mode register 0	R/W	R/W	UART0	00000000B
000021H	SCR0	Serial control register 0	R/W	R/W		00000100B
000022H	SIDR0 / SODR0	Input data register 0 / Output data register 0	R/W	R/W		XXXXXXXXB
000023H	SSR0	Serial status register 0	R/W	R/W		00001000B
000024H	SMR1	Serial mode register 1	R/W	R/W	UART1	00000000B
000025H	SCR1	Serial control register 1	R/W	R/W		00000100B
000026H	SIDR1 / SODR1	Input data register 1 / Output data register 1	R/W	R/W		XXXXXXXXB
000027H	SSR1	Status register 1	R/W	R/W		00001000B

MB90460/5 series I/O map

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000028H	PWCSL1	PWC control status register CH1	R/W	R/W	PWC timer (CH1)	00000000B
000029H	PWCSH1		R/W	R/W		00000000B
00002AH	PWC1	PWC data buffer register CH1	-	R/W		XXXXXXXXB
00002BH						XXXXXXXXB
00002CH	DIV1	Divide ratio control register CH1	R/W	R/W		------00B
00002DH ~ 2FH	Prohibited area					
000030H	ENIR	Interrupt / DTP enable register	R/W	R/W	DTP/external interrupt	00000000B
000031H	EIRR	Interrupt / DTP cause register	R/W	R/W		XXXXXXXXB
000032H	ELVRL	Request level setting register (lower byte)	R/W	R/W		00000000B
000033H	ELVRH	Request level setting register (higher byte)	R/W	R/W		00000000B
000034H	ADCS0	A/D control status register 0	R/W	R/W	8/10-bit A/D converter	00000000B
000035H	ADCS1	A/D control status register 1	R/W	R/W		00000000B
000036H	ADCR0	A/D data register 0	R	R		XXXXXXXXB
000037H	ADCR1	A/D data register 1	R/W	R/W		00000-XXB
000038H	PDCR0	PPG0 down counter register	-	R	16-bit PPG timer (CH0)	11111111B
000039H						11111111B
00003AH	PCSR0	PPG0 period setting register	-	W		XXXXXXXXB
00003BH						XXXXXXXXB
00003CH	PDUT0	PPG0 duty setting register	-	W		XXXXXXXXB
00003DH						XXXXXXXXB
00003EH	PCNTL0	PPG0 control status register	R/W	R/W		--000000B
00003FH	PCNTH0		R/W	R/W		00000000B
000040H	PDCR1	PPG1 down counter register	-	R	16-bit PPG timer (CH1)*	11111111B
000041H						11111111B
000042H	PCSR1	PPG1 period setting register	-	W		XXXXXXXXB
000043H						XXXXXXXXB
000044H	PDUT1	PPG1 duty setting register	-	W		XXXXXXXXB
000045H						XXXXXXXXB
000046H	PCNTL1	PPG1 control status register	R/W	R/W		--000000B
000047H	PCNTH1		R/W	R/W		00000000B
000048H	PDCR2	PPG2 down counter register	-	R	16-bit PPG timer (CH2)	11111111B
000049H						11111111B
00004AH	PCSR2	PPG2 period setting register	-	W		XXXXXXXXB
00004BH						XXXXXXXXB
00004CH	PDUT2	PPG2 duty setting register	-	W		XXXXXXXXB
00004DH						XXXXXXXXB
00004EH	PCNTL2	PPG2 control status register	R/W	R/W		--000000B
00004FH	PCNTH2		R/W	R/W		00000000B

MB90460/5 series I/O map

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000050H	TMRR0	16-bit timer register 0	-	R/W	Waveform generator	XXXXXXXXB
000051H						XXXXXXXXB
000052H	TMRR1	16-bit timer register 1	-	R/W		XXXXXXXXB
000053H						XXXXXXXXB
000054H	TMRR2	16-bit timer register 2	-	R/W		XXXXXXXXB
000055H						XXXXXXXXB
000056H	DTCR0	16-bit timer control register 0	R/W	R/W		00000000B
000057H	DTCR1	16-bit timer control register 1	R/W	R/W		00000000B
000058H	DTCR2	16-bit timer control register 2	R/W	R/W		00000000B
000059H	SIGCR	Waveform control register	R/W	R/W		00000000B
00005AH	CPCLRB / CPCLR	Compare clear buffer register / Compare clear register (lower)	-	R/W	16-bit free-running timer	11111111B
00005BH						11111111B
00005CH	TCDT	Timer data register (lower)	-	R/W		00000000B
00005DH						00000000B
00005EH	TCCSL	Timer control status register (lower)	R/W	R/W		00000000B
00005FH	TCCSH	Timer control status register (upper)	R/W	R/W		-0000000B
000060H	IPCP0	Input capture data register CH0	-	R	16-bit input capture (CH0 ~ CH3)	XXXXXXXXB
000061H						XXXXXXXXB
000062H	IPCP1	Input capture data register CH1	-	R		XXXXXXXXB
000063H						XXXXXXXXB
000064H	IPCP2	Input capture data register CH2	-	R		XXXXXXXXB
000065H						XXXXXXXXB
000066H	IPCP3	Input capture data register CH3	-	R		XXXXXXXXB
000067H						XXXXXXXXB
000068H	PICSL01	Input capture control status register 01 (lower)	R/W	R/W		00000000B
000069H	PICSH01	PPG output control / Input capture control status register 01 (upper)	R/W	R/W		00000000B
00006AH	ICSL23	Input capture control status register 23 (lower)	R/W	R/W		00000000B
00006BH	ICSH23	Input capture control status register 23 (upper)	R	R		------00B
00006CH ~ 6EH	Prohibited area					
00006FH	ROMM	ROM mirroring function selection register	W	W	ROM mirroring function	-------1B

MB90460/5 series I/O map

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000070H	OCCPB0 / OCCP0	Output compare buffer register / Output compare register 0	-	R/W	Output compare (CH0 ~ CH5)	XXXXXXXXB
000071H						XXXXXXXXB
000072H	OCCPB1 / OCCP1	Output compare buffer register / Output compare register 1	-	R/W		XXXXXXXXB
000073H						XXXXXXXXB
000074H	OCCPB2 / OCCP2	Output compare buffer register / Output compare register 2	-	R/W		XXXXXXXXB
000075H						XXXXXXXXB
000076H	OCCPB3 / OCCP3	Output compare buffer register / Output compare register 3	-	R/W		XXXXXXXXB
000077H						XXXXXXXXB
000078H	OCCPB4 / OCCP4	Output compare buffer register / Output compare register 4	-	R/W		XXXXXXXXB
000079H						XXXXXXXXB
00007AH	OCCPB5 / OCCP5	Output compare buffer register / Output compare register 5	-	R/W		XXXXXXXXB
00007BH						XXXXXXXXB
00007CH	OCS0	Compare control register 0	R/W	R/W		00000000B
00007DH	OCS1	Compare control register 1	R/W	R/W		-0000000B
00007EH	OCS2	Compare control register 2	R/W	R/W		00000000B
00007FH	OCS3	Compare control register 3	R/W	R/W		-0000000B
000080H	OCS4	Compare control register 4	R/W	R/W		00000000B
000081H	OCS5	Compare control register 5	R/W	R/W		-0000000B
000082H	TMCSRL0	Timer control status register CH0 (lower)	R/W	R/W	16-bit reload timer (CH0)	00000000B
000083H	TMCSRH0	Timer control status register CH0 (upper)	R/W	R/W		----0000B
000084H	TMR0 / TMRD0	16 bit timer register CH0 / 16-bit reload register CH0	-	R/W		XXXXXXXXB
000085H						XXXXXXXXB
000086H	TMCSRL1	Timer control status register CH1 (lower)	R/W	R/W	16-bit reload timer (CH1)	00000000B
000087H	TMCSRH1	Timer control status register CH1 (upper)	R/W	R/W		----0000B
000088H	TMR1 / TMRD1	16 bit timer register CH1 / 16-bit reload register CH1	-	R/W		XXXXXXXXB
000089H						XXXXXXXXB
00008AH	OPCLR	Output control lower register	R/W	R/W	Waveform sequencer*	00000000B
00008BH	OPCUR	Output control upper register	R/W	R/W		00000000B
00008CH	IPCLR	Input control lower register	R/W	R/W		00000000B
00008DH	IPCUR	Input control upper register	R/W	R/W		00000000B
00008EH	TCSR	Timer control status register	R/W	R/W		00000000B
00008FH	NCCR	Noise cancellation control register	R/W	R/W		00000000B
000090H ~ 9DH	Prohibited area					
00009EH	PACSR	Program address detect control status register	R/W	R/W	Address match detection	00000000B
00009FH	DIRR	Delayed interrupt cause / clear register	R/W	R/W	Delayed interrupt	-------0B
0000A0H	LPMCR	Low-power consumption mode register	R/W	R/W	Low-power consumption control register	00011000B
0000A1H	CKSCR	Clock selection register	R/W	R/W		11111100B
0000A2H ~ A7H	Prohibited area					
0000A8H	WDTC	Watchdog control register	R/W	R/W	Watchdog timer	X-XXX111B
0000A9H	TBTC	Timebase timer control register	R/W	R/W	Timebase timer	1--00100B

MB90460/5 series I/O map

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000AA$_H$ ~ AD$_H$	Prohibited area					
0000AE$_H$	FMCS	Flash memory control status register	R/W	R/W	Flash memory interface circuit	00010000$_B$
0000AF$_H$	Prohibited area					
0000B0$_H$	ICR00	Interrupt control register 00	R/W	R/W	Interrupt controller	00000111$_B$
0000B1$_H$	ICR01	Interrupt control register 01	R/W	R/W		00000111$_B$
0000B2$_H$	ICR02	Interrupt control register 02	R/W	R/W		00000111$_B$
0000B3$_H$	ICR03	Interrupt control register 03	R/W	R/W		00000111$_B$
0000B4$_H$	ICR04	Interrupt control register 04	R/W	R/W		00000111$_B$
0000B5$_H$	ICR05	Interrupt control register 05	R/W	R/W		00000111$_B$
0000B6$_H$	ICR06	Interrupt control register 06	R/W	R/W		00000111$_B$
0000B7$_H$	ICR07	Interrupt control register 07	R/W	R/W		00000111$_B$
0000B8$_H$	ICR08	Interrupt control register 08	R/W	R/W		00000111$_B$
0000B9$_H$	ICR09	Interrupt control register 09	R/W	R/W		00000111$_B$
0000BA$_H$	ICR10	Interrupt control register 10	R/W	R/W		00000111$_B$
0000BB$_H$	ICR11	Interrupt control register 11	R/W	R/W		00000111$_B$
0000BC$_H$	ICR12	Interrupt control register 12	R/W	R/W		00000111$_B$
0000BD$_H$	ICR13	Interrupt control register 13	R/W	R/W		00000111$_B$
0000BE$_H$	ICR14	Interrupt control register 14	R/W	R/W		00000111$_B$
0000BF$_H$	ICR15	Interrupt control register 15	R/W	R/W		00000111$_B$
0000C0$_H$ ~ FF$_H$	External area					
001FF0$_H$	PADRL0	Program address detection register 0 (lower byte)	R/W	R/W	Address match detection	XXXXXXXX$_B$
001FF1$_H$	PADRM0	Program address detection register 0 (middle byte)	R/W	R/W		XXXXXXXX$_B$
001FF2$_H$	PADRH0	Program address detection register 0 (higher byte)	R/W	R/W		XXXXXXXX$_B$
001FF3$_H$	PADRL1	Program address detection register 1 (lower byte)	R/W	R/W		XXXXXXXX$_B$
001FF4$_H$	PADRM1	Program address detection register 1 (middle byte)	R/W	R/W		XXXXXXXX$_B$
001FF5$_H$	PADRH1	Program address detection register 1 (higher byte)	R/W	R/W		XXXXXXXX$_B$

MB90460/5 series I/O map

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
003FE0H	OPDBR0	Output data buffer register 0	-	R/W	Waveform sequencer*	00000000B
003FE1H						00000000B
003FE2H	OPDBR1	Output data buffer register 1	-	R/W		00000000B
003FE3H						00000000B
003FE4H	OPDBR2	Output data buffer register 2	-	R/W		00000000B
003FE5H						00000000B
003FE6H	OPDBR3	Output data buffer register 3	-	R/W		00000000B
003FE7H						00000000B
003F78H	OPDBR4	Output data buffer register 4	-	R/W		00000000B
003FE9H						00000000B
003FEAH	OPDBR5	Output data buffer register 5	-	R/W		00000000B
003FEBH						00000000B
003FECH	OPEBR6	Output data buffer register 6	-	R/W		00000000B
003FEDH						00000000B
003FEEH	OPEBR7	Output data buffer register 7	-	R/W		00000000B
003FEFH						00000000B
003FF0H	OPEBR8	Output data buffer register 8	-	R/W		00000000B
003FF1H						00000000B
003FF2H	OPEBR9	Output data buffer register 9	-	R/W		00000000B
003FF3H						00000000B
003FF4H	OPEBRA	Output data buffer register A	-	R/W		00000000B
003FF5H						00000000B
003FF6H	OPEBRB	Output data buffer register B	-	R/W		00000000B
003FF7H						00000000B
003FF8H	OPDR	Output data register	-	R		XXXXXXXXB
003FF9H						0000XXXXB
003FFAH	CPCR	Compare clear register	-	R/W		XXXXXXXXB
003FFBH						XXXXXXXXB
003FFCH	TMBR	Timer buffer register	-	R		00000000B
003FFDH						00000000B
003FFEH ~ 003FFFH	Prohibited area					

- Meaning of abbreviations used for reading and writing
  R/W : Read and write enabled
  R : Read-only
  W : Write-only
- Explanation of initial values
  0 : The bit is initialized to 0.
  1 : The bit is initialized to 1.
  X : The initial value of the bit is undefined.
  - : The bit is not used. Its initial value is undefined.
- Instruction using IO addressing e.g. MOV A, io, is not supported for registers area $003FE0_H$ to $003FFF_H$.

Note: For bits that is initialized by an reset operation, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results.
For LPMCR/CKSCR/WDTC, there are cases where initialization is performed or not performed, depending on the types of the reset. However initial value for resets that initializes the value are listed.

*: These registers are not present in MB90465 series

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS support	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
Reset	X	#08	08H	FFFFDCH	-	-	High
INT9 instruction	X	#09	09H	FFFFD8H	-	-	
Exception processing	X	#10	0AH	FFFFD4H	-	-	
A/D converter conversion termination	O	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
Output compare channel 0 match	O	#12	0CH	FFFFCCH			
End of measurement by PWC timer 0 / PWC timer 0 overflow*	O	#13	0DH	FFFFC8H	ICR01	0000B1H*1	
16-bit PPG timer 0	O	#14	0EH	FFFFC4H			
Output compare channel 1 match	O	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
16-bit PPG timer 1*	O	#16	10H	FFFFBCH			
Output compare channel 2 match	O	#17	11H	FFFFB8H	ICR03	0000B3H*1	
16-bit reload timer 1 underflow	O	#18	12H	FFFFB4H			
Output compare channel 3 match	O	#19	13H	FFFFB0H	ICR04	0000B4H*1	
DTP/ext. interrupt channels 0/1 detection	O	#20	14H	FFFFACH			
DTTI0	Δ						
Output compare channel 4 match	O	#21	15H	FFFFA8H	ICR05	0000B5H*2	
DTP/ext. interrupt channels 2/3 detection	O	#22	16H	FFFFA4H			
DTTI1*	Δ						
Output compare channel 5 match	O	#23	17H	FFFFA0H	ICR06	0000B6H*1	
End of measurement by PWC timer 1 / PWC timer 1 overflow	O	#24	18H	FFFF9CH			
DTP/ext. interrupt channels 4/5 detection	O	#25	19H	FFFF98H	ICR07	0000B7H*1	
Waveform sequencer timer compare match / write timing*	O	#26	1AH	FFFF94H			
DTP/ext. interrupt channels 6/7 detection	O	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Waveform sequencer position detect / compare interrupt*	O	#28	1CH	FFFF8CH			
Waveform generator 16-bit timer 0/1/2 underflow	Δ	#29	1DH	FFFF88H	ICR09	0000B9H*1	
16-bit reload timer 0 underflow	O	#30	1EH	FFFF84H			
16-bit free-running timer zero detect	Δ	#31	1FH	FFFF80H	ICR10	0000BAH*1	
16-bit PPG timer 2	O	#32	20H	FFFF7CH			
Input capture channels 0/1	O	#33	21H	FFFF78H	ICR11	0000BBH*1	
16-bit free-running timer compare clear	Δ	#34	22H	FFFF74H			
Input capture channels 2/3	O	#35	23H	FFFF70H	ICR12	0000BCH*1	
Timebase timer	Δ	#36	24H	FFFF6CH			
UART1 receive	⊙	#37	25H	FFFF68H	ICR13	0000BDH*1	
UART1 send	Δ	#38	26H	FFFF64H			
UART0 receive	⊙	#39	27H	FFFF60H	ICR14	0000BEH*1	
UART0 send	Δ	#40	28H	FFFF5CH			
Flash memory status	Δ	#41	29H	FFFF58H	ICR15	0000BFH*1	
Delayed interrupt generator module	Δ	#42	2AH	FFFF54H			Low

⊙ : Can be used and support the EI²OS stop request.
O : Can be used and interrupt request flag is cleared by EI²OS interrupt clear signal.
X : Cannot be used.
Δ : Usable when an interrupt cause that shares the ICR is not used.
* : In MB90465 series, these resources are not present, therefore, interrupt not available.

■ PERIPHERAL RESOURCES

1. Low-power Consumption Control Circuit

The MB90460 series has the following CPU operating mode configured by selection of an operating clock and clock operation control.

- Clock mode
  PLL clock mode : A PLL clock that is a multiple of the oscillation clock (HCLK) frequency is used to operate the CPU and peripheral functions.
  Main clock mode : The main clock, with a frequency one-half that of the oscillation clock (HCLK), is used to operate the CPU and peripheral functions. In main clock mode, the PLL multiplier circuit is inactive.
- CPU intermittent operation mode
  CPU intermittent operation mode causes the CPU to operate intermittently, while high-speed clock pulses are supplied to peripheral functions, reducing power consumption. In CPU intermittent operation mode, intermittent clock pulses are only applied to the CPU when it is accessing a register, internal memory, a peripheral function, or an external unit.
- Standby mode
  In standby mode, the low power consumption control circuit stops supplying the clock to the CPU (sleep mode) or the CPU and peripheral functions (timebase timer mode), or stops the oscillation clock itself (stop mode), reducing power consumption.
  - PLL sleep mode
    PLL sleep mode is activated to stop the CPU operating clock when the microcontroller enters PLL clock mode; other components continue to operate on the PLL clock.
  - Main sleep mode
    Main sleep mode is activated to stop the CPU operating clock when the microcontroller enters main clock mode; other components continue to operate on the main clock.
  - PLL timebase timer mode
    PLL timebase timer mode causes microcontroller operation, with the exception of the oscillation clock, PLL clock and timebase timer, to stop. All functions other than the timebase timer are deactivated.
  - Main timebase timer mode
    Main timebase timer mode causes microcontroller operation, with the exception of the oscillation clock, main clock and the timebase timer, to stop. All functions other than the timebase timer are deactivated.
  - Stop mode
    Stop mode causes the source oscillation to stop. All functions are deactivated.

(1) Register configuration

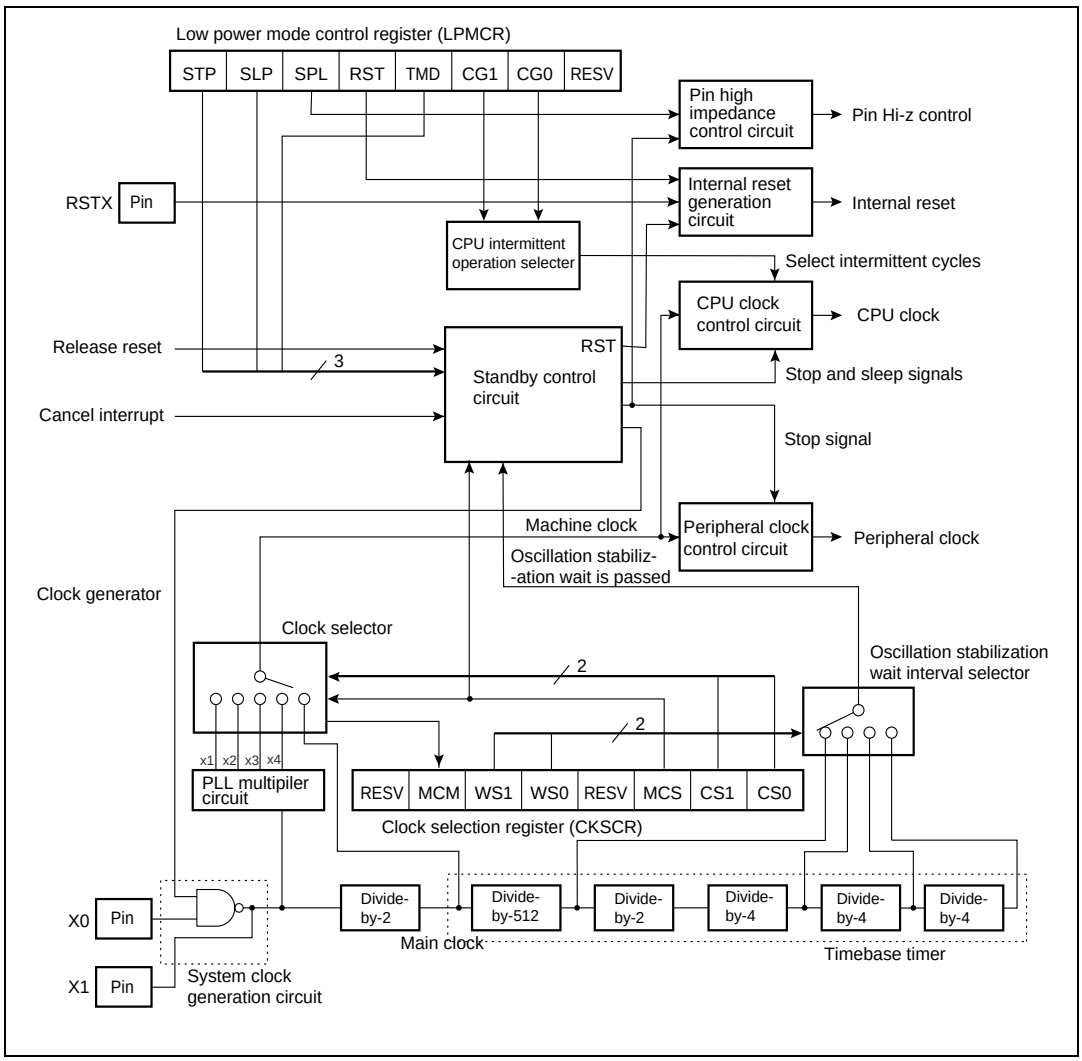
Clock Selection Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00000A1H	Reserved	MCM	WS1	WS0	Reserved	MCS	CS1	CS0	CKSCR
Read/write ⇨	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	0	0	

Low-power Consumption Mode Control Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 0000A0H	STP	SLP	SPL	RST	TMDX	CG1	CG0	Reserved	LPMCR
Read/write ⇨	W	W	R/W	W	W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	1	1	0	0	0	

(2) Block diagram



2. I/O Ports

(1) Outline of I/O ports

When a data register serving for control output is read, the data output from it as a control output is read regardless of the value in the direction register. Note that, if a read-modify-write instruction (such as a bit set instruction) is used to preset output data in the data register when changing its setting from input to output, the data read is not the data register latched value but the input data from the pin. Also note that, for port (other than Port 0, 1, 2 and 3) that is multiplexed with resource, use read-modify-write instruction may accidentally write unexpected value to the DDR and PDR register when resource is enabled.

Ports 0 to 4 and Port 6 are input/output ports which serve as inputs when the direction register value is “0” or as outputs when the value is “1”. Port 5 are input/output ports as other port when ADER is 00_H.

(2) Register configuration

Port 0 Data Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 000000_H	P07	P06	P05	P04	P03	P02	P01	P00	PDR0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Port 1 Data Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 000001_H	P17	P16	P15	P14	P13	P12	P11	P10	PDR1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Port 2 Data Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 000002_H	P27	P26	P25	P24	P23	P22	P21	P20	PDR2
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Port 3 Data Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 000003_H	P37	P36	P35	P34	P33	P32	P31	P30	PDR3
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Port 4 Data Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 000004_H	—	P46	P45	P44	P43	P42	P41	P40	PDR4
Read/write ⇨	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	—	X	X	X	X	X	X	X	

Port 5 Data Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 000005_H	P57	P56	P55	P54	P53	P52	P51	P50	PDR5
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Port 6 Data Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 000006_H	—	—	—	—	P63	P62	P61	P60	PDR6
Read/write ⇨	—	—	—	—	R/W	R/W	R/W	R/W	
Initial value ⇨	—	—	—	—	X	X	X	X	

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Port 0 Direction Register

Bit number	7	6	5	4	3	2	1	0
Address: 000010H	D07	D06	D05	D04	D03	D02	D01	D00
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DDR0

Port 1 Direction Register

Bit number	15	14	13	12	11	10	9	8
Address: 000011H	D17	D16	D15	D14	D13	D12	D11	D10
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DDR1

Port 2 Direction Register

Bit number	7	6	5	4	3	2	1	0
Address: 000012H	D27	D26	D25	D24	D23	D22	D21	D20
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DDR2

Port 3 Direction Register

Bit number	15	14	13	12	11	10	9	8
Address: 000013H	D37	D36	D35	D34	D33	D32	D31	D30
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DDR3

Port 4 Direction Register

Bit number	7	6	5	4	3	2	1	0
Address: 000014H	—	D46	D45	D44	D43	D42	D41	D40
Read/write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	—	X	X	X	X	X	X	X

DDR4

Port 5 Direction Register

Bit number	15	14	13	12	11	10	9	8
Address: 000015H	D57	D56	D55	D54	D53	D52	D51	D50
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DDR5

Port 6 Direction Register

Bit number	7	6	5	4	3	2	1	0
Address: 000016H	—	—	—	—	D63	D62	D61	D60
Read/write	—	—	—	—	R/W	R/W	R/W	R/W
Initial value	—	—	—	—	0	0	0	0

DDR6

Port 5 Analog Input Enable Register

Bit number	15	14	13	12	11	10	9	8
Address: 000017H	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

ADER

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Port 0 Pull-up Resistor Setting Register

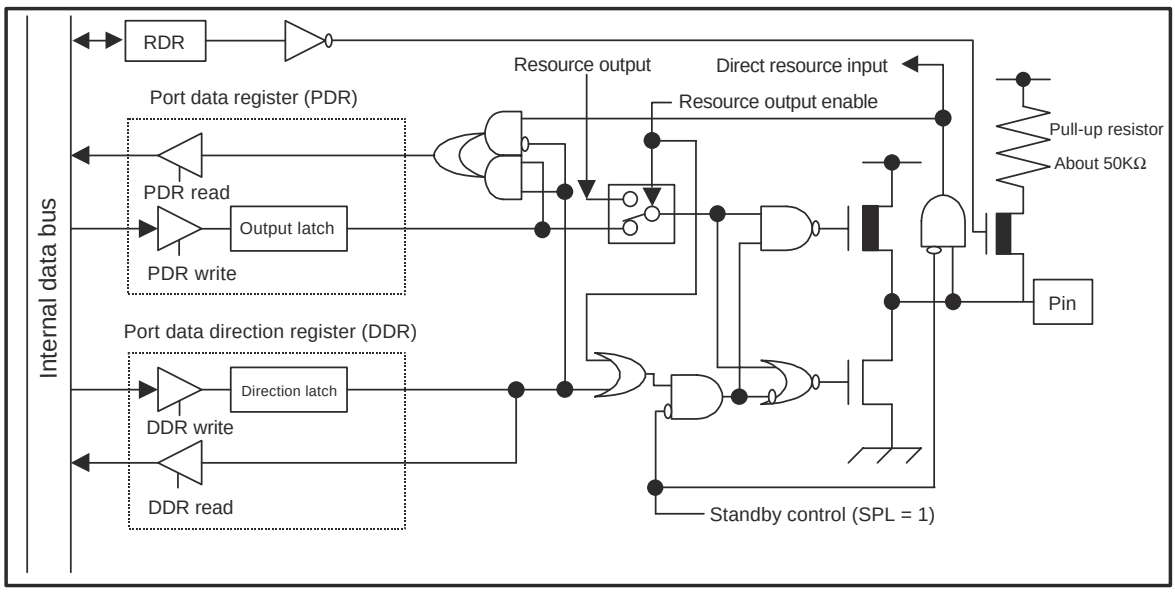
	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00001C$_H$	RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	RDR0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Port 1 Pull-up Resistor Setting Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00001D$_H$	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RDR1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

(3) Block diagram

- Block diagram of Port 0 pins



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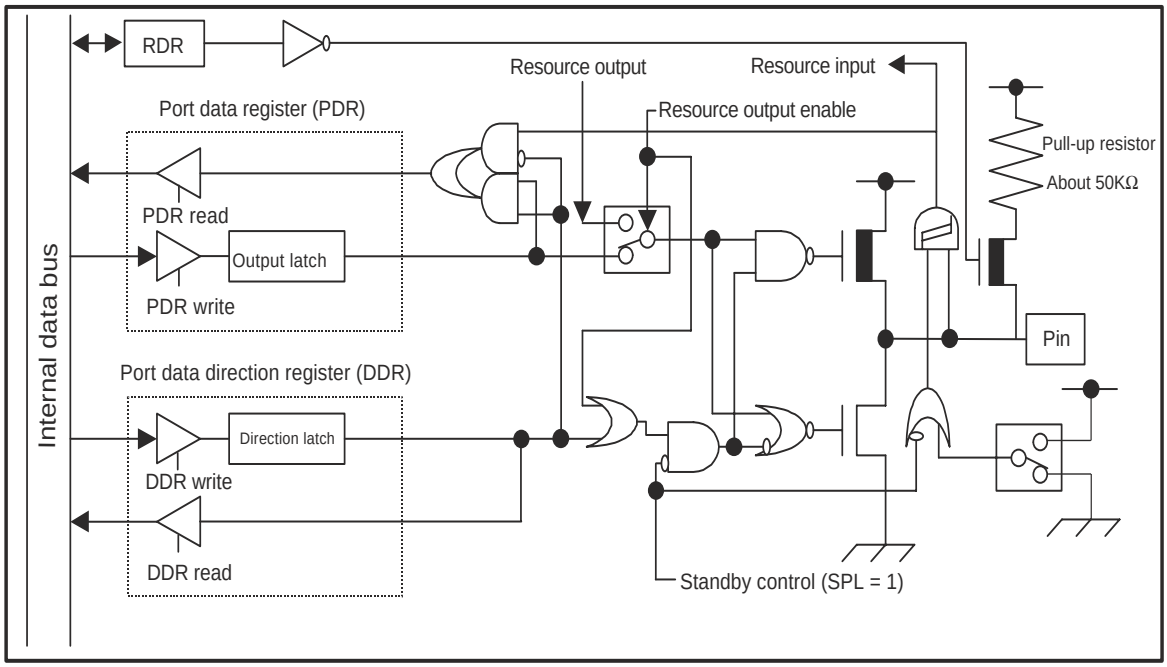
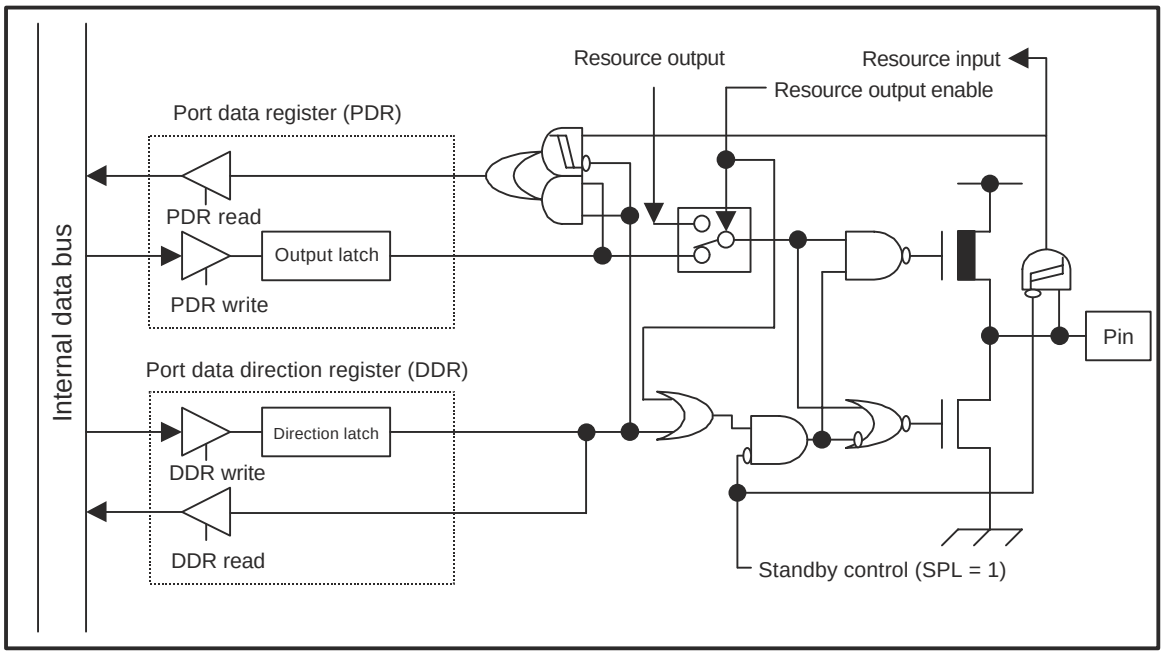
- Block diagram of Port 1 pins



- Block diagram of Port 2 pins



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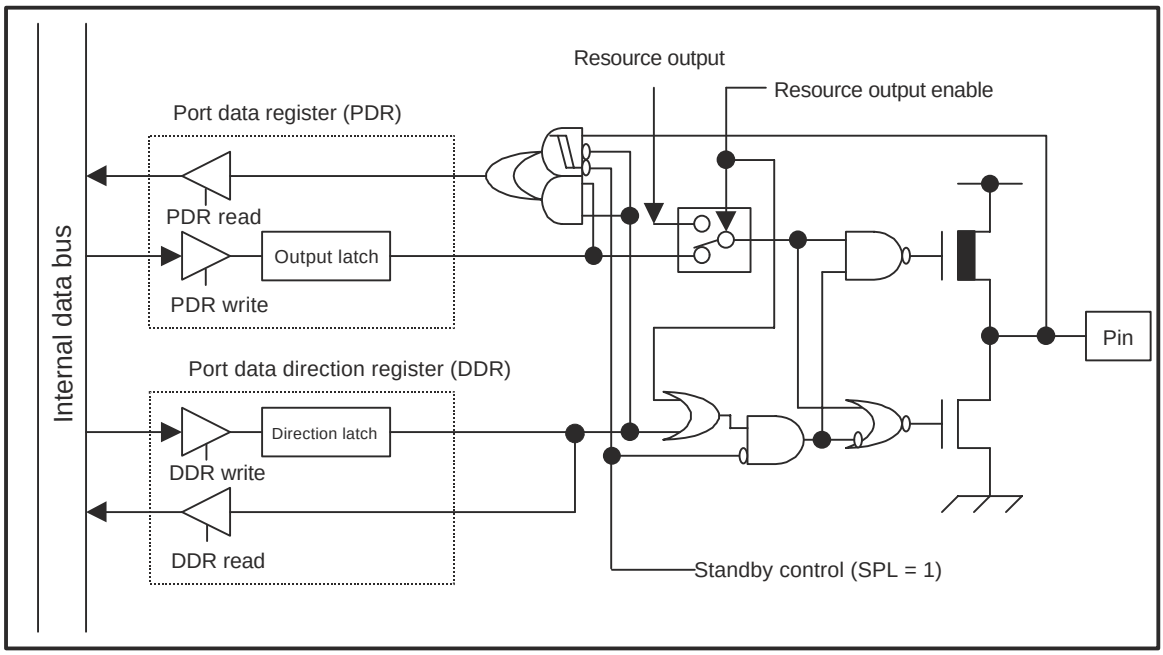
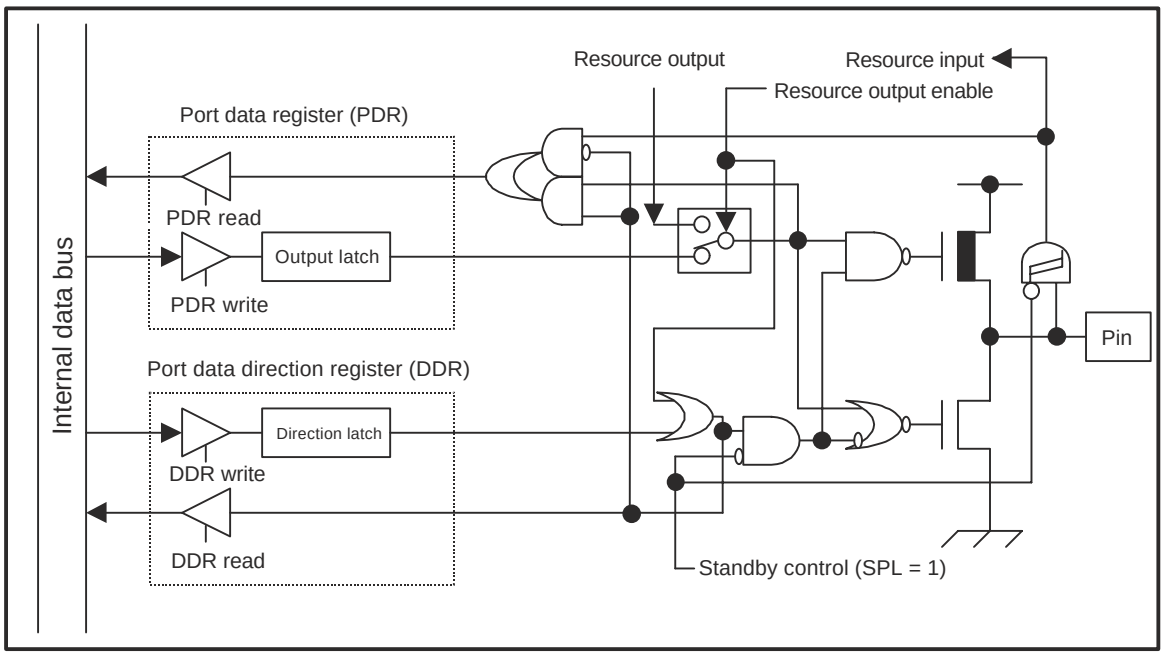
- Block diagram of Port 3 pins



- Block diagram of Port 4 pins



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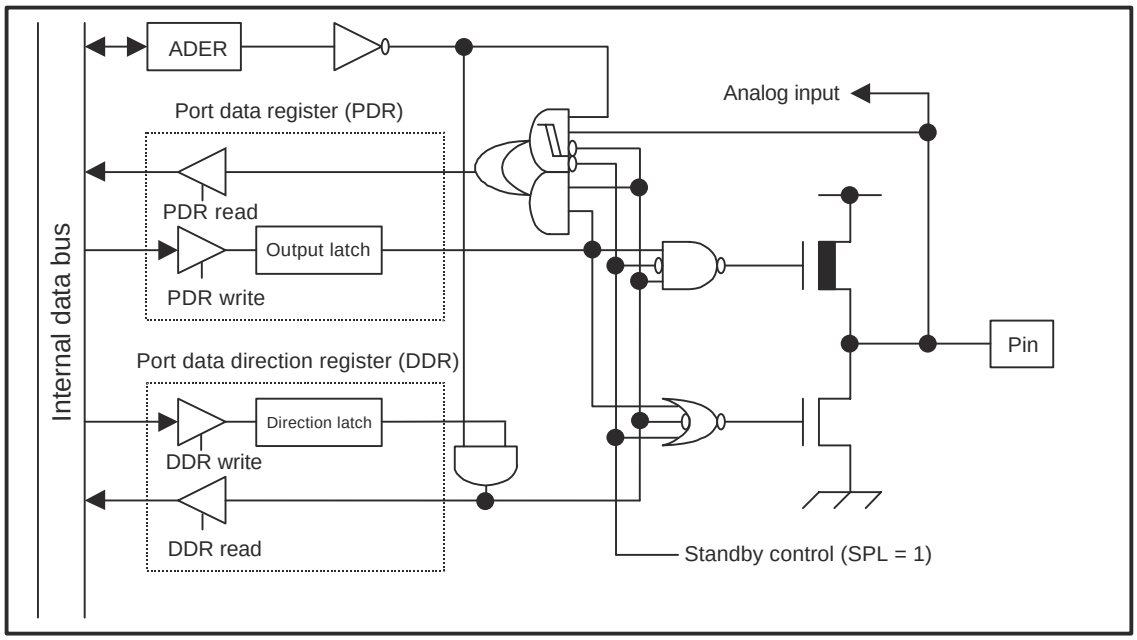
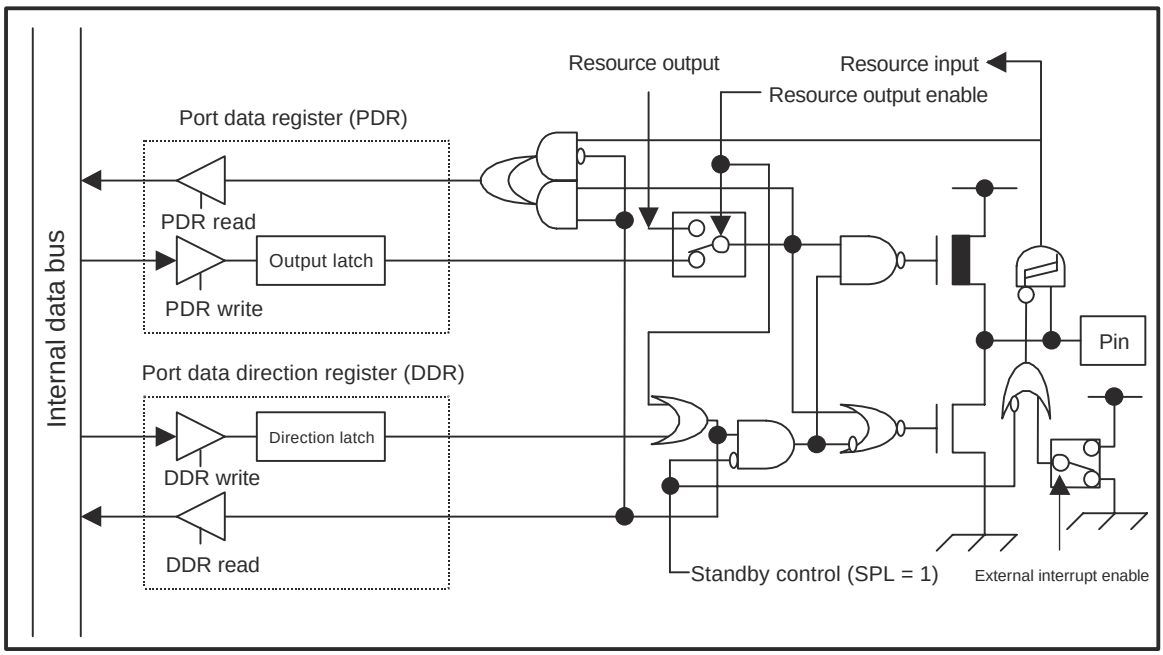
- Block diagram of Port 5 pins



- Block diagram of Port 6 pins



3. Timebase Timer

The timebase timer is an 18-bit free-running counter (timebase counter) that counts up in synchronization with the internal count clock (one-half of the source oscillation).

Features of timebase timer :

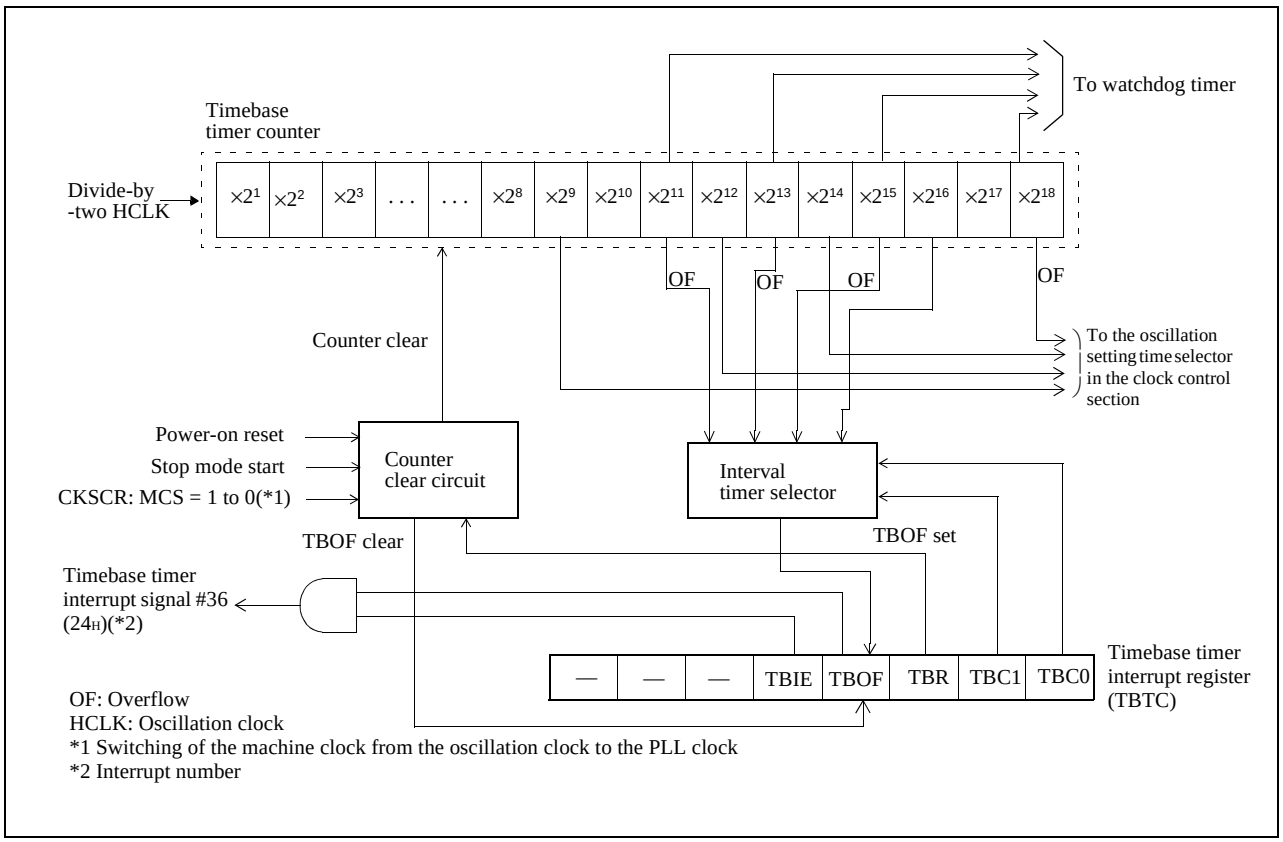
- Interrupt generated when counter overflow
- EI²OS supported
- Interval timer function:
  An interrupt generated at four different time intervals
- Clock supply function:
  Four different clock can be selected as watchdog timer's count clock
  Supply clock for oscillation stabilization

(1) Register configuration

Timebase Timer Control Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 0000A9H	Reserved	——	——	TBIE	TBOF	TBR	TBC1	TBC0	TBTC
Read/write ⇨	R/W	——	——	R/W	R/W	W	R/W	R/W	
Initial value ⇨	1	——	——	0	0	1	0	0	

(2) Block diagram



4. Watchdog Timer

The watchdog timer is a 2-bit counter that uses the timebase timer's supply clock as the count clock. After activation, if the watchdog timer is not cleared within a given period, the CPU will be reset.

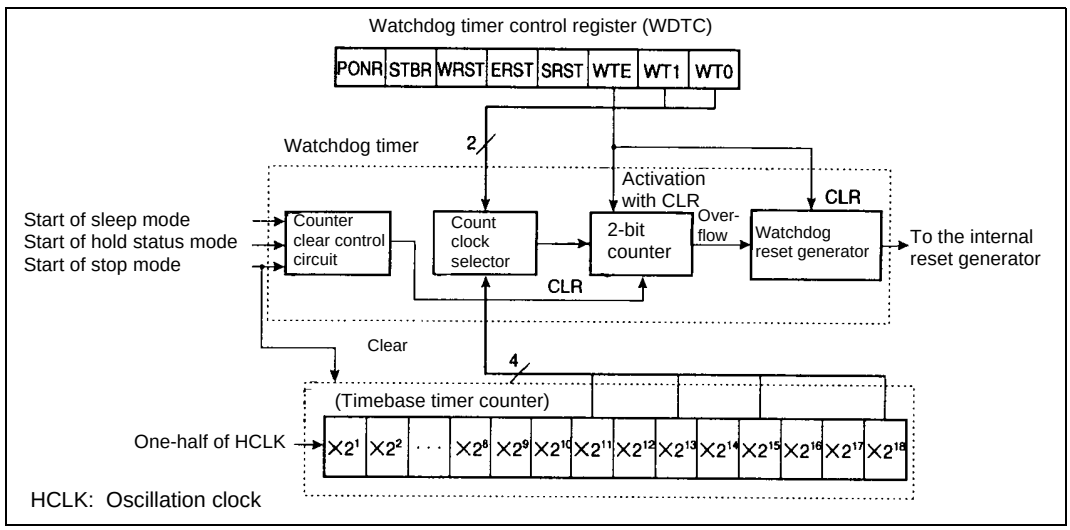
- Features of watchdog timer :
  Reset CPU at four different time intervals
  Status bits to indicate the reset causes

(1) Register configuration

Watchdog Timer Control Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 0000A8H	PONR	—	WRST	ERST	SRST	WTE	WT1	WT0	WDTC
Read/write ⇨	R	—	R	R	R	W	W	W	
Initial value ⇨	X	—	X	X	X	1	1	1	

(2) Block diagram



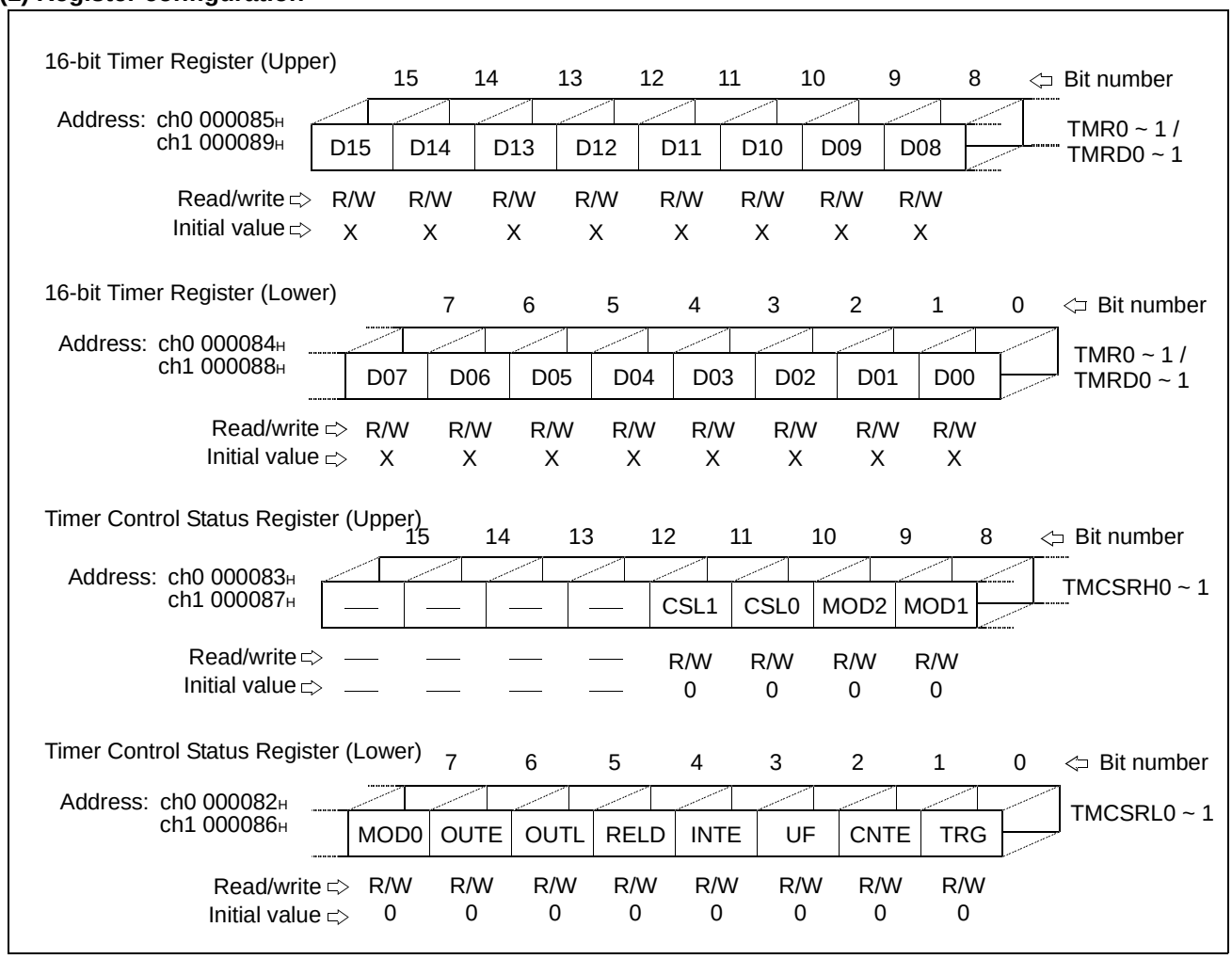
5. 16-bit reload timer (x 2)

The 16-bit reload timer provides two operating mode, internal clock mode and event count mode. In each operating mode, the 16-bit down counter can be reloaded (reload mode) or stopped when underflow (one-shot mode).
Output pins TO1 ~ TO0 are able to output different waveform accroding to the counter operating mode. TO1 ~ TO0 toggles when counter underflow if counter is operated as reload mode. TO1 ~ TO0 output specified level (H or L) when counter is counting if the counter is in one-shot mode.

Features of the 16 bit reload timer :

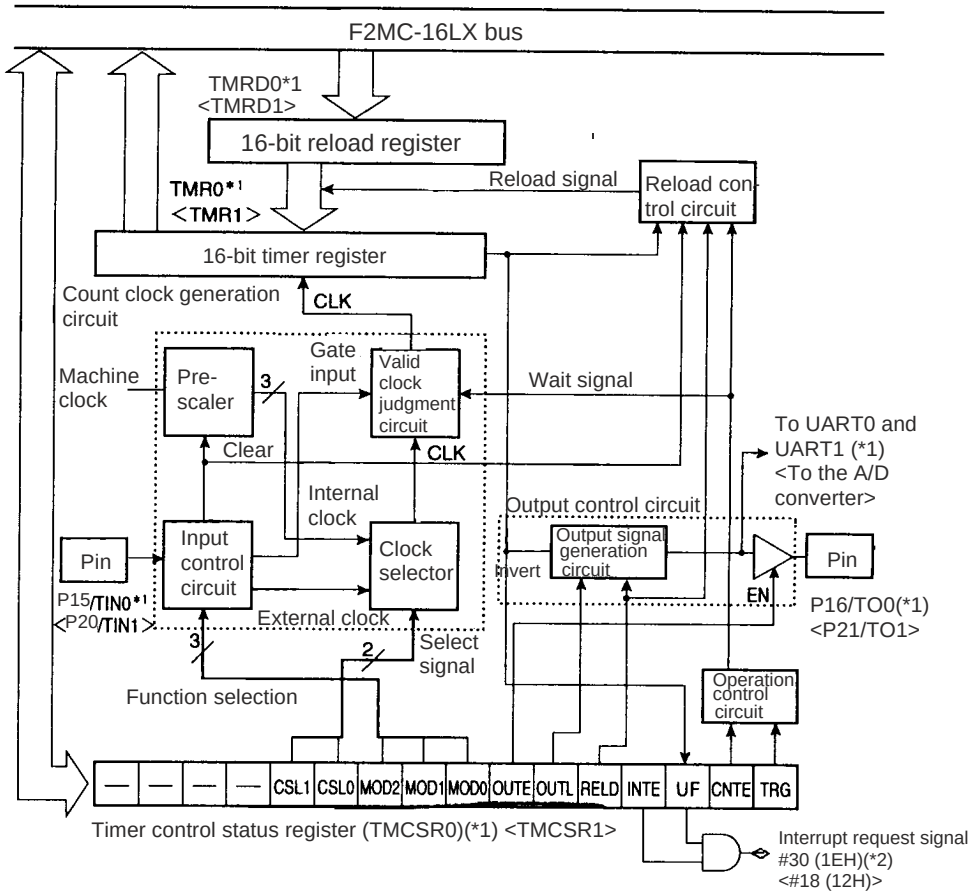
- Interrupt generated when timer underflow
- EI^{2}OS supported
- Internal clock operating mode :
  Three internal count clocks can be selected
  Counter can be activated by software or exteranl trigger (signal at TIN1 ~ TIN0 pin)
  Counter can be reloaded or stopped when underflow after activated
- Event count operating mode :
  Counter counts down by one when specified edge at TIN1 ~ TIN0 pin
  Counter can be reloaded or stopped when underflow

(1) Register configuration



Note : Registers TMR0~1/TMRD0~1 are word access only.

(2) Block diagram



*1 This register includes channel 0 and channel 1. The register enclosed in < and > indicates the channel 1 register.

*2 Interrupt number

6. 16-bit PPG Timer (x 3, PPG1 is not present in MB90465 series)

The 16-bit PPG timer consists of a 16-bit down counter, prescaler, 16-bit period setting register, 16-bit duty setting register, 16-bit control register and a PPG output pin. This module can be used to output pulses synchronized by software trigger or GATE signal from Multi-functional timer, refer to “Multi-functional Timer”.

Features of 16-bit PPG timer :

- Two operating mode : PWM and One-shot
- 8 types of counter operation clock (ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128) can be selected
- Interrupt is generated when trigger signal arrived, or counter borrow, or change of PPG output
- EI^{2}OS supported

(1) Register configuration

PPG Control Status Register (Upper)

Address: ch0 00003F$_H$
ch1 000047$_H$
ch2 00004F$_H$

Bit number	15	14	13	12	11	10	9	8
PCNTH0 ~ 2	CNTE	STGR	MDSE	RTRG	CKS2	CKS1	CKS0	PGMS
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value ⇨	0	0	0	0	0	0	0	0

PPG Control Status Register (Lower)

Address: ch0 00003E$_H$
ch1 000046$_H$
ch2 00004E$_H$

Bit number	7	6	5	4	3	2	1	0
PCNTL0 ~ 2	—	—	IREN	IRQF	IRS1	IRS0	POEN	OSEL
Read/write ⇨	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Initial value ⇨	—	—	0	0	0	0	0	0

PPG Duty Setting Register (Upper)

Address: ch0 00003D$_H$
ch1 000045$_H$
ch2 00004D$_H$

Bit number	15	14	13	12	11	10	9	8
PDUT0 ~ 2	DU15	DU14	DU13	DU12	DU11	DU10	DU09	DU08
Read/write ⇨	W	W	W	W	W	W	W	W
Initial value ⇨	X	X	X	X	X	X	X	X

PPG Duty Setting Register (Lower)

Address: ch0 00003C$_H$
ch1 000044$_H$
ch2 00004C$_H$

Bit number	7	6	5	4	3	2	1	0
PDUT0 ~ 2	DU07	DU06	DU05	DU04	DU03	DU02	DU01	DU00
Read/write ⇨	W	W	W	W	W	W	W	W
Initial value ⇨	X	X	X	X	X	X	X	X

PPG Period Setting Register (Upper)

Address: ch0 00003B$_H$
ch1 000043$_H$
ch2 00004B$_H$

Bit number	15	14	13	12	11	10	9	8
PCSR0 ~ 2	CS15	CS14	CS13	CS12	CS11	CS10	CS09	CS08
Read/write ⇨	W	W	W	W	W	W	W	W
Initial value ⇨	X	X	X	X	X	X	X	X

PPG Period Setting Register (Lower)

Address: ch0 00003A$_H$
ch1 000042$_H$
ch2 00004A$_H$

Bit number	7	6	5	4	3	2	1	0
PCSR0 ~ 2	CS07	CS06	CS05	CS04	CS03	CS02	CS01	CS00
Read/write ⇨	W	W	W	W	W	W	W	W
Initial value ⇨	X	X	X	X	X	X	X	X

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PPG Down Counter Register (Upper)

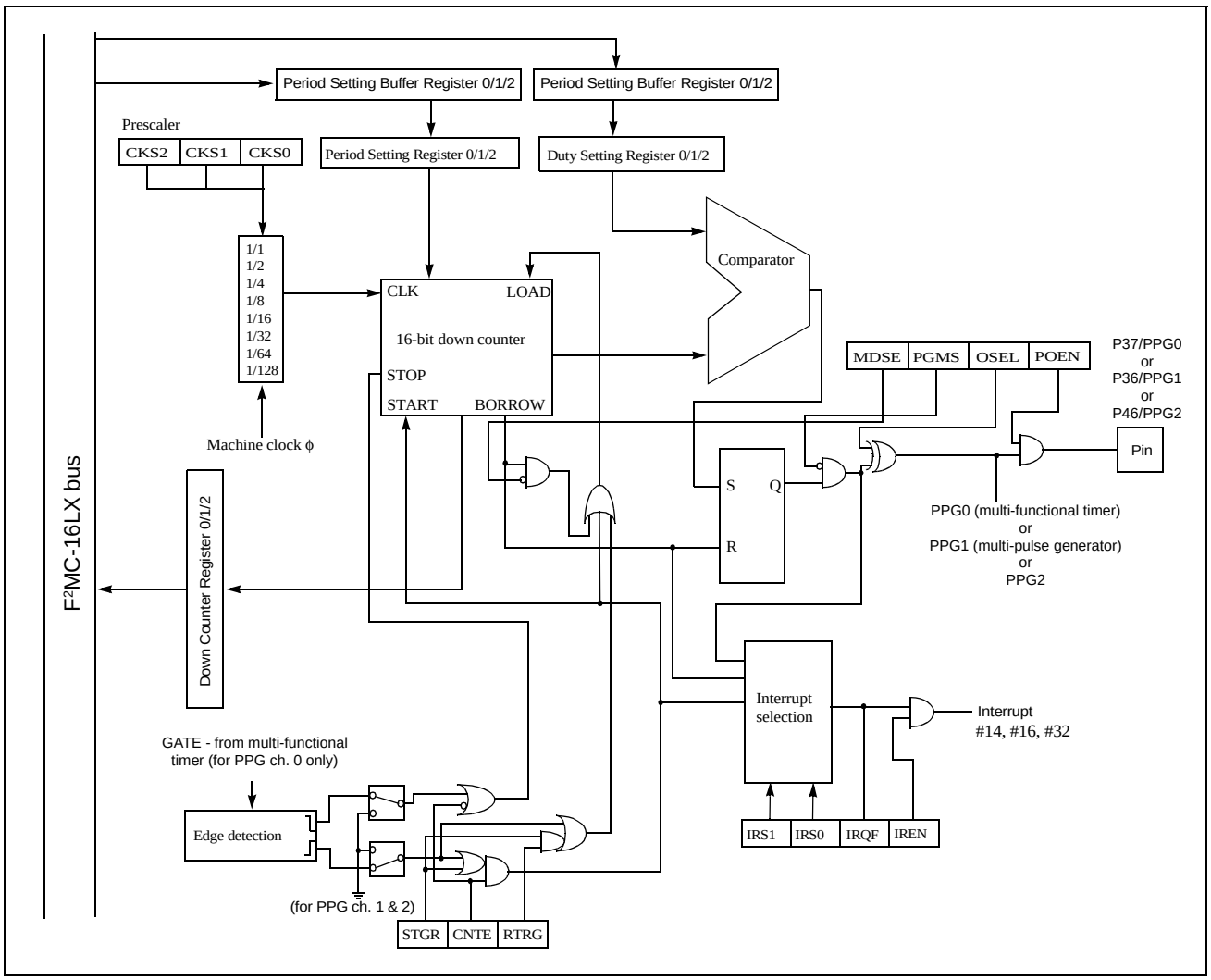
Address:	15	14	13	12	11	10	9	8	⇦ Bit number
ch0 000039H ch1 000041H ch2 000049H	DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08	PDCR0 ~ 2
Read/write ⇨	R	R	R	R	R	R	R	R	
Initial value ⇨	1	1	1	1	1	1	1	1	

PPG Down Counter Register (Lower)

Address:	7	6	5	4	3	2	1	0	⇦ Bit number
ch0 000038H ch1 000040H ch2 000048H	DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00	PDCR0 ~ 2
Read/write ⇨	R	R	R	R	R	R	R	R	
Initial value ⇨	1	1	1	1	1	1	1	1	

Note : Registers PDCR0~2, PDSR0~2 and PDUT0~2 are word access only

(2) Block diagram



7. Multi-functional Timer

The 16-bit multi-functional timer module consists of one 16-bit free-running timer, four input capture circuits, six output comparators and one channel of 16-bit PPG timer. This module allows six independent waveforms generated by PPG timer or waveform generator to be outputted. With the 16-bit free-running timer and the input capture circuit, input pulse width and external clock period measurement can be done.

(1) 16-bit free-running timer (1 channel)

- The 16-bit free-running timer consists of a 16-bit up/up-down counter, control register, 16-bit compare clear register (with buffer register) and a prescaler.
- 8 types of counter operation clock (ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128) can be selected. (ϕ is the machine clock)
- Two types of interrupt causes :
  - Compare clear interrupt is generated when there is a comparing match with compare clear register and 16-bit free-running timer.
  - Zero detection interrupt is generated while 16-bit free-running timer is detected as zero in count value.
- EI^{2}OS supported.
- Compare-clear register buffer provided :
  The selectable buffer enables the 16-bit free-running timer update its compare-clear register automatically without stop the timer operation. User can read the next compare-clear value to the compare-clear reigster when the timer is running. The compare-clear register will be updated when the timer value is "0000$_H$"
- Reset, software clear, compare match with compare clear register in up-count mode will reset the counter value to "0000$_H$".
- Supply clock to output compare module :
  The prescaler ouptut is acted as the count clock of the output compare.

(2) Output compare module (6 channels)

- The output compare module consists of six 16-bit compare registers (with selectable buffer register), compare output latch and compare control registers. An interrupt is generated and output level is inverted when the value of 16-bit free-running timer and compare register are matched.
- 6 compare registers can be operated independently.
- Output pins and interrupt flag are corresponding to each compare register.
- 2 compare registers can be paired to control the output pins.
- Inverts output pins by using 2 compare registers together.
- Setting the initial value for each output pin is possible.
- Interrupt generated when there is a comparing match with output compare register and 16-bit free-running timer.
- EI^{2}OS supported.

(3) Input capture module (4 channels)

Input capture consists of 4 independent external input pins, the corresponding capture register and capture control register. By detecting any edge of the input signal from the external pin, the value of the 16-bit free-running timer can be stored in the capture register and an interrupt is generated simultaneously.

- Operations synchronized with the 16-bit free-running timer's count clock.
- 3 types of trigger edge (rising edge, falling edge and both edge) of the external input signal can be selected and there is indication bit to show the trigger edge is rising or falling.
- 4 input captures can be operated independently.
- Two independent interrupts are generated when detecting a valid edge from external input.
- EI^{2}OS supported.

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(4) 16-bit PPG timer (x 1)

The 16-bit PPG timer 0 is used to provide a PPG signal for waveform generator. (See section "■ PERIPHERAL RESOURCES", "6. 16-bit PPG Timer")

(5) Waveform generator module

The waveform generator consists of three 16-bit timer registers, three timer control registers and 16-bit waveform control register.
With waveform generator, it is possible to generate real time output, 16-bit PPG waveform output, non-overlap 3-phase waveform output for inverter control and DC chopper waveform output.

- It is possible to generate a non-overlap waveform output based on dead-time of 16-bit timer. (Dead-time timer function)
- It is possible to generate a non-overlap waveform output when realtime output is operated in 2-channel mode. (Dead-time timer function)
- By detecting realtime output compare match, GATE signal of the PPG timer operation will be generated to start or stop PPG timer operation. (GATE function)
- When a match is detected by real time output compare, the 16-bit timer is activated. The PPG timer can be started or stopped easily by generating a GATE signal for PPG operation until the 16-bit timer stops. (GATE function)
- Force to stop output waveform using DTTI0 pin input.
- Interrupt is generated when DTTI0 active or 16-bit tmer underflow.
- EI^{2}OS supported.

(6) Register configuration

- 16-bit free-running timer registers

Timer Control Status Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00005F$_H$	ECKE	IRQZF	IRQZE	MSI2	MSI1	MSI0	ICLR	ICRE	TCCSH
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Timer Control Status Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00005E$_H$	—	BFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0	TCCSL
Read/write ⇨	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	—	0	1	0	0	0	0	0	

Timer Data Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00005D$_H$	T15	T14	T13	T12	T11	T10	T09	T08	TCDT
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Timer Data Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00005C$_H$	T07	T06	T05	T04	T03	T02	T01	T00	TCDT
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

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Compare Clear Buffer Register / Compare Clear Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00005B$_H$	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	CPCLRB/CPCLR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	1	1	

Compare Clear Buffer Register / Compare Clear Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00005A$_H$	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	CPCLRB/CPCLR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	1	1	

Note : Registers TCDT, CPCLRB/CPCLR are word access only.

- Output compare registers

Compare Control Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: ch1 00007D$_H$ ch3 00007F$_H$ ch5 000081$_H$	—	BTS1	BTS0	CMOD	OTE1	OTE0	OTD1	OTD0	OCS1/3/5
Read/write ⇨	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	—	1	1	0	0	0	0	0	

Compare Control Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: ch0 00007C$_H$ ch2 00007E$_H$ ch4 000080$_H$	IOP1	IOP0	IOE1	IOE0	BUF1	BUF0	CST1	CST0	OCS0/2/4
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	1	1	0	0	

Output Compare Buffer Register / Output Compare Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: ch0 000071$_H$ ch1 000073$_H$ ch2 000075$_H$ ch3 000077$_H$ ch4 000079$_H$ ch5 00007B$_H$	OP15	OP14	OP13	OP12	OP11	OP10	OP09	OP08	OCCPB0 ~ 5/ OCCP0 ~ 5
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Output Compare Buffer Register / Output Compare Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: ch0 000070$_H$ ch1 000072$_H$ ch2 000074$_H$ ch3 000076$_H$ ch4 000078$_H$ ch5 00007A$_H$	OP07	OP06	OP05	OP04	OP03	OP02	OP01	OP00	OCCPB0 ~ 5/ OCCP0 ~ 5
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Note : Register OCCPB0~5/OCCP0~5 are word access only.

• Input capture registers

Input Capture Control Status Register (2/3) (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00006B$_H$	—	—	—	—	—	—	IEI3	IEI2	ICSH23
Read/write ⇨	—	—	—	—	—	—	R	R	
Initial value ⇨	—	—	—	—	—	—	0	0	

Input Capture Control Status Register (2/3) (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00006A$_H$	ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20	ICSL23
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

PPG output control/ Input Capture Control Status Register (0/1) (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 000069$_H$	PGEN5	PGEN4	PGEN3	PGEN2	PGEN1	PGEN0	IEI1	IEI0	PICSH01
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R	R	
Initial value ⇨	0	0	0	0	0	0	0	0	

Input Capture Control Register (0/1)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 000068$_H$	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	PICSL01
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Input Capture Data Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: ch0 000061$_H$ ch1 000063$_H$ ch2 000065$_H$ ch3 000067$_H$	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	IPCP0 ~ 3
Read/write ⇨	R	R	R	R	R	R	R	R	
Initial value ⇨	X	X	X	X	X	X	X	X	

Input Capture Data Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: ch0 000060$_H$ ch1 000062$_H$ ch2 000064$_H$ ch3 000066$_H$	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	IPCP0 ~ 3
Read/write ⇨	R	R	R	R	R	R	R	R	
Initial value ⇨	X	X	X	X	X	X	X	X	

Note : Registers IPCP0~3 are word access only.

• Waveform generator registers

Waveform Control Register

Bit number	15	14	13	12	11	10	9	8	
Address: 000059H	DTIE	DTIF	NRSL	DCK2	DCK1	DCK0	NWS1	NWS0	SIGCR
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

16-bit Timer Control Register

Bit number	7	6	5	4	3	2	1	0	
Address: ch0 000056H ch2 000058H	DMOD	GTEN1	GTEN0	TMIF	TMIE	TMD2	TMD1	TMD0	DTCR0, DTCR2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

16-bit Timer Control Register

Bit number	15	14	13	12	11	10	9	8	
Address: ch1 000057H	DMOD	GTEN1	GTEN0	TMIF	TMIE	TMD2	TMD1	TMD0	DTCR1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

16-bit Timer Register (Upper)

Bit number	15	14	13	12	11	10	9	8	
Address: ch0 000051H ch1 000053H ch2 000055H	TR15	TR14	TR13	TR12	TR11	TR10	TR09	TR08	TMRR0~2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	

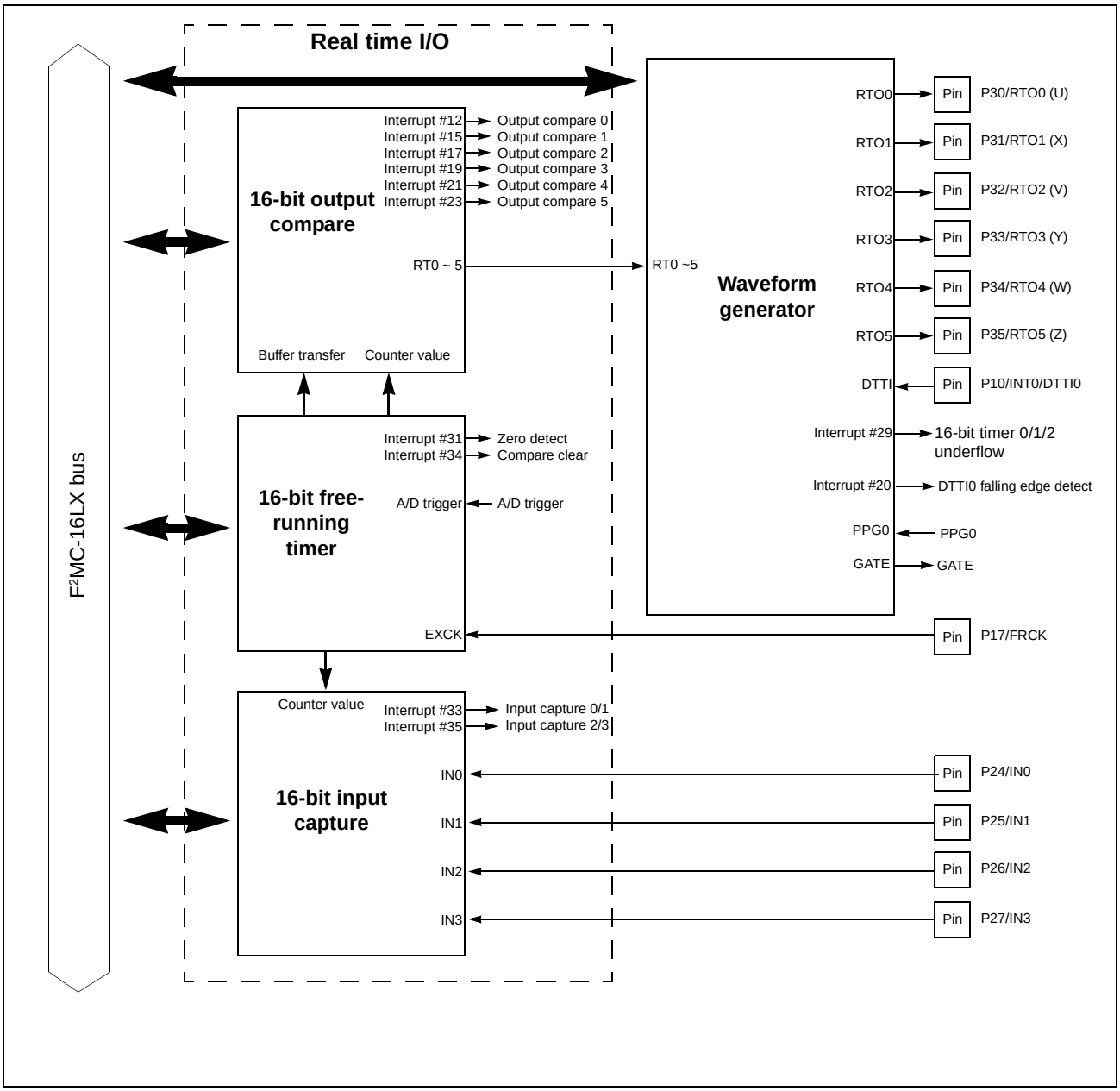
16-bit Timer Register (Lower)

Bit number	7	6	5	4	3	2	1	0	
Address: ch0 000050H ch1 000052H ch2 000054H	TR07	TR06	TR05	TR04	TR03	TR02	TR01	TR00	TMRR0~2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	

Note : Registers TMRR0 ~ 2 are word access only

(7) Block diagram

- Block diagram of Multi-functional timer



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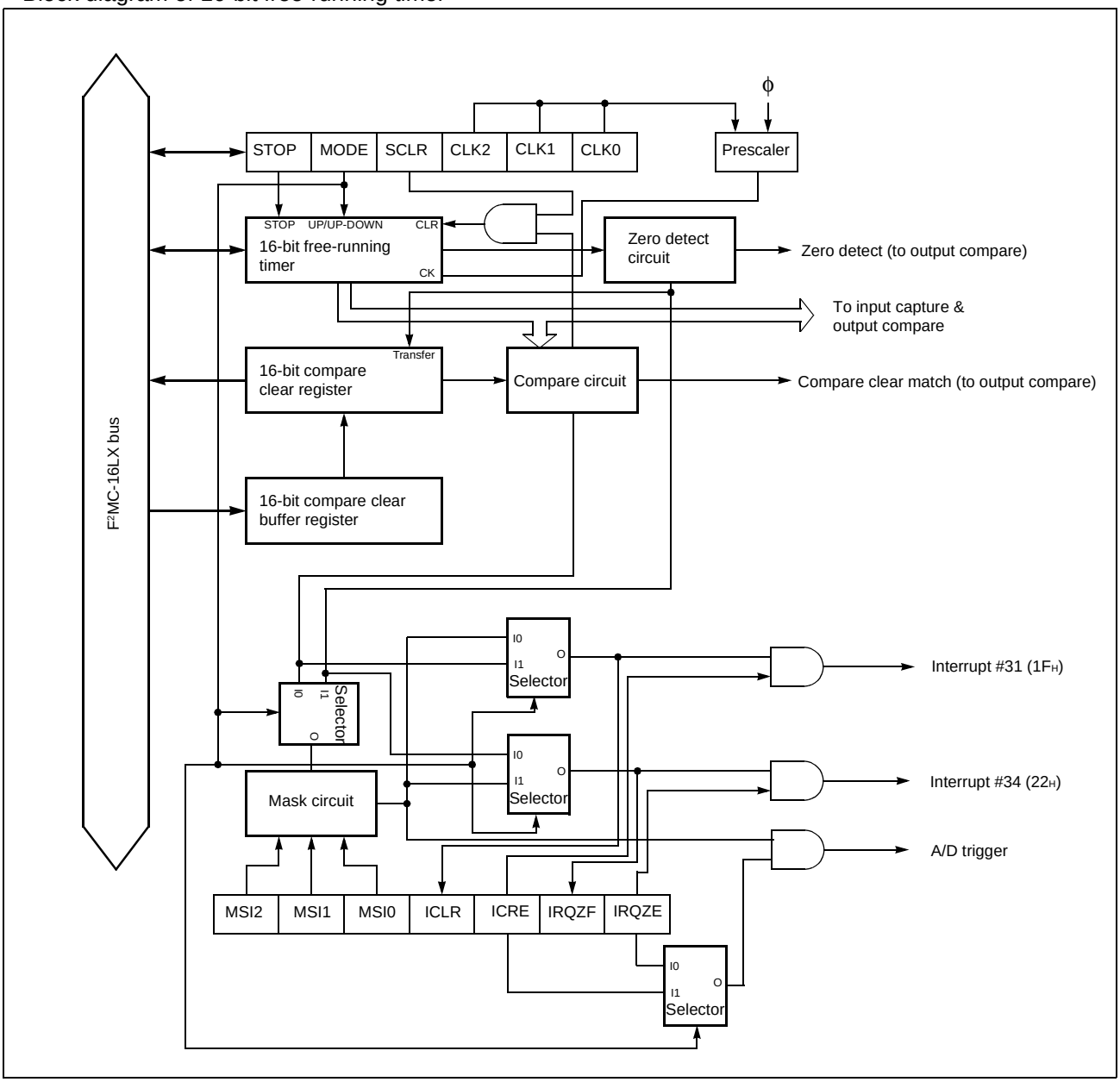
- Block diagram of 16-bit free-running timer



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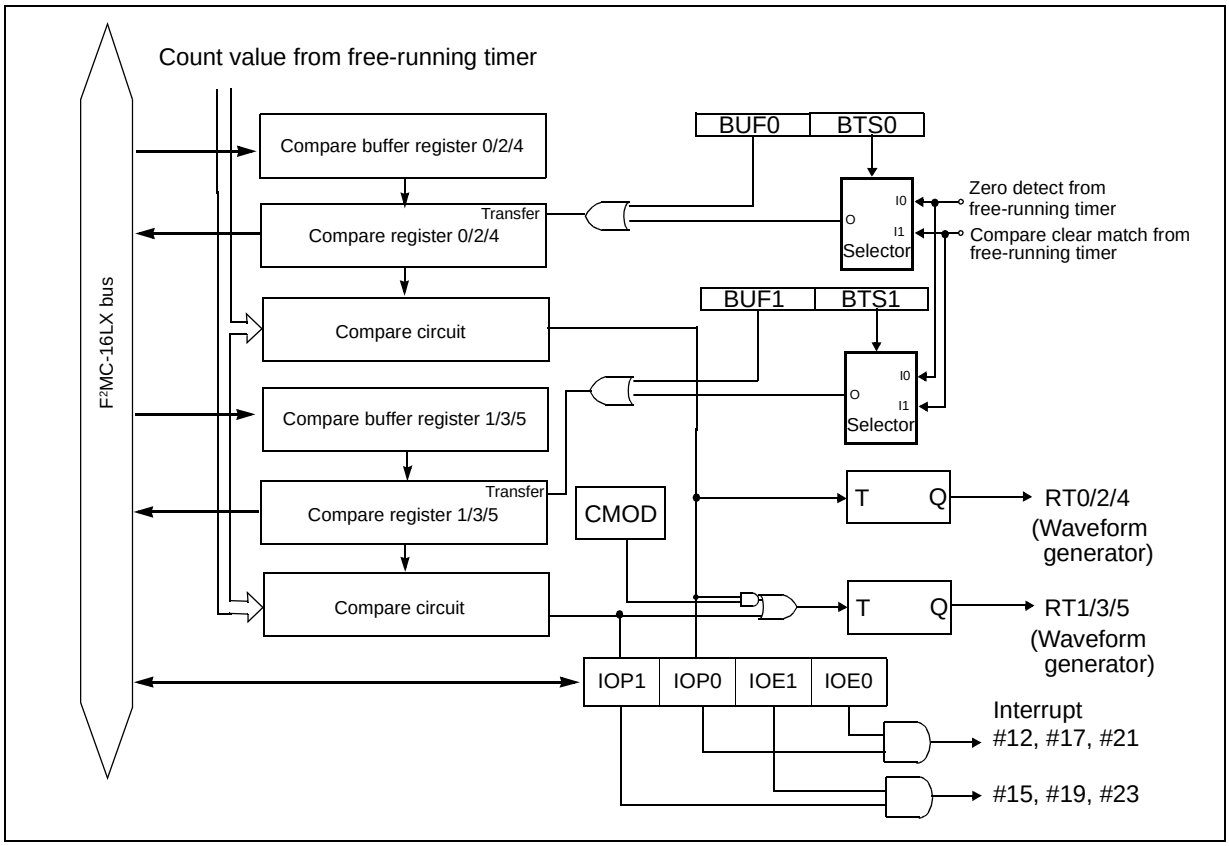
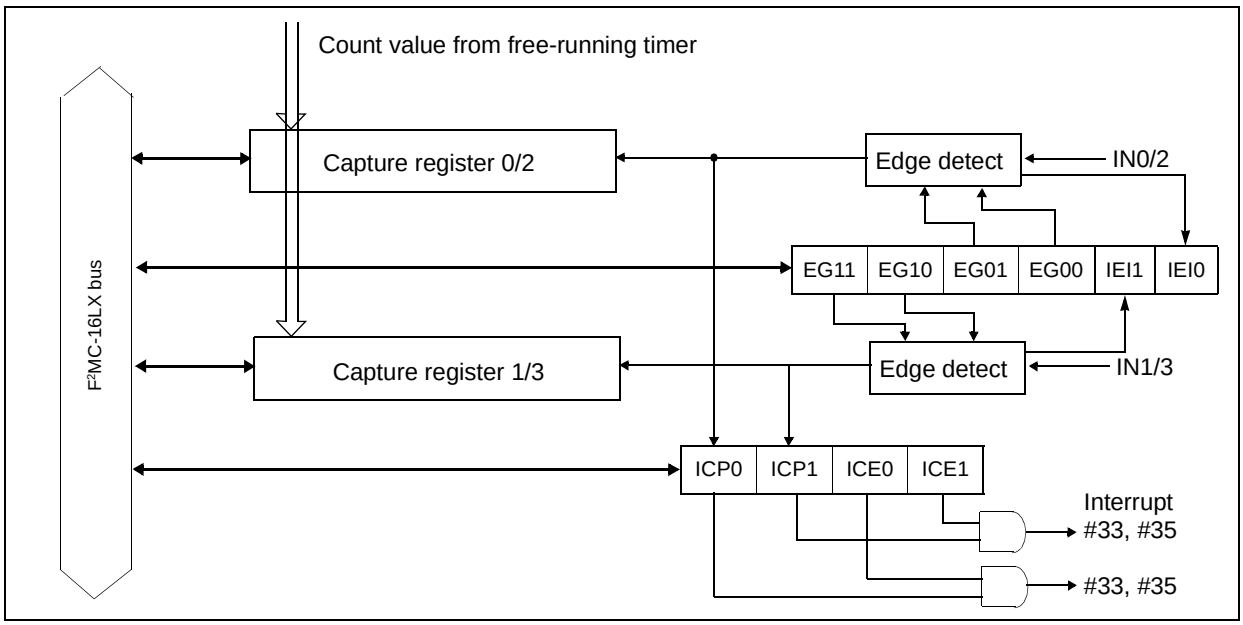
- Block diagram of 16-bit output compare



- Block diagram of 16-bit input capture



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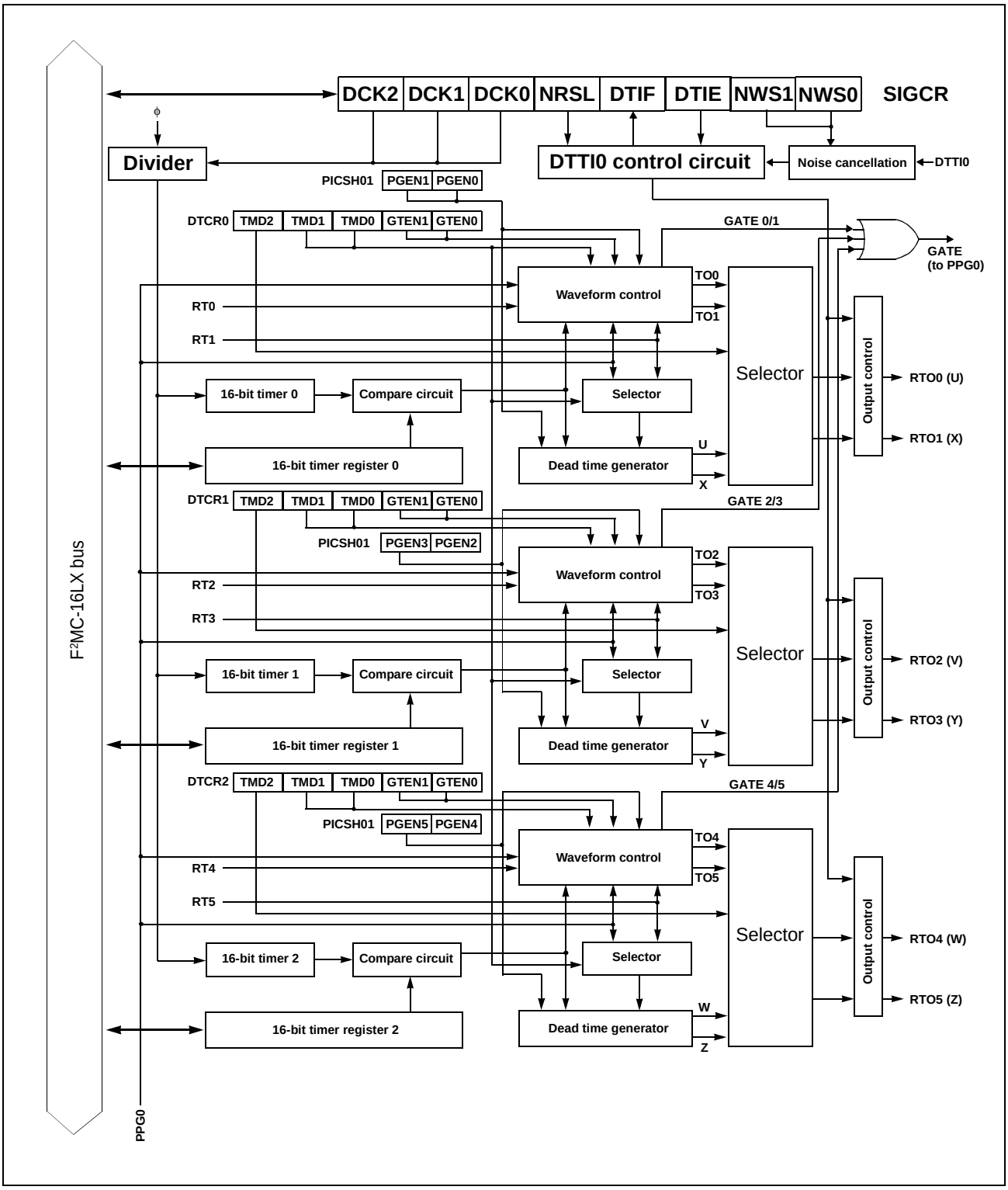
- Block diagram of waveform generator



8. Multi-pulse Generator (Not present in MB90465 series, but the 16-bit reload timer 0 can be used individually)

The Multi-pulse generator consists of a 16-bit PPG timer, a 16-bit reload timer and a waveform sequencer.

The Multi-pulse generator has the following features :

- Output signal control
  - 12 output data buffer registers are provided
  - Output data register can be updated by any one of output data buffer registers when :
  1. an effective edge detected at SNI2 ~ SNI0 pin
  2. 16-bit reload timer underflow
  3. output data buffer register OPDBR0 is written
- Output data register (OPDR) determines which OPT terminals (OPT5 ~ 0) output the 16-bit PPG waveform
  - Waveform sequencer is provided with a 16-bit timer to measure the speed of motor
  - The 16-bit timer can be used to disable the OPT output when the position detection is missing
- Input position detect control
  - SNI2 ~ SNI0 input can be used to detect the rotor position
  - A controllable noise filter is provided to the SNI2 ~ SNI0 input
- PPG synchronization for output signal
  - OPT output is able to synchronize the edge of PPG waveform to avoid a short pulse (or glitch) appearance
- Various interrupt generation causes
- EI^{2}OS supported

(1) 16-bit PPG timer (x 1, not present in MB90465 series)

The 16-bit PPG timer 1 is used to provide a PPG signal for waveform sequencer. (See section "■ PERIPHERAL RESOURCES", "6. 16-bit PPG Timer")

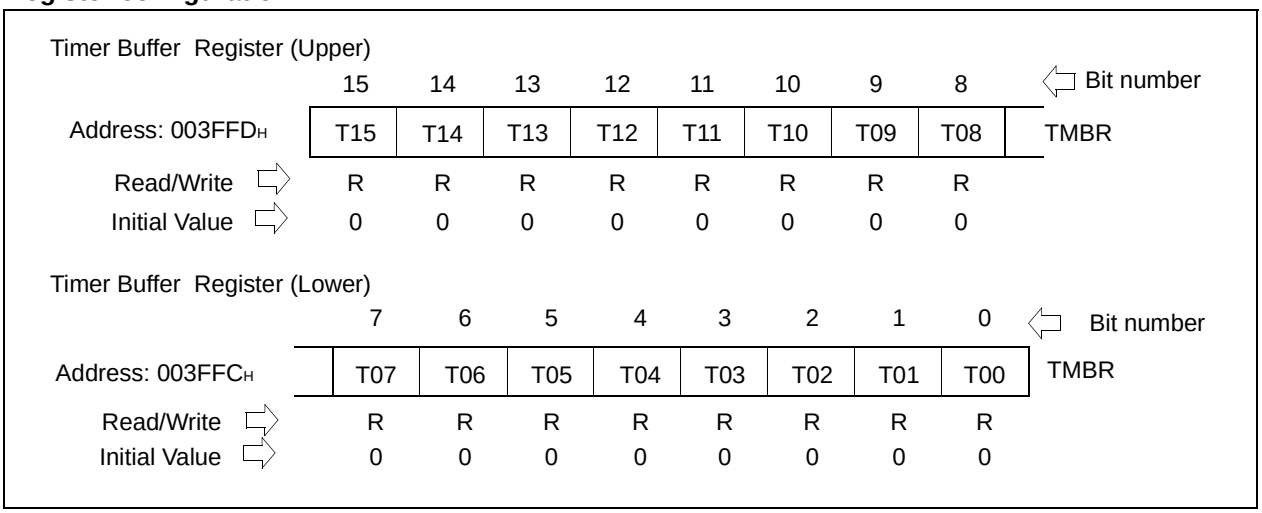
(2) 16-bit reload timer (x 1)

The 16-bit reload timer 0 is used to provide signal to waveform sequencer. (See section "■ PERIPHERAL RESOURCES", "5. 16-bit Reload Timer")

(3) Waveform sequencer (not present in MB90465 series)

By using the waveform sequencer, 16-bit PPG timer output signal can be directed to Multi-pulse generator output (OPT5 ~ 0) according to the input signal of Multi-pulse generator (SNI2 ~ 0). Meanwhile, the OPT5 ~ 0 output signal can be hardware terminated by DTTI input (DTTI1) in case of emergency. The OPT5 ~ 0 output signals are synchronized with the PPG signal in order to eliminate the unwanted glitch.

(4) Register configuration



Note : Register TMBR is word access only.

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Compare Clear Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 003FFB$_H$	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	CPCR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	X	X	X	X	X	X	X	X	

Compare Clear Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 003FFA$_H$	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	CPCR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	X	X	X	X	X	X	X	X	

Output Data Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 003FF9$_H$	BNKF	RDA2	RDA1	RDA0	OP51	OP50	OP41	OP40	OPDR
Read/Write ⇨	R	R	R	R	R	R	R	R	
Initial Value ⇨	0	0	0	0	X	X	X	X	

Output Data Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 003FF8$_H$	OP31	OP30	OP21	OP20	OP11	OP10	OP01	OP00	OPDR
Read/Write ⇨	R	R	R	R	R	R	R	R	
Initial Value ⇨	X	X	X	X	X	X	X	X	

Output Data Buffer Registers (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Addresses: 003FF7$_H$~E1$_H$ (Odd Addresses)	BNKF	RDA2	RDA1	RDA0	OP51	OP50	OP41	OP40	OPDBRB~0
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

Output Data Buffer Registers (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Addresses: 003FF6$_H$~E0$_H$ (Even Addresses)	OP31	OP30	OP21	OP20	OP11	OP10	OP01	OP00	OPDBRB~0
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

Note : Registers CPCR, OPDR, OPDBRB~0 are word access only

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Noise Cancellation Control Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00008F$_H$	S21	S20	S11	S10	S01	S00	D1	D0	NCCR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

Timer Control Status Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00008E$_H$	TCLR	MODE	ICLR	ICRE	TMEN	CLK2	CLK1	CLK0	TCSR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

Input Control Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00008D$_H$	WTS1	WTS0	CPIF	CPIE	CPD2	CPD1	CPD0	CMPE	IPCUR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

Input Control Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00008C$_H$	CPE1	CPE0	SNC2	SNC1	SNC0	SEE2	SEE1	SEE0	IPCLR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

Output Control Register (Upper)

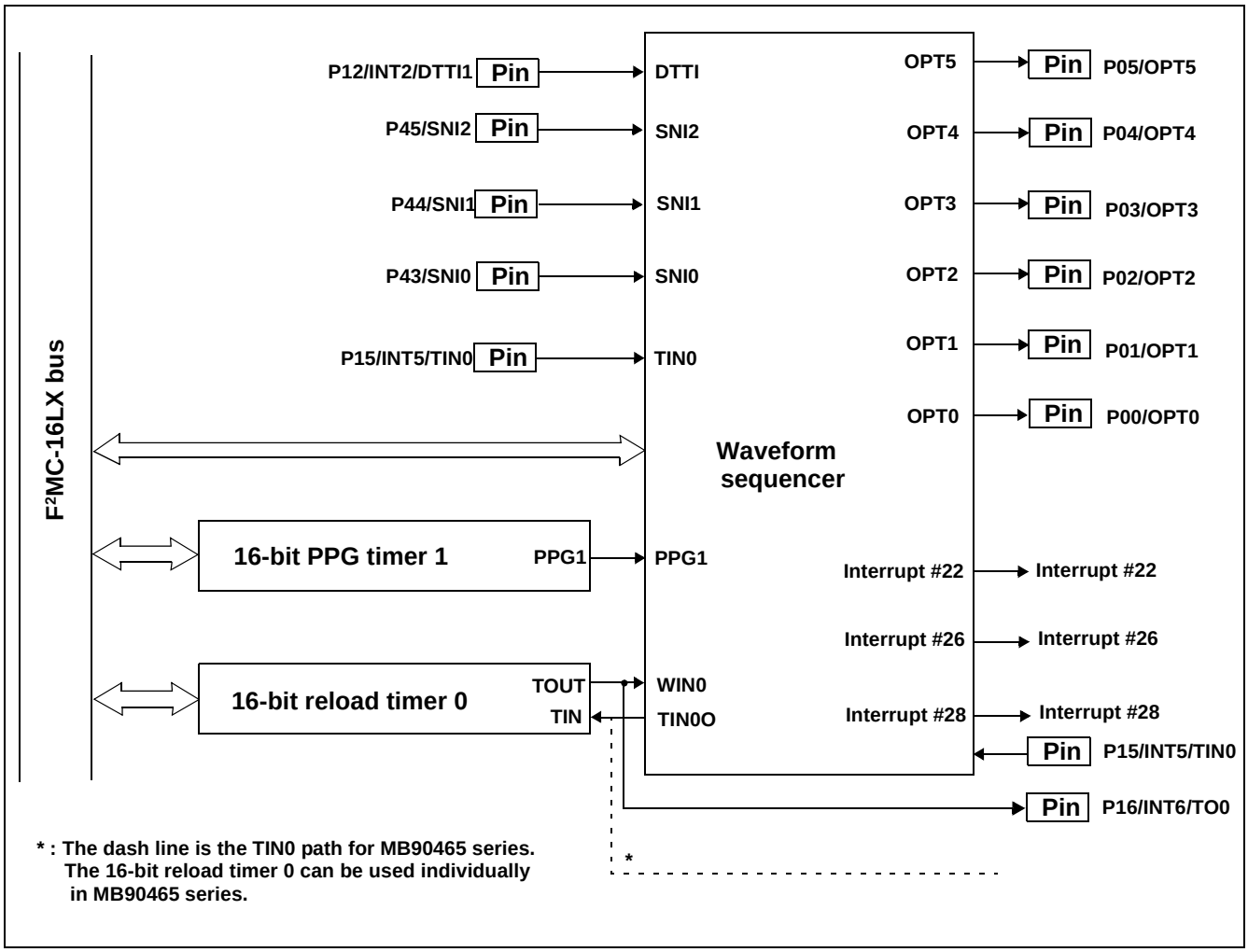
	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00008B$_H$	DTIE	DTIF	NRSL	OPS2	OPS1	OPS0	WTIF	WTIE	OPCUR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

Output Control Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00008A$_H$	PDIF	PDIE	OPE5	OPE4	OPE3	OPE2	OPE1	OPE0	OPCLR
Read/Write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value ⇨	0	0	0	0	0	0	0	0	

(5) Block diagram

- Block diagram of Multi-pulse generator



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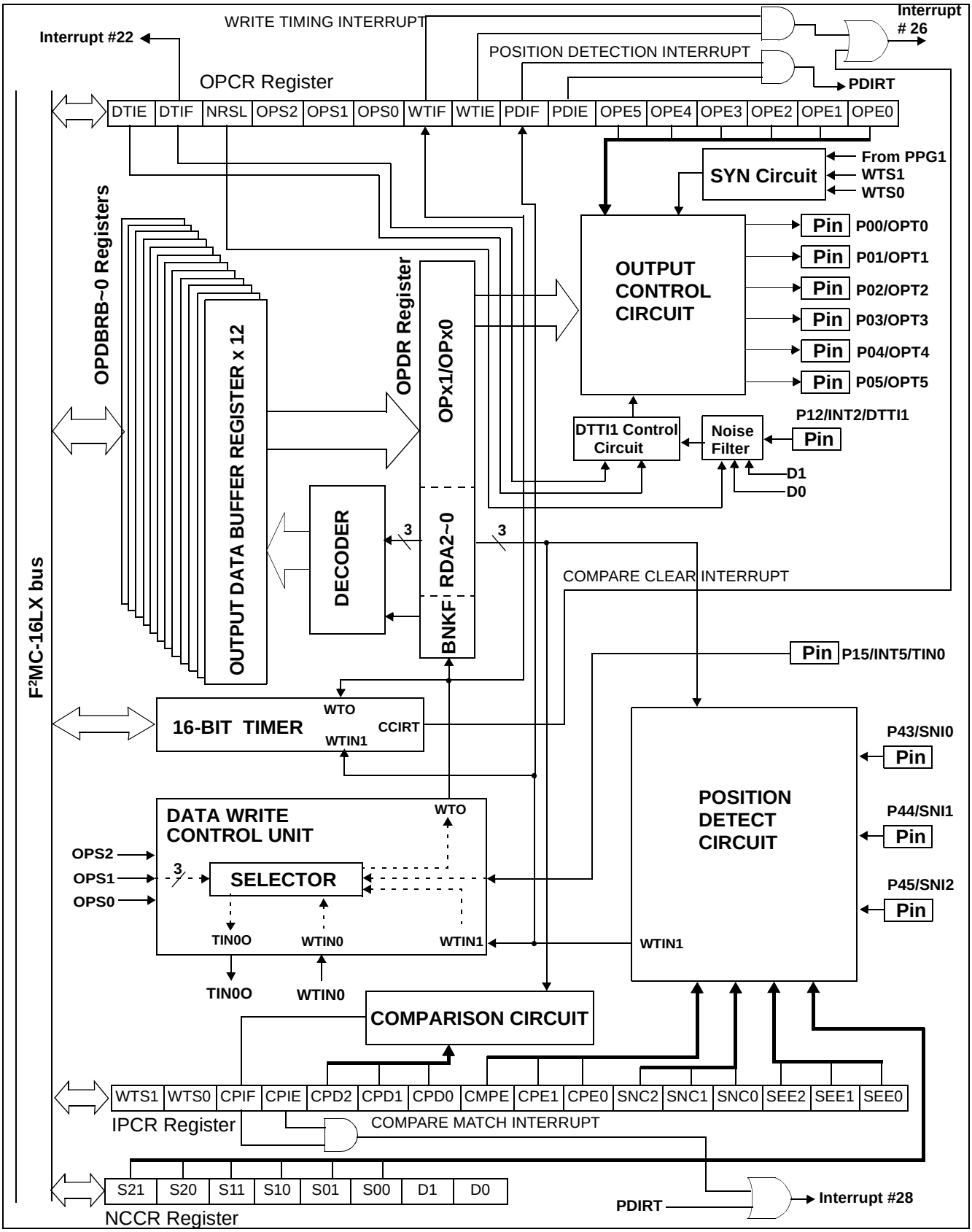
- Block diagram of waveform sequencer



9. PWC Timer (x 2, PWC0 is not present in MB90465 series)

The PWC (pulse width count) timer is a 16-bit multi-functional up counter with reload timer functions and input signal pulse width count functions.

The PWC timer consists of a 16-bit counter, an input pulse divider, a division ratio control register, a count input pin, a pulse output pin, and a 16-bit control register.

The PWC timer has the following features:

- Interrupt generated when timer overflow or end of PWC measurement.
- EI^{2}OS supported.
- Timer functions :
  - Generates an interrupt request at set time intervals.
  - Outputs pulse signals synchronized with the timer cycle.
  - Selects the counter clock from among three internal clocks.
- Pulse-width count functions:
  - Counts the time between external pulse input events.
  - Selects the counter clock from among three internal clocks.
  - Count mode:
    - H pulse width (rising edge to falling edge) / L pulse width (falling edge to rising edge)
    - Rising-edge cycle (rising edge to falling edge) / Falling-edge cycle (falling edge to rising edge)
    - Count between edges (rising or falling edge to falling or rising edge)

  Capable of counting cycles by dividing input pulses by 2^2, 2^4, 2^6, 2^8 using an 8-bit input divider.
  Generates an interrupt request upon the completion of count operation.
  Selects single or consecutive count operation.

(1) Register configuration

Division Rate Control Register

Address: ch0 00000C$_H$
ch1 00002C$_H$

	7	6	5	4	3	2	1	0	⇦ Bit number
	—	—	—	—	—	—	DIV1	DIV0	DIV0~1
Read/write ⇨	—	—	—	—	—	—	R/W	R/W	
Initial value ⇨	—	—	—	—	—	—	0	0	

PWC Data Buffer Register (Upper)

Address: ch0 00000B$_H$
ch1 00002B$_H$

	15	14	13	12	11	10	9	8	⇦ Bit number
	PW15	PW14	PW13	PW12	PW11	PW10	PW09	PW08	PWC0~1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

PWC Data Buffer Register (Lower)

Address: ch0 00000A$_H$
ch1 00002A$_H$

	7	6	5	4	3	2	1	0	⇦ Bit number
	PW07	PW06	PW05	PW04	PW03	PW02	PW01	PW00	PWC0~1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Note : Registers PWC0 ~ 1 are word access only.

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PWC Control Status Register (Upper)

Address: ch0 000009H
ch1 000029H

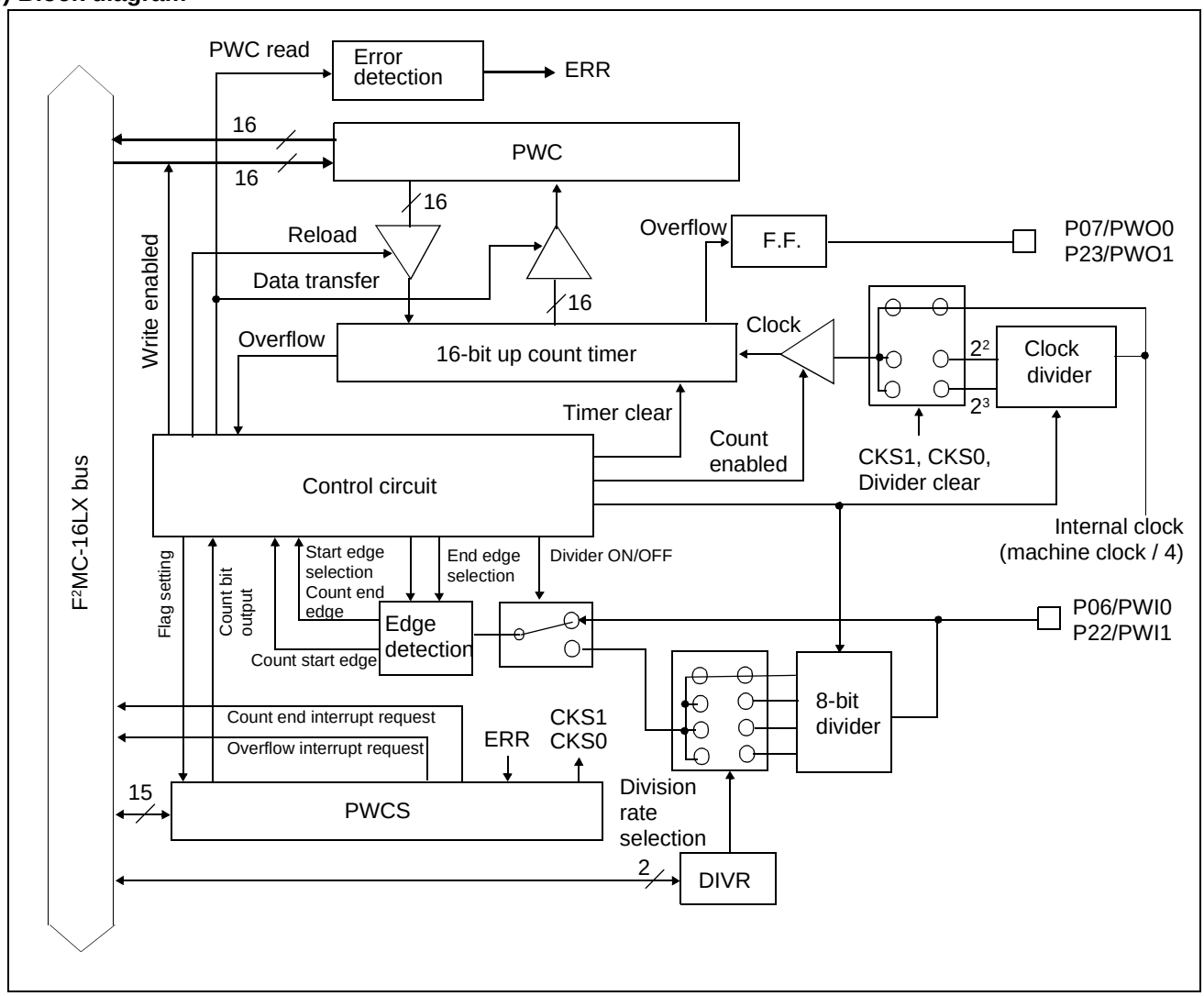
15	14	13	12	11	10	9	8	⇦ Bit number
STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	POUT	PWCSH0~1
Read/write ⇨	R/W	R/W	R	R/W	R/W	R/W	R	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

PWC Control Status Register (Lower)

Address: ch0 000008H
ch1 000028H

7	6	5	4	3	2	1	0	⇦ Bit number
CKS1	CKS0	Reserved	Reserved	S/C	MOD2	MOD1	MOD0	PWCSL0~1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

(3) Block diagram



10. UART (x 2)

The UART is a serial I/O port for asynchronous (start-stop) communication or clock-synchronous communication.
The UART has the following features :

- Full-duplex double buffering
- Capable of asynchronous (start-stop bit) and CLK-synchronous communications
- Support for the multiprocessor mode
- Various method of baud rate generation :
  - External clock input possible
  - Internal clock (a clock supplied from 16-bit reload timer can be used)
  - Embedded dedicated baud rate generator

Operation	Baud rate
Asynchronous	31250/9615/4808/2404/1202 bps
CLK synchronous	2 M/1 M/500 K/250 K/125 K/62.5 Kbps

  * : Assuming internal machine clock frequencies of 6, 8, 10, 12, and 16 MHz
- Error detection functions (parity, framing, overrun)
- NRZ (Non Return to Zero) signal format
- Interrupt request :
  - Receive interrupt (receive complete, receive error detection)
  - Transmit interrupt (transmission complete)
  - Transmit / receive conforms to extended intelligent I/O service (EI^{2}OS)

(1) Register configuration

Serial Status Register

Address: ch0 000023H
ch1 000027H

Bit number	15	14	13	12	11	10	9	8
SSR0~1	PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE
Read/write	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0

Serial Input Data Register / Serial Output Data Register

Address: ch0 000022H
ch1 000026H

Bit number	7	6	5	4	3	2	1	0
SIDR0~1 / SODR0~1	D7	D6	D5	D4	D3	D2	D1	D0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	X	X	X	X	X	X	X	X

Serial Control Register

Address: ch0 000021H
ch1 000025H

Bit number	15	14	13	12	11	10	9	8
SCR0~1	PEN	P	SBL	CL	A/D	REC	RXE	TXE
Read/write	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W
Initial value	0	0	0	0	0	1	0	0

Serial Mode Register

Address: ch0 000020H
ch1 000024H

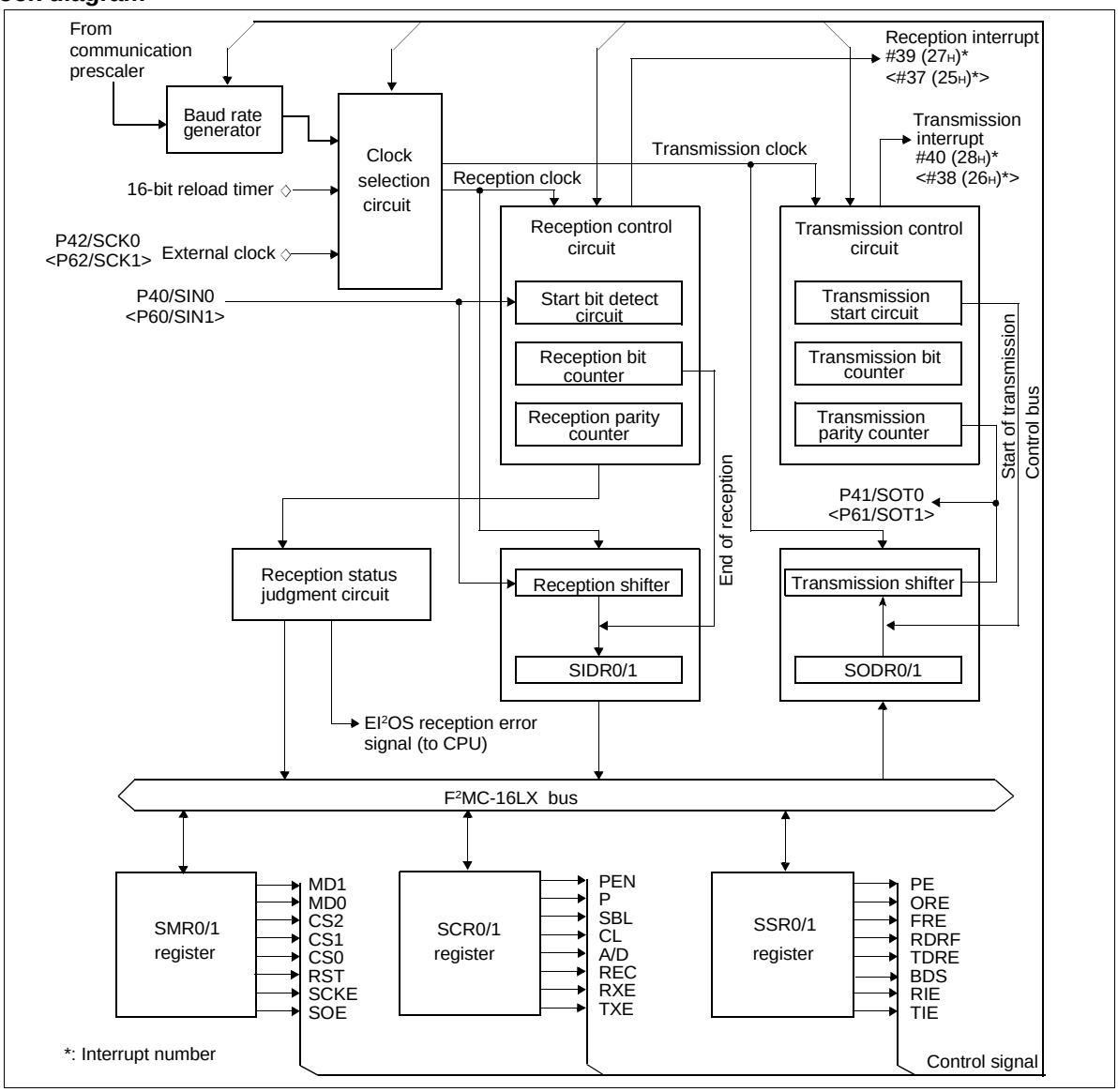
Bit number	7	6	5	4	3	2	1	0
SMR0~1	MOD1	MOD0	CS2	CS1	CS0	RST	SCKE	SOE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Communication Prescaler Control Register

Address: ch0 000019H
ch1 00001BH

Bit number	15	14	13	12	11	10	9	8
CDCR0~1	MD	—	—	—	—	DIV2	DIV1	DIV0
Read/write	R/W	—	—	—	—	R/W	R/W	R/W
Initial value	0	—	—	—	—	0	0	0

(2) Block diagram



11. DTP/External Interrupts

The DTP/external interrupt circuit is activated by the signal supplied to a DTP/external interrupt pin. The CPU accepts the signal using the same procedure it uses for normal hardware interrupts and generates external interrupts or activates the extended intelligent I/O service (EI²OS).

Features of DTP/External Interrupt :

- Total 8 external interrupt channels.
- Two request levels ("H" and "L") are provided for the intelligent I/O service.
- Four request levels (rising edge, falling edge, "H" level and "L" level) are provided for external interrupt requests.

(1) Register configuration

DTP/Interrupt Source Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 0000031H	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EIRR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

DTP/Interrupt Enable Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 000030H	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	ENIR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

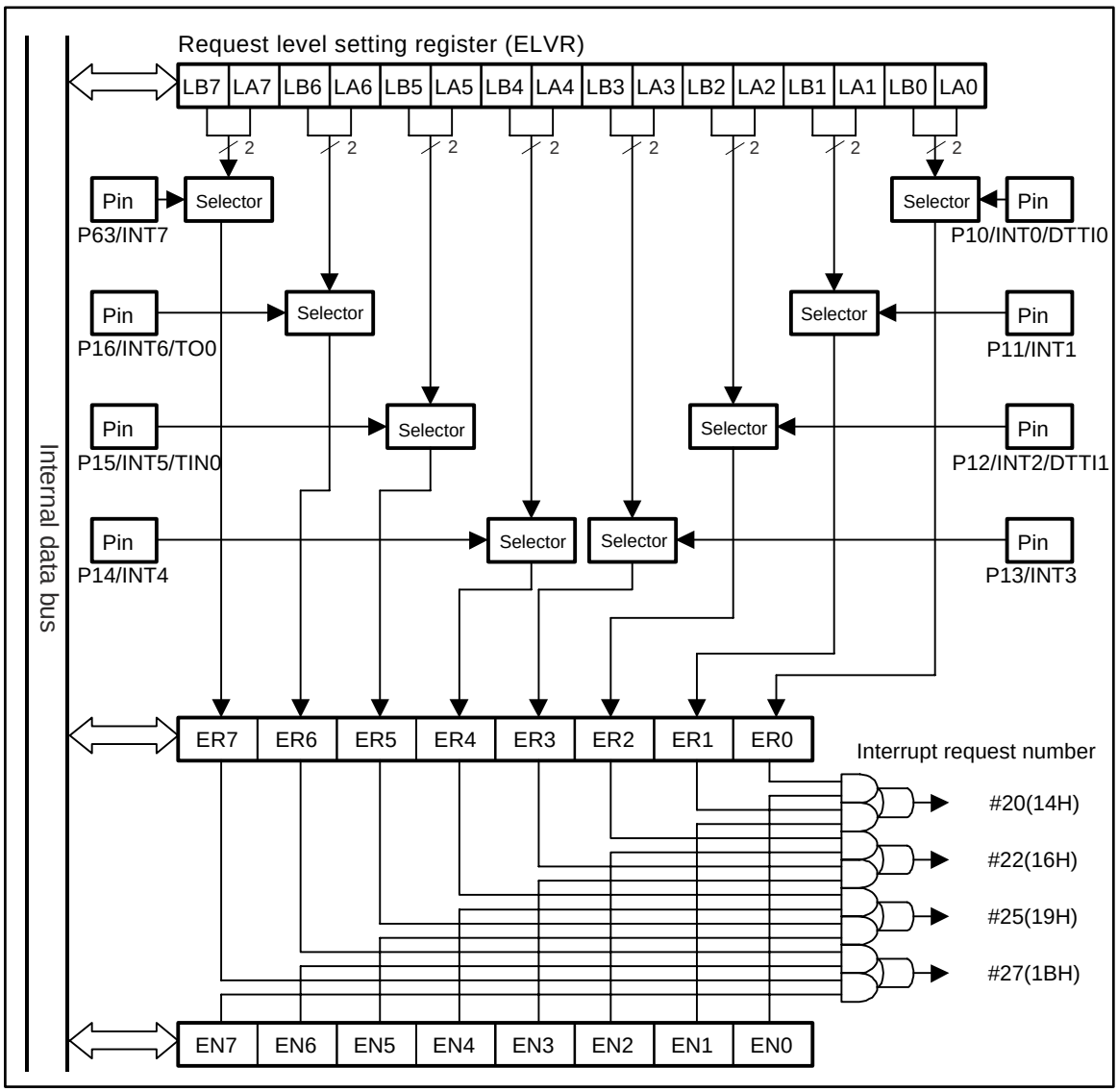
Request Level Setting Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 0000033H	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	ELVRH
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Request Level Setting Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 000032H	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	ELVRL
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

(2) Block diagram



12. Delayed Interrupt Generation Module

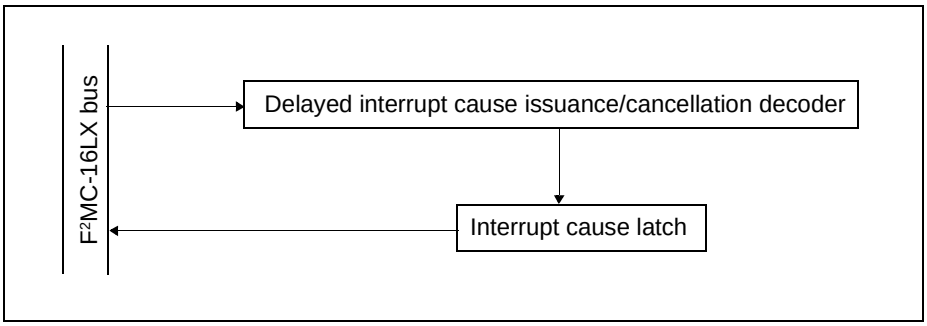
The delayed interrupt generation module is used to generate a task switching interrupt. Interrupt requests to the F²MC-16LX CPU can be generated and cleared by software using this module.

(1) Register configuration

Delayed interrupt generator module register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 00009F$_H$	—	—	—	—	—	—	—	R0	DIRR
Read/write ⇨	—	—	—	—	—	—	—	R/W	
Initial value ⇨	—	—	—	—	—	—	—	0	

(2) Block diagram



13. A/D Converter

The converter converts the analog voltage input to an analog input pin (input voltage) to a digital value. The converter has the following features :

- The minimum conversion time is 6.13 µs (for a machine clock of 16 MHz; includes the sampling time).
- The minimum sampling time is 3.75 µs (for a machine clock of 16 MHz).
- The converter uses the RC-type successive approximation conversion method with a sample and hold circuit.
- A resolution of 10 bits or 8 bits can be selected.
- Up to eight channels for analog input pins can be selected by a program.
- Various conversion mode :
  - Single conversion mode : Selectively convert one channel.
  - Scan conversion mode : Continuously convert multiple channels. Maximum of 8 program selectable channels.
  - Continuous conversion mode : Repeatedly convert specified channels.
  - Stop conversion mode : Convert one channel then halt until the next activation (enables synchronization of the conversion start timing).
- At the end of A/D conversion, an interrupt request can be generated and EI²OS can be activated.
- In the interrupt-enabled state, the conversion data protection function prevents any part of the data from being lost through continuous conversion.
- The conversion can be activated by software, 16-bit reload timer 1 (rising edge) and 16-bit free-running timer zero detection edge.

(1) Register configuration

Control Status Register (upper)

	15	14	13	12	11	10	9	8	
Address: 0000035H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	ADCS1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	W	—	
Initial value	0	0	0	0	0	0	0	—	

Control Status Register (lower)

	7	6	5	4	3	2	1	0	
Address: 000034H	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	ADCS0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

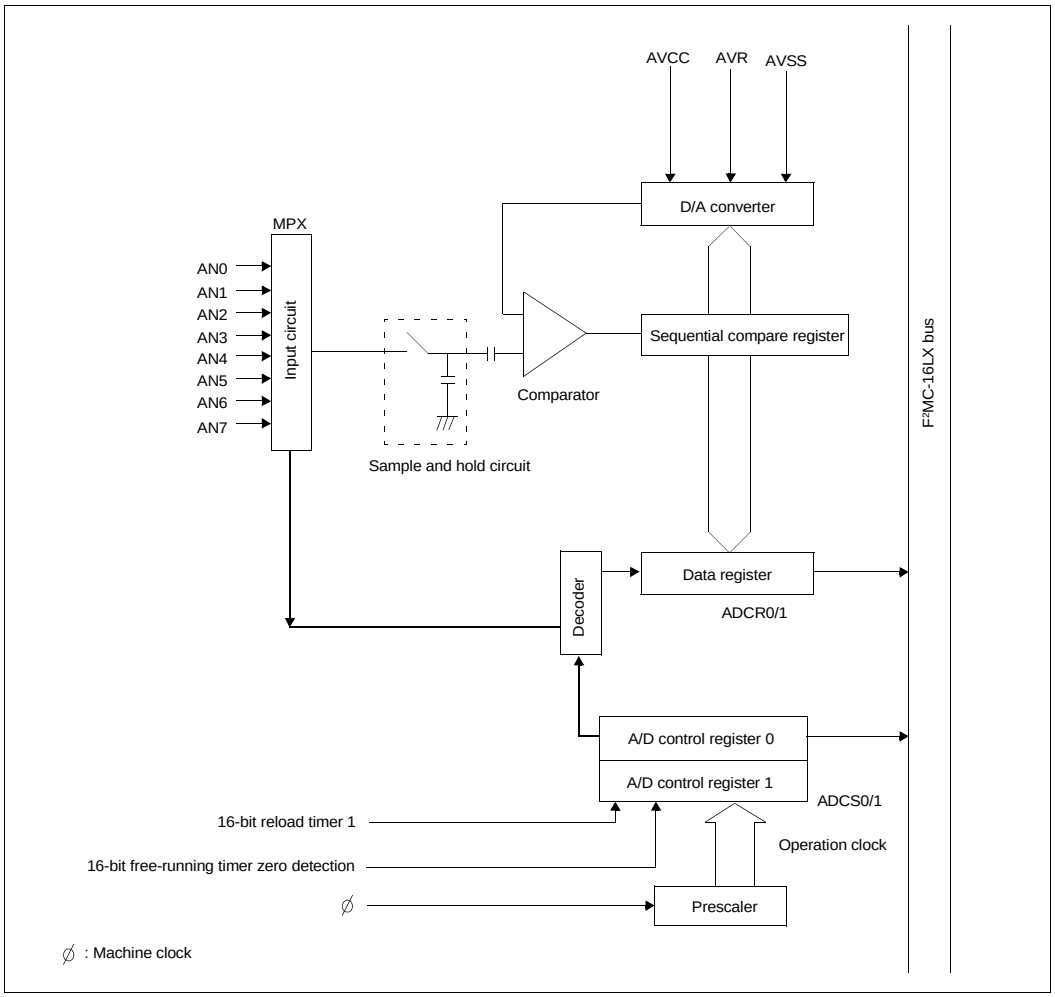
A/D Data Register (upper)

	15	14	13	12	11	10	9	8	
Address: 0000037H	S10	ST1	ST0	CT1	CT0	—	D9	D8	ADCR1
Read/write	R/W	W	W	W	W	—	R	R	
Initial value	0	0	0	0	0	—	X	X	

A/D Data Register (lower)

	7	6	5	4	3	2	1	0	
Address: 000036H	D7	D6	D5	D4	D3	D2	D1	D0	ADCR0
Read/write	R	R	R	R	R	R	R	R	
Initial value	X	X	X	X	X	X	X	X	

(2) Block diagram



14. ROM Correction Function

When an address matches the value set in the address detection register, the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code (01_H). When executing a set instruction, the CPU executes the INT9 instruction. The address match detection function is implemented by processing using the INT9 interrupt routine.

The device contains two address detection registers, each provided with a compare enable bit. When the value set in the address detection register matches an address and the interrupt enable bit is “1”, the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code.

(1) Register configuration

Program Address Detection Control / Status Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 00009E$_H$	—	—	—	—	AD1E	AD1D	AD0E	AD0D	PADCSR
Read/write ⇨	—	—	—	—	R/W	R/W	R/W	R/W	
Initial value ⇨	—	—	—	—	0	0	0	0	

Program Address Detection Register 0 (Upper Byte)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 001FF2$_H$									PADRH0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Program Address Detection Register 0 (Middle Byte)

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 001FF1$_H$									PADRM0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Program Address Detection Register 0 (Lower Byte)

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 001FF0$_H$									PADRL0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

(Continued)

(Continued)

Program Address Detection Register 1 (Upper Byte)

	15	14	13	12	11	10	9	8	
Address: 001FF5H									PADRH1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	

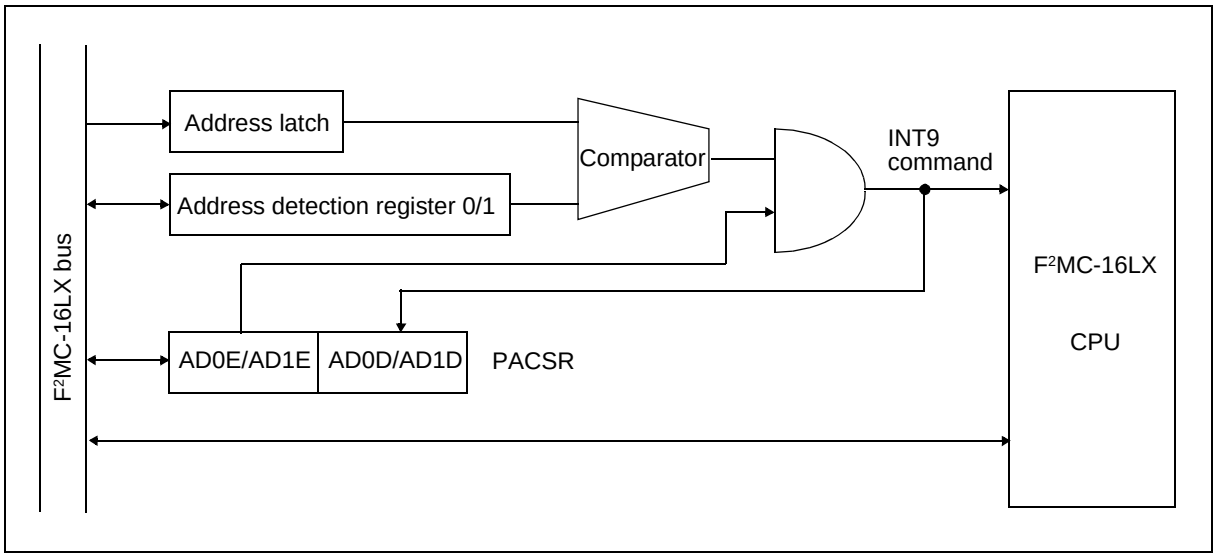
Program Address Detection Register 1 (Middle Byte)

	7	6	5	4	3	2	1	0	
Address: 001FF4H									PADRM1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	

Program Address Detection Register 1 (Lower Byte)

	15	14	13	12	11	10	9	8	
Address: 001FF3H									PADRL1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	

(2) Block diagram



15. ROM Mirroring Function Selection Module

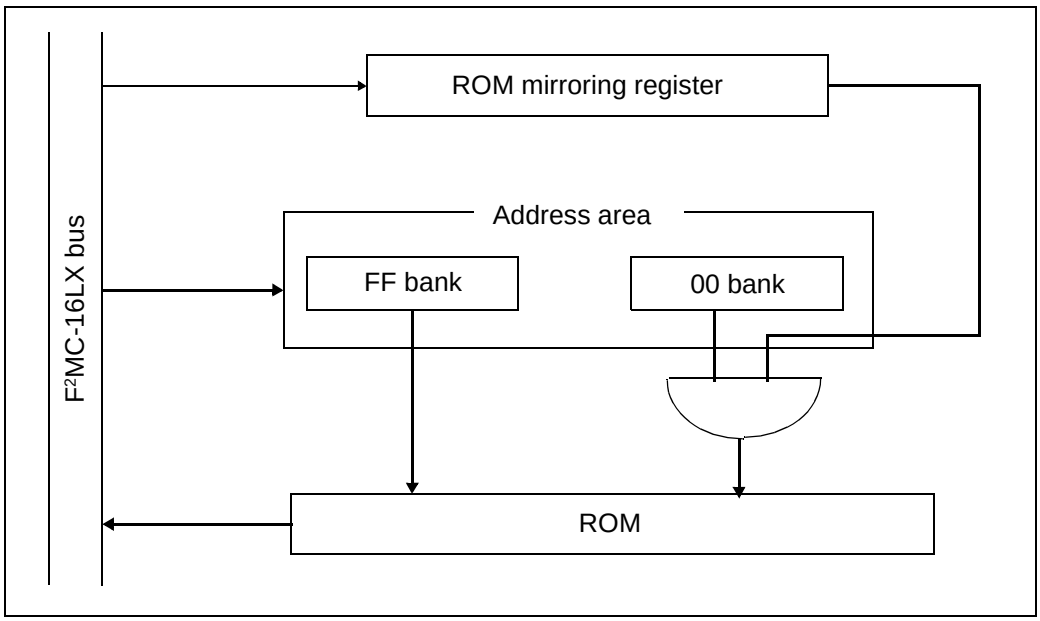
The ROM mirroring function selection module can select what the FF bank allocated the ROM and sees through the 00 bank according to register settings.

(1) Register configuration

ROM Mirror Function Selection Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address : 00006F$_H$	—	—	—	—	—	—	—	M1	ROMM
Read/write ⇨	—	—	—	—	—	—	—	R/W	
Initial value ⇨	—	—	—	—	—	—	—	1	

(2) Block diagram



16. 512/1024 Kbit Flash Memory

The 512 Kbit (MB90F462 and MB90F462A) or 1024 Kbit (MB90F463A) flash memory is allocated in the FE_H to FF_H banks on the CPU memory map. Like masked ROM, flash memory is read-accessible and program-accessible to the CPU using the flash memory interface circuit. The flash memory can be programmed/erased by the instruction from the CPU via the flash memory interface circuit. The flash memory can therefore be reprogrammed (updated) while still on the circuit board under integrated CPU control, allowing program code and data to be improved efficiently.
Note that sector operations such as “enable sector protect” cannot be used.

Features of 512/1024 Kbit flash memory

- 64K words x 8 bits/32K words x 16 bits (16K+8K+8K+32K) sector configuration for MB90F462/F462A
- 128K words x 8 bits/64K words x 16 bits (64K+16K+8K+8K+32K) sector configuration for MB90F463A
- Automatic program algorithm (same as the Embedded Algorithm* : MBM29F400TA)
- Installation of the deletion temporary stop/delete restart function
- Write/delete completion detected by the data polling or toggle bit
- Write/delete completion detected by the CPU interrupt
- Compatibility with the JEDEC standard-type command
- Each sector deletion can be executed (sectors can be freely combined)
- Flash security feature
- Number of write/delete operations 10,000 times guaranteed.

* : Embedded Algorithm is a trademark of Advanced Micro Devices, Inc.

(1) Register configuration

Flash Memory Control Status Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: $0000AE_H$	INTE	RDYINT	WE	RDY	Reserved	LPM1	Reserved	LMP0	FMCS
Read/write ⇨	R/W	R/W	R/W	R	W	R/W	W	R/W	
Initial value ⇨	0	0	0	1	0	0	0	0	

(2) Sector configuration of flash memory

The flash memory has the sector configuration illustrated below. The addresses in the illustration are the upper and lower addresses of each sector.
When 512 Kbit flash memory is accessed from the CPU, SA0 to SA3 are allocated in the FF bank registers.

Flash memory	CPU address	*Writer address
SA3 (16 Kbytes)	$FFFFFF_H$	$7FFFF_H$
	$FFC000_H$	$7C000_H$
SA2 (8 Kbytes)	$FFBFFF_H$	$7BFFF_H$
	$FFA000_H$	$7A000_H$
SA1 (8 Kbytes)	$FF9FFF_H$	$79FFF_H$
	$FF8000_H$	78000_H
SA0 (32 Kbytes)	$FF7FFF_H$	$77FFF_H$
	$FF0000_H$	70000_H

When 1024 Kbit flash memory is accessed from the CPU, SA0 and SA1 to SA4 are allocated in the FE and FF bank registers, respectively.

Flash memory	CPU address	*Writer address
SA4 (16 Kbytes)	$FFFFFF_H$	$7FFFF_H$
	$FFC000_H$	$7C000_H$
SA3 (8 Kbytes)	$FFBFFF_H$	$7BFFF_H$
	$FFA000_H$	$7A000_H$
SA2 (8 Kbytes)	$FF9FFF_H$	$79FFF_H$
	$FF8000_H$	78000_H
SA1 (32 Kbytes)	$FF7FFF_H$	$77FFF_H$
	$FF0000_H$	70000_H
SA0 (64 Kbytes)	$FEFFFF_H$	$6FFFF_H$
	$FE0000_H$	60000_H

* : Programmer addresses correspond to CPU addresses when data is programmed in flash memory by a parallel programmer. Programmer addresses are used to program/erase data using a general-purpose programmer.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} \geq AV_{CC}$ *1
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$, $AVR \geq AV_{ss}$
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
“L” level maximum output current	I_{OL}	—	15	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	Average output current = operating current × operating efficiency
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Average output current = operating current × operating efficiency
“H” level maximum output current	I_{OH}	—	–15	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	Average output current = operating current × operating efficiency
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Average output current = operating current × operating efficiency
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : AV_{CC} shall never exceed V_{CC} when power-on.

*2 : V_I and V_O shall never exceed V_{CC} + 0.3 V.

*3 : The maximum output current is a peak value for a corresponding pin.

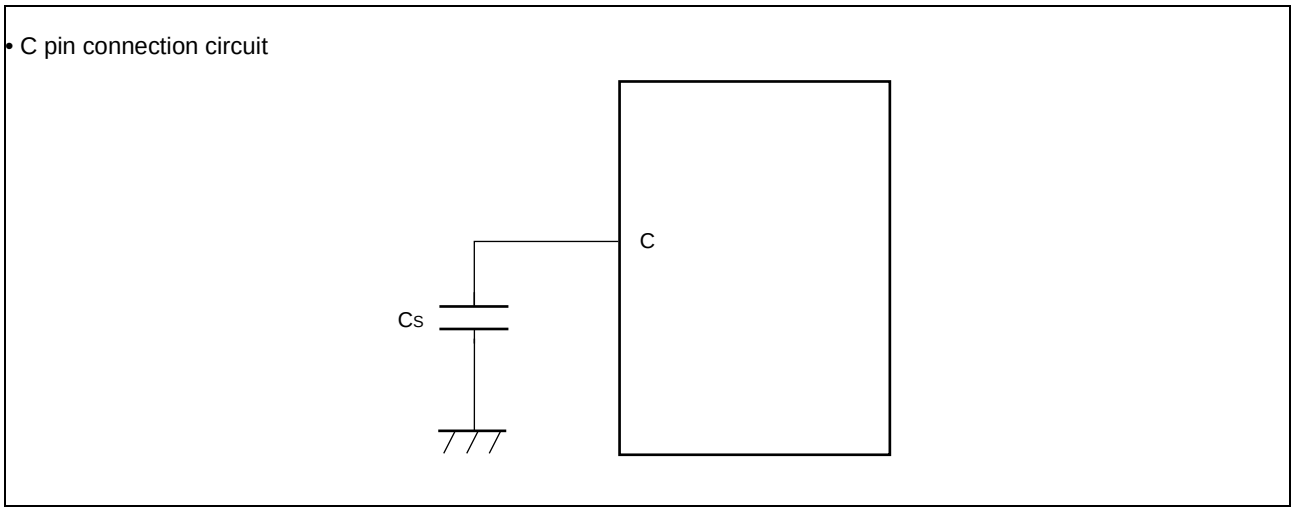
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	5.5	V	Normal operation (MB90462, MB90467, MB90V460)
		4.5	5.5	V	Normal operation (MB90F462, MB90F462A, MB90F463A))
	V_{CC}	3.0	5.5	V	Retains status at the time of operation stop
Smoothing capacitor	C_S	0.1	1.0	µF	Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.
Operating temperature	T_A	–40	+85	°C	

• C pin connection circuit



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	All pins except P00 ~ P05 and P30 ~ P35	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P00 ~ P05 P30 ~ P35	V_{CC} = 4.5 V, I_{OL2} = 12.0 mA	—	—	0.4	V	
"H" level input voltage	V_{IH}	P00 ~ P07 P30 ~ P37 P50 ~ P57	V_{CC} = 3.0V ~ 5.5V (MB90462, MB90467) V_{CC} = 4.5V ~ 5.5V (MB90F462, MB90F462A, MB90F463A)	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS}	P10 ~ P17 P20 ~ P27 P40 ~ P46 P60 ~ P63 $\overline{RST}$		0.8 V_{CC}	—	V_{CC} + 0.3	V	CMOS hysteresis input pin
	V_{IHM}	MD0 ~ 2		V_{CC} – 0.3	—	V_{CC} + 0.3	V	Mode input pin
"L" level input voltage	V_{IL}	P00 ~ P07 P30 ~ P37 P50 ~ P57		V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	P10 ~ P17 P20 ~ P27 P40 ~ P46 P60 ~ P63 $\overline{RST}$		V_{SS} – 0.3	—	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	MD0 ~ 2		V_{SS} – 0.3	—	V_{SS} + 0.3	V	Mode pin input
Input leakage current	I_{IL}	All input pins	V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal operation at 16 MHz, Normal operation	—	40	50	mA	MB90462, MB90467
				—	30	50	mA	MB90F462, MB90F462A, MB90F463A
			V_{CC} = 5.0 V, Internal operation at 16 MHz, When data is written in flash mode (erasing or programming)	—	45	60	mA	MB90F462, MB90F462A, MB90F463A
	I_{CCS}		V_{CC} = 5.0 V, Internal operation at 16 MHz, In sleep mode	—	15	25	mA	MB90462, MB90467, MB90F462, MB90F462A, MB90F463A
Power supply current*	I_{CCT}	V_{CC}	V_{CC} = 5.0 V, Internal operation at 16 MHz, In timer mode, T_A = 25 °C	—	2.5	5.0	mA	MB90462, MB90467, MB90F462, MB90F462A, MB90F463A
	I_{CCH}		In stop mode, T_A = 25 °C	—	5	20	µA	MB90462, MB90467, MB90F462, MB90F462A, MB90F463A
Input capacitance	C_{IN}	Except AV_{CC}, AV_{SS}, C, V_{CC} and V_{SS}	—	—	10	80	pF	
Pull-up resistance	R_{UP}	P00 to P07 P10 to P17 $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

* : The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice. The power supply current is measured with an external clock.

4. AC Characteristics

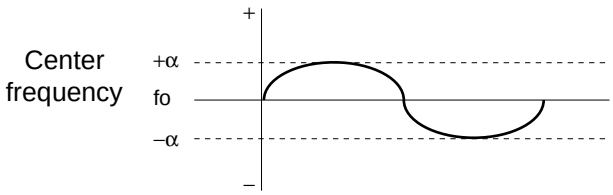
(1) Clock Timings

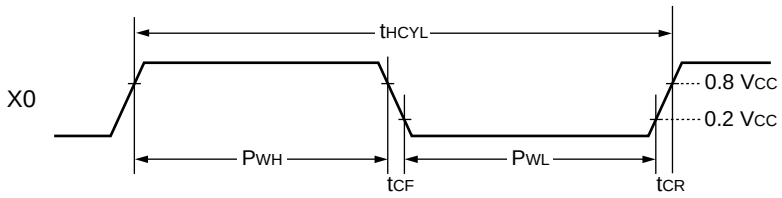
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	f_C	X0, X1	—	3	—	16	MHz	
Clock cycle time	t_{HCYL}	X0, X1	—	62.5	—	333	ns	
Frequency fluctuation rate	Δf	—	—	—	—	5	%	
Input clock pulse width	P_{WH} P_{WL}	X0	—	10	—	—	ns	Recommened duty ratio of 30% to 70%
Input clock rise / fall time	t_{CR} t_{CF}	X0	—	—	—	5	ns	External clock operation
Internal operating	f_{CP}	—	—	1.5	—	16	MHz	Main clock operation
Internal operating clock cycle time	t_{CP}	—	—	62.5	—	666	ns	Main clock operation

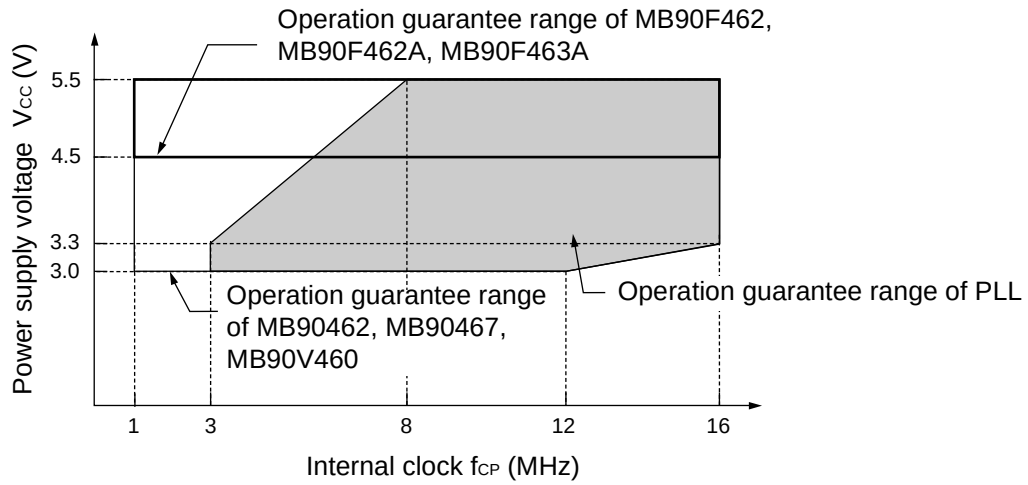
*: The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

$$\Delta f = \frac{|\alpha|}{fo} \times 100\ (\%)$$

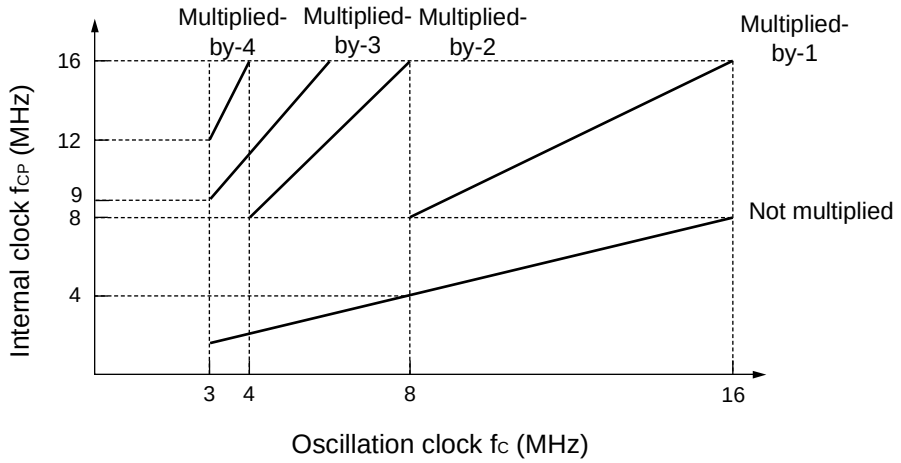




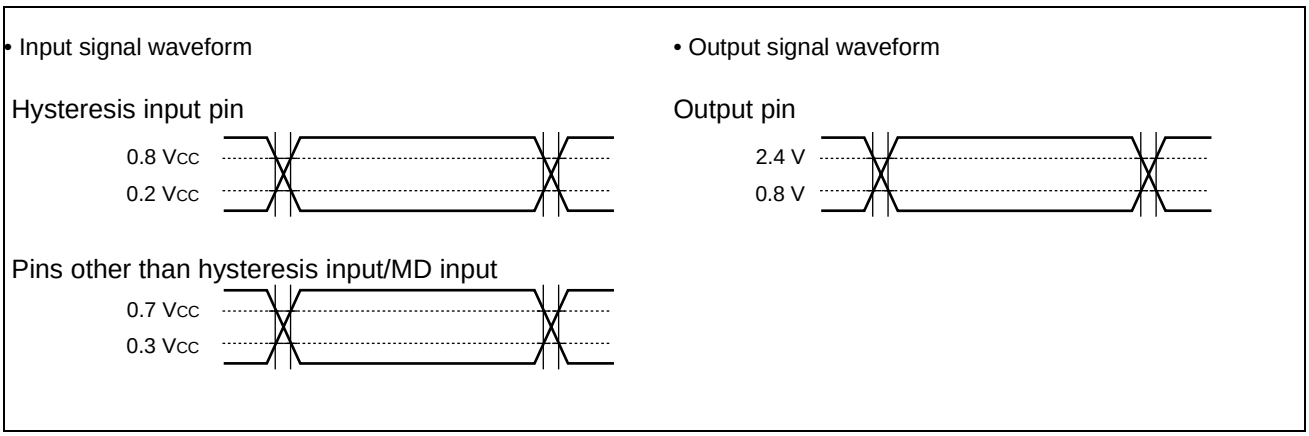
Relationship between internal operating clock frequency and power supply voltage



Relationship between oscillating frequency and internal operating clock frequency



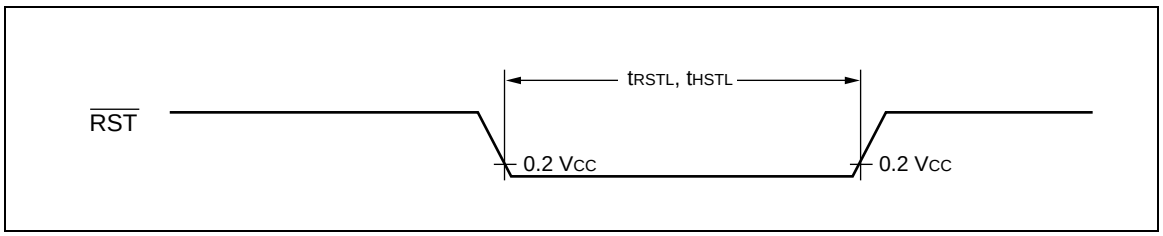
The AC ratings are measured for the following measurement reference voltages



(2) Reset Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	4 t_{CP}	—	ns	



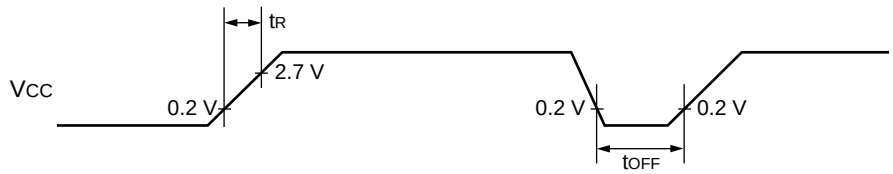
(3) Power-on Reset

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

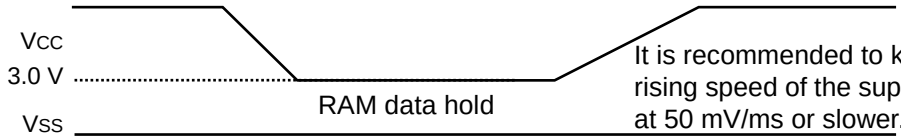
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	
Power supply cut-off time	t_{OFF}	V_{CC}		4	—	ms	Due to repeated operations

* : V_{CC} must be kept lower than 0.2 V before power-on.

Note The above values are used for causing a power-on reset.
Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

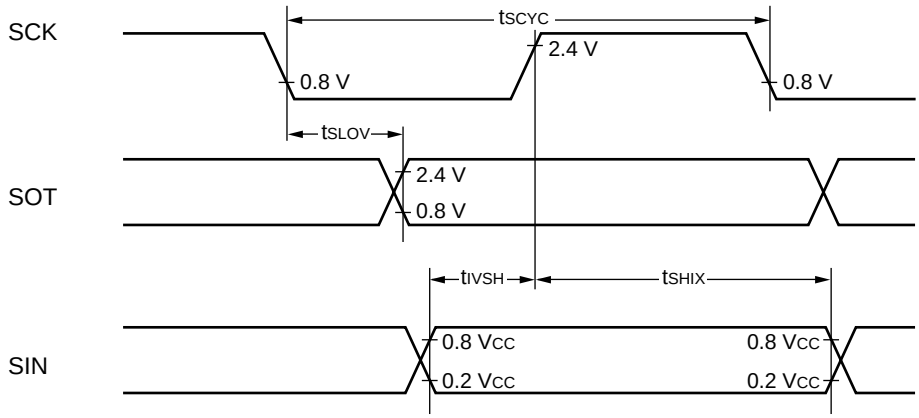
(4) UART0 to UART1

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

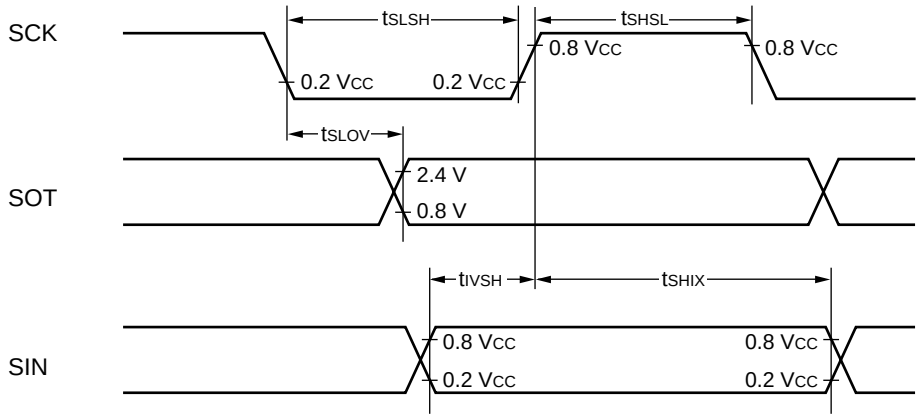
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK1	C_L = 80 pF + 1 TTL for an output pin of internal shift clock mode	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK1 SOT0 to SOT1		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK1 SIN0 to SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK1	C_L = 80 pF + 1 TTL for an output pin of external shift clock mode	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK1		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK1 SOT0 to SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns	

Note : • These are AC ratings in the CLK synchronous mode.
• CL is the load capacitance value connected to pins while testing.
• t_{CP} is machine cycle time (unit:ns).

• Internal shift clock mode



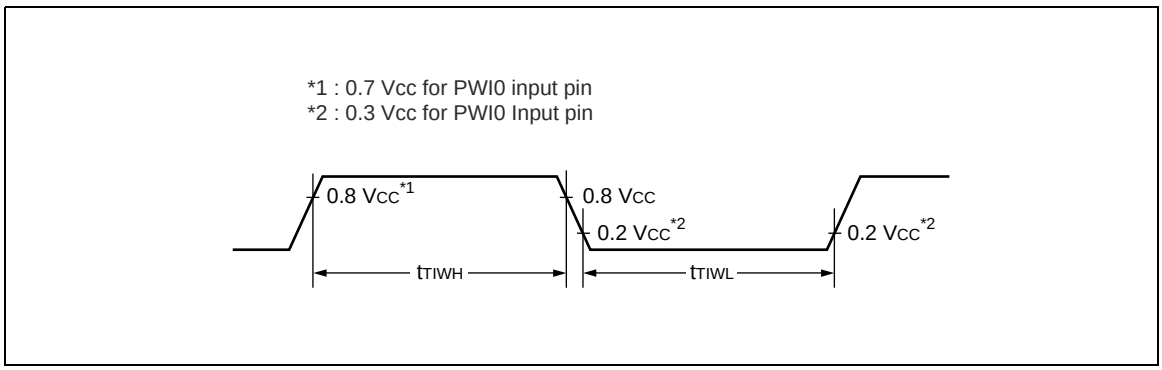
• External shift clock mode



(5) Resources Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

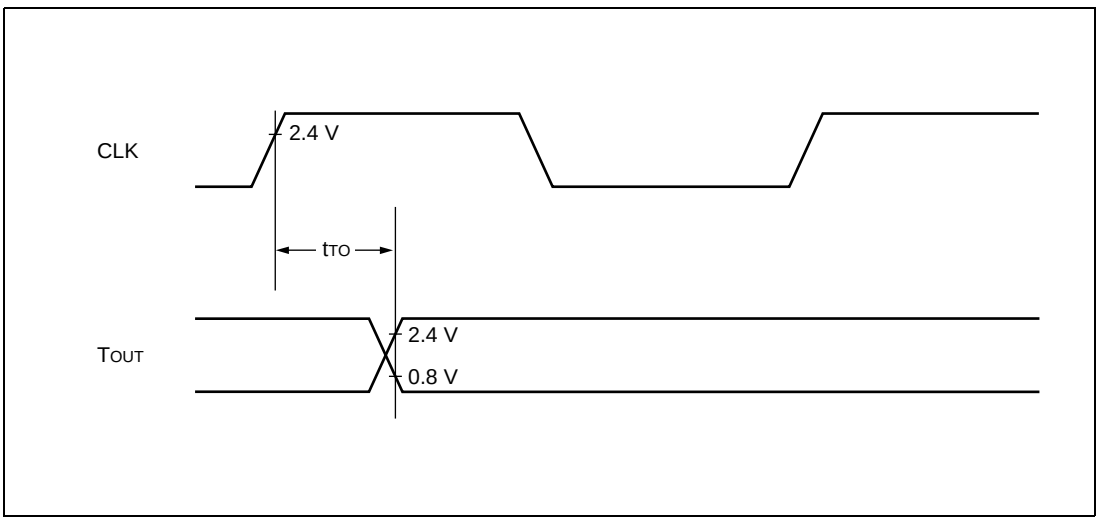
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	IN0 to IN3 SNI0 to SNI3 TIN0 to TIN1 PWI0 to PWI1 DTTI0, DTTI1	—	4 t_{CP}	—	ns	



(6) Resources Output Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

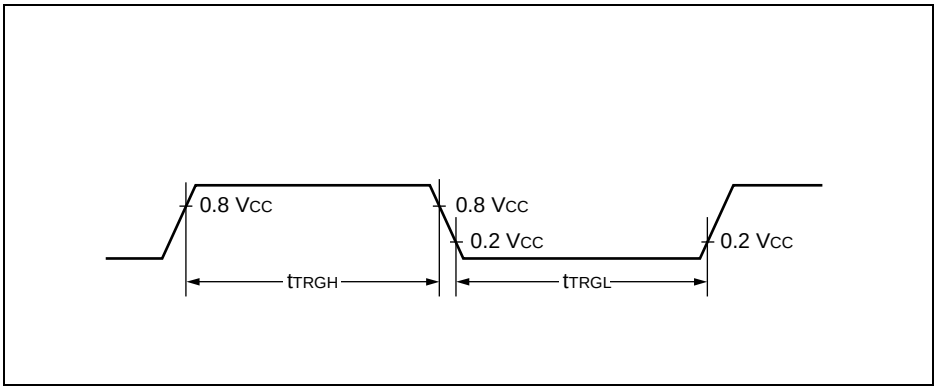
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK↑→T_{OUT} transition time	t_{TO}	PWO0 to PWO1 PPG0 to PPG2 TO0 to TO1	—	30	—	ns	



(8) Trigger Input Timimg

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7	—	5 t_{CP}	—	ns	



5. A/D Converter Electrical Characteristics

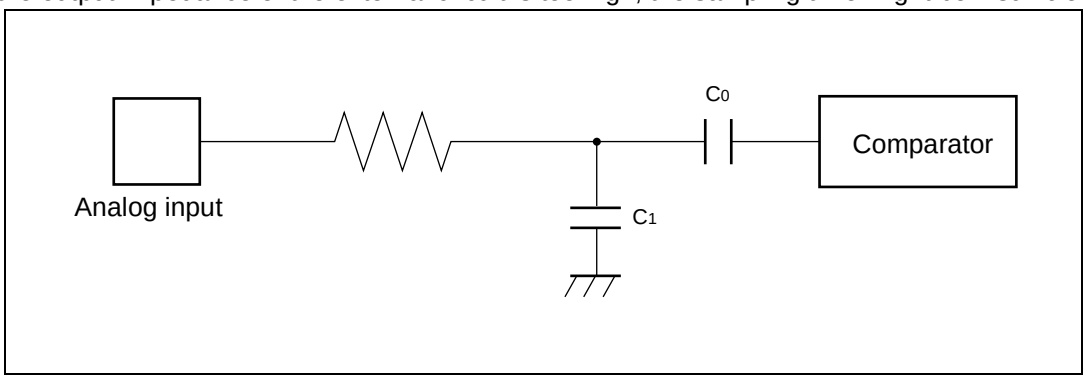
(3.0 V ≤ AVR – AV_{SS}, V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	—	bit	
Total error	—	—	—	—	±3.0	LSB	For MB90F462, MB90F462A, MB90F463A, MB90462, MB90467
	—	—	—	—	±5.0	LSB	For MB90V460
Non-linear error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	For MB90F462, MB90F462A, MB90F463A, MB90462, MB90467
			AV_{SS} – 3.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 4.5 LSB	mV	For MB90V460
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV	For MB90F462, MB90F462A, MB90F463A, MB90462, MB90467
			AVR – 6.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	For MB90V460
Conversion time	—	—	6.125	—	1000	µs	For MB90V460, MB90F462, MB90F462A, MB90F463A, MB90467. Actual value is specified as a sum of values specified in ADCR0 : CT1, CT0 and ADCR0 : ST1, ST0. Be sure that the setting value is greater than the min value
Sampling period	—	—	2	—	—	µs	Actual value is specified in ADCR0 : ST1, ST0 bits. Be sure that the setting value is greater than the min value
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.3	6	mA	For MB90F462, MB90F462A, MB90F463A, MB90462, MB90467
				2	5	mA	For MB90V460
	I_{AH}*		—	—	5	µA	*

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Reference voltage supply current	I_R	AVR	—	140	260	µA	For MB90F462, MB90462, MB90467
			—	600	900	µA	For MB90F462A, MB90F463A
			—	0.9	1.3	mA	For MB90V460
	I_{RH}*		—	—	5	µA	*
Offset between channels	—	AN0 to AN7	—	—	4	LSB	

* : The current when the A/D converter is not operating or the CPU is in stop mode (for V_{CC} = AV_{CC} = AVR = 5.0 V)

Note: • The error increases proportionally as |AVR - AV_{SS}| decreases.
- The output impedance of the external circuits connected to the analog inputs should be in the following range.
- The output impedance of the external circuit : TBD
- If the output impedance of the external circuit is too high, the sampling time might be insufficient.



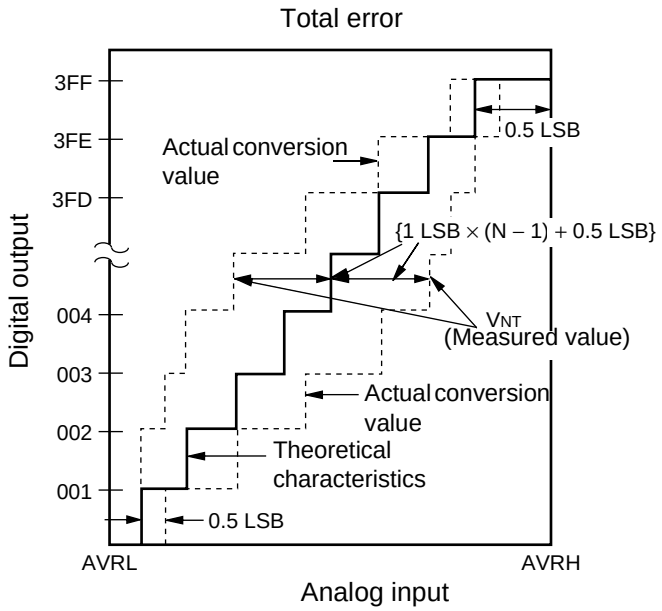
6. A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Theoretical value})\ \frac{AVR - AVss}{1024}\ [\text{V}]$$

V_{OT}(Theoretical value) = AVss + 0.5 LSB [V]

V_{FST}(Theoretical value) = AVR − 1.5 LSB [V]

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

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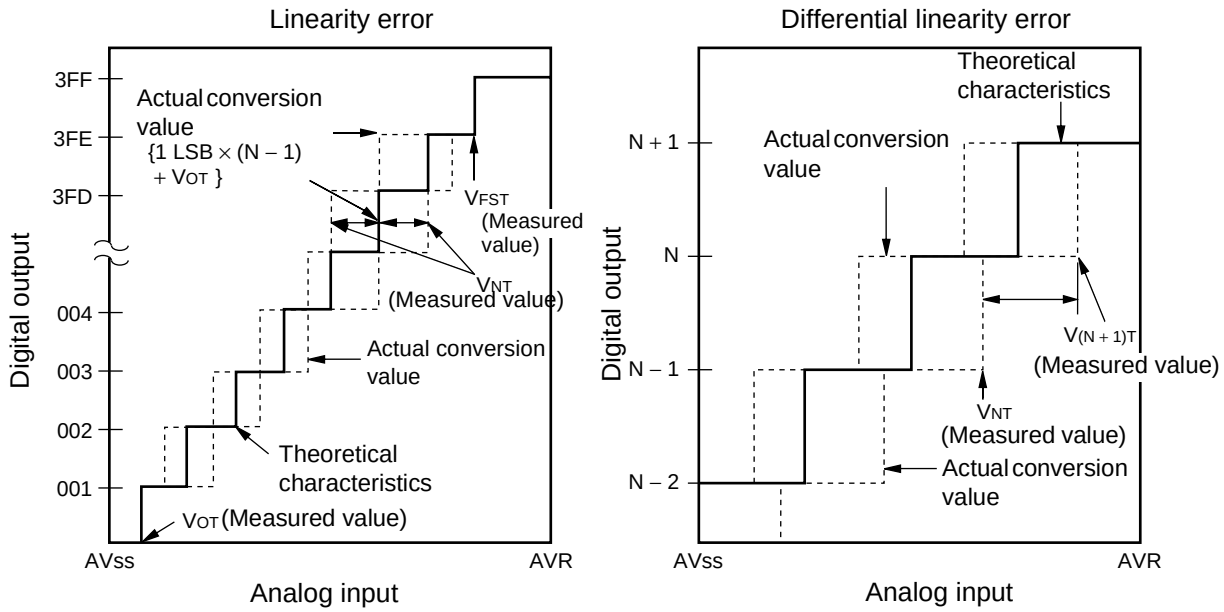


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from “000_H” to “001_H”
V_{FST} : Voltage at transition of digital output from “$3FE_H$” to “$3FF_H$”

7. Notes on Using A/D Converter

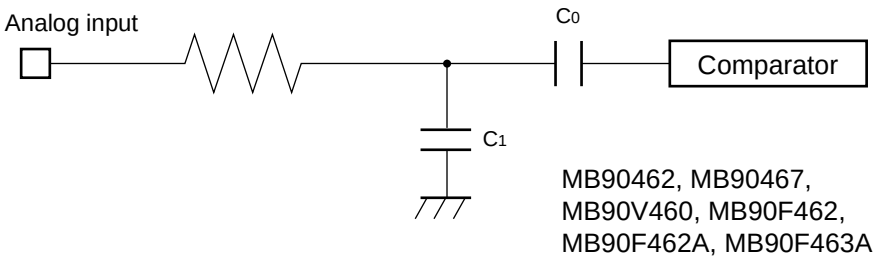
Select the output impedance value for the external circuit of analog input according to the following conditions.

Output impedance values of the external circuit of 5 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 µs @ machine clock of 16 MHz).

• Equipment of analog input circuit model



MB90462, MB90467, MB90V460, MB90F462, MB90F462A, MB90F463A	R ≅ 2.6 kΩ, C ≅ 30 pF
	R ≅ 3.2 kΩ, C ≅ 28 pF

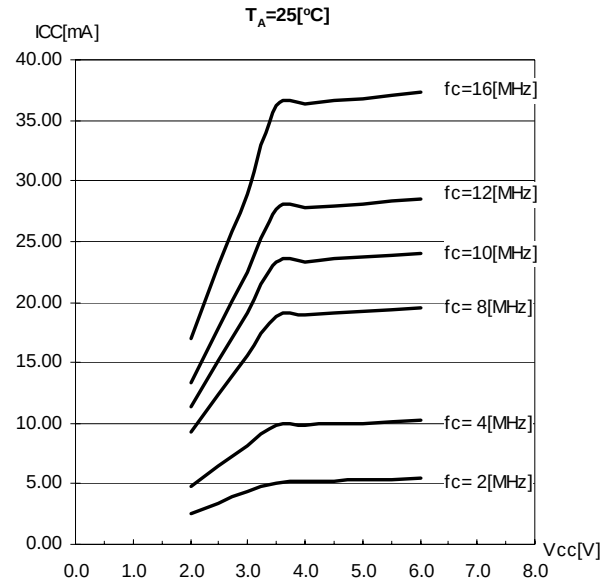
Note: Listed values must be considered as standards.

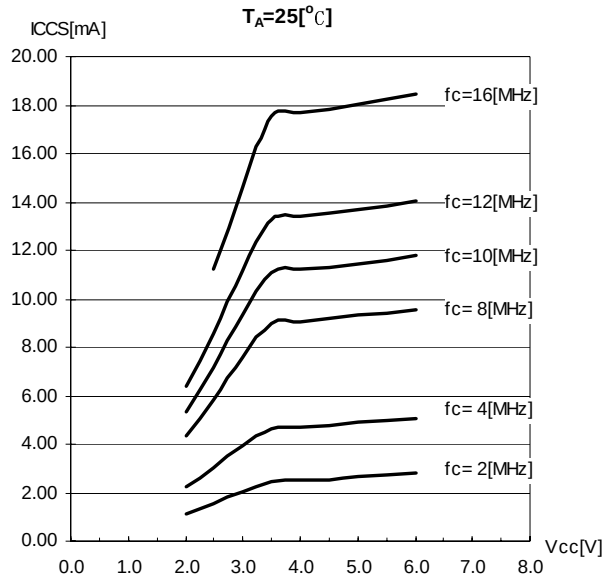
• Error

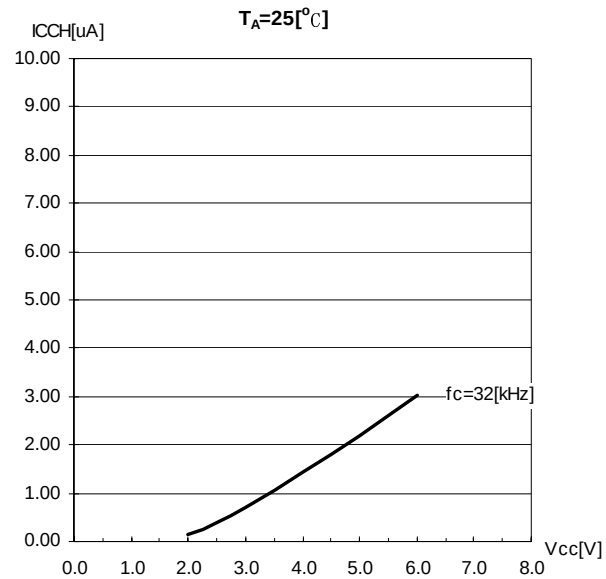
The smaller the | AVR - AV_{SS} |, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

• Power suppy current of MB90462/467







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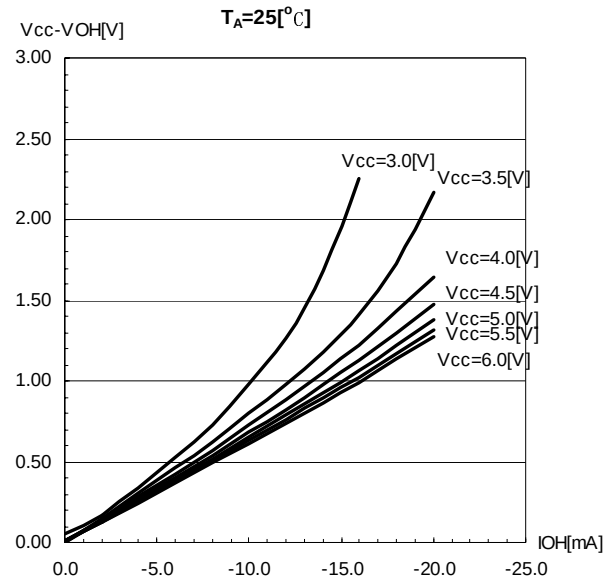
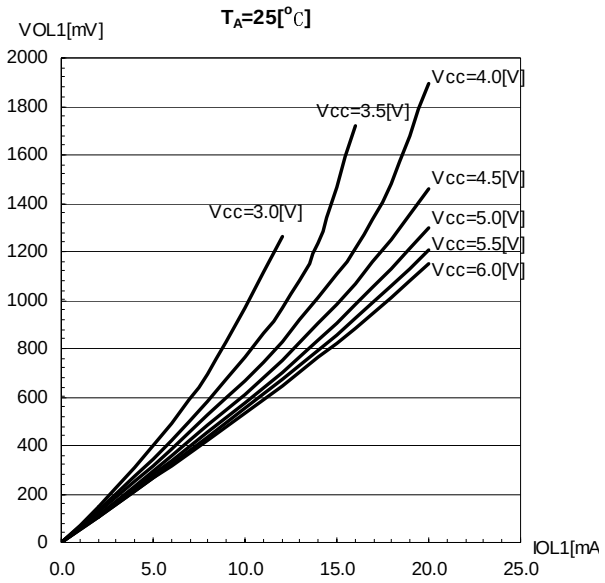
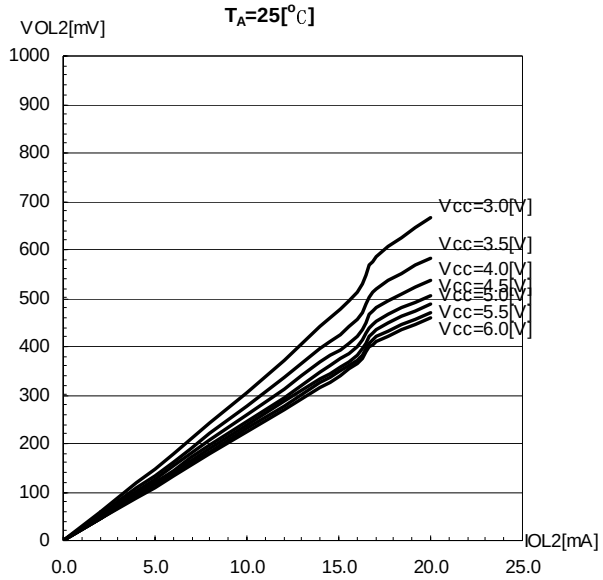
• Output voltage of MB90462/467







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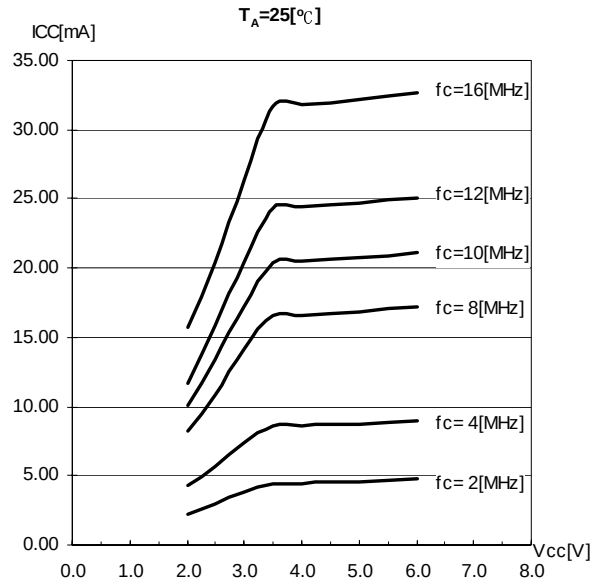
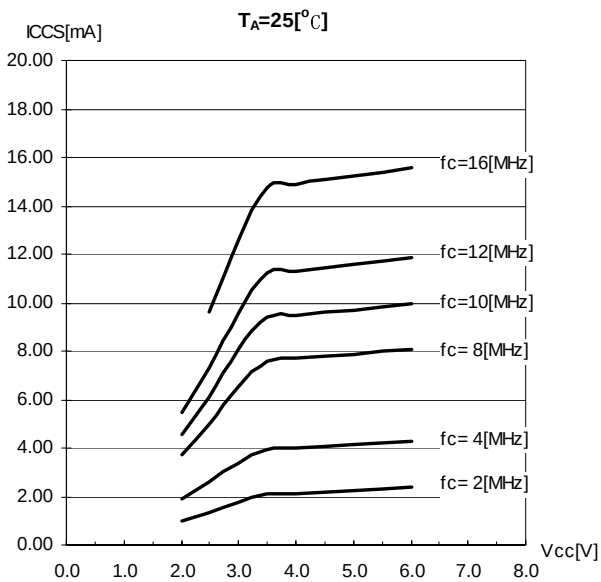
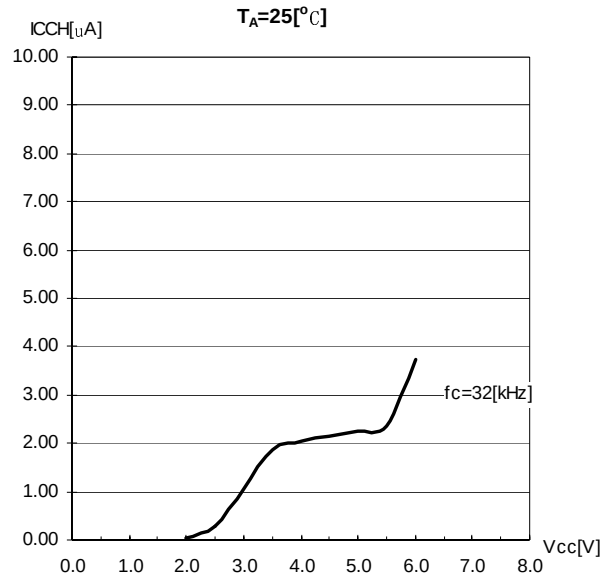
• Power suppy current of MB90F462







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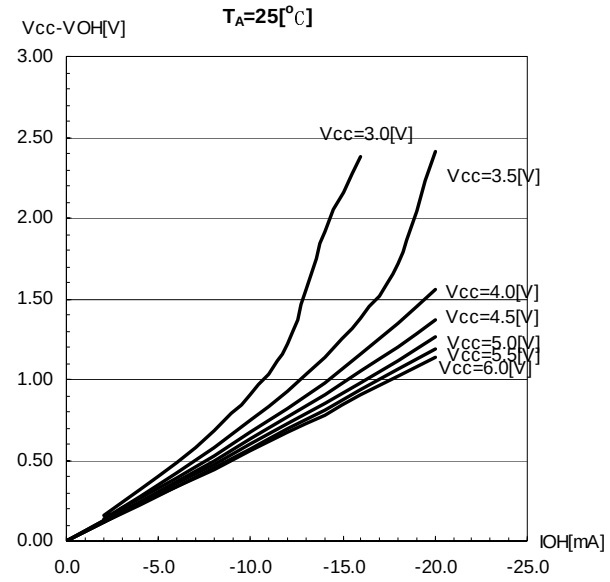
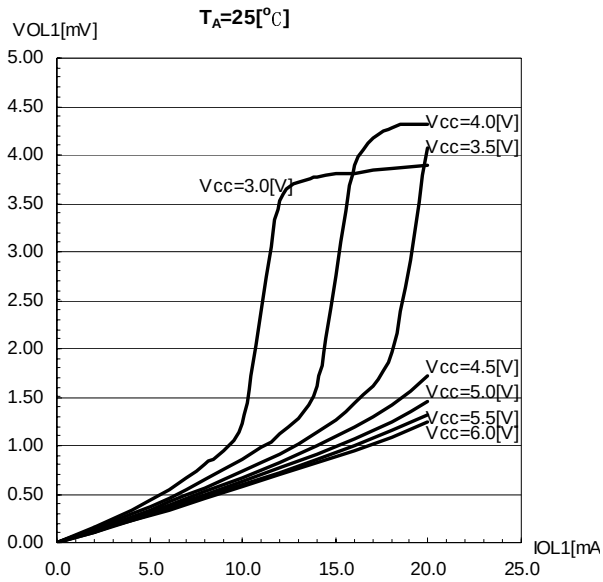
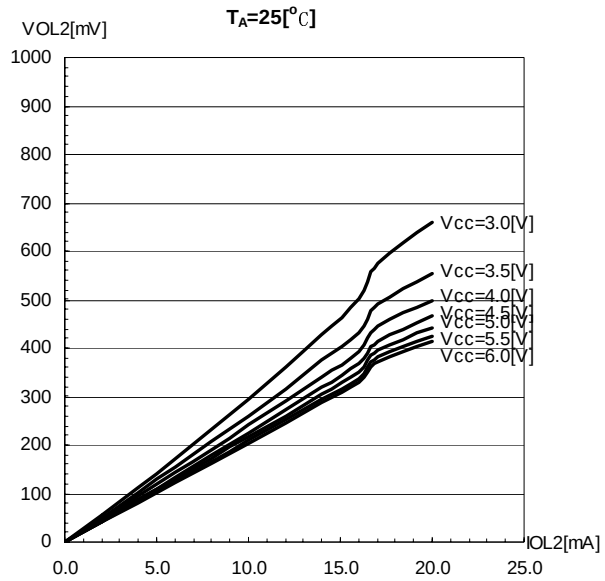
• Output voltage of MB90F462







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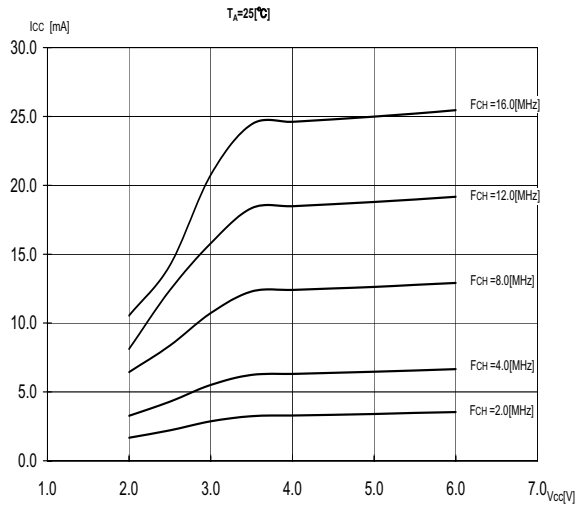
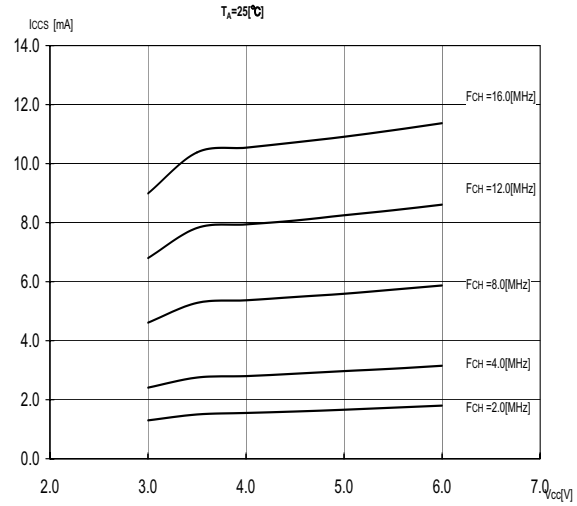
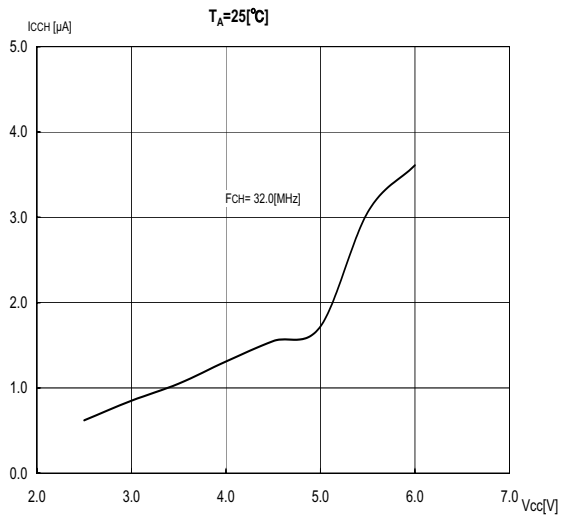
• Power supply current of MB90F462A/F463A







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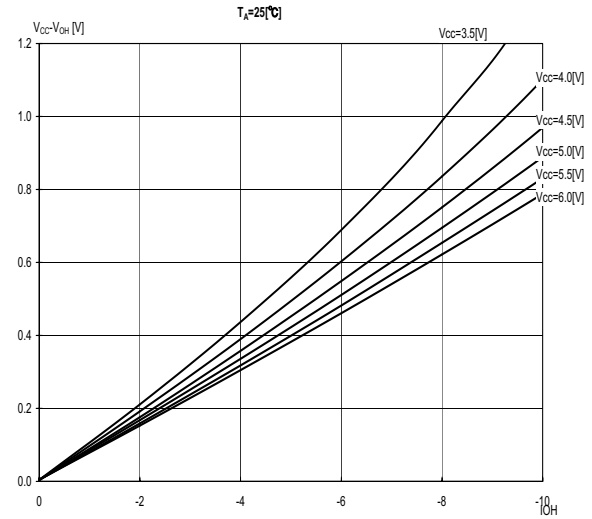
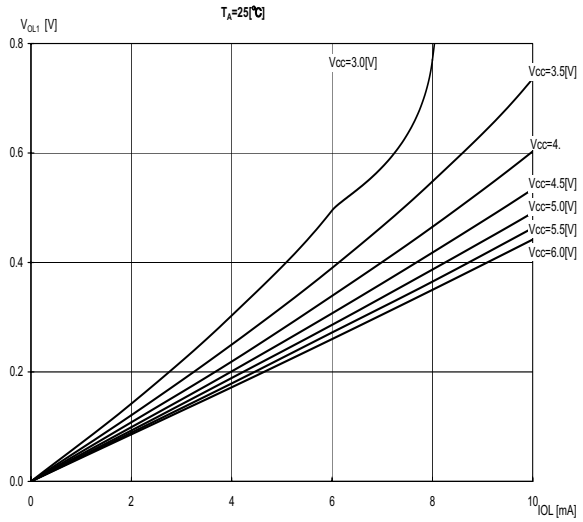
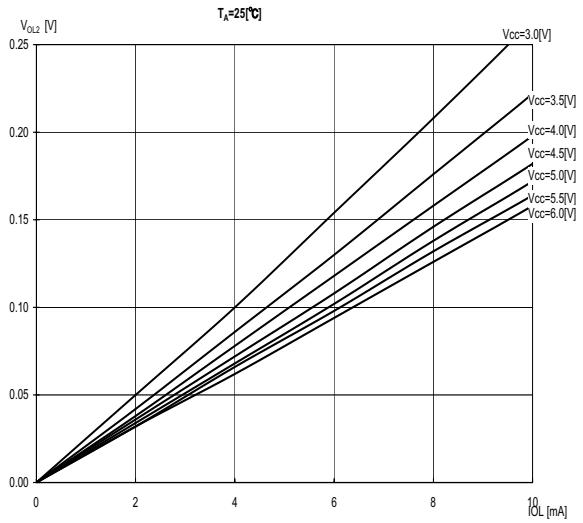
• Output voltage of MB90F462A/F463A







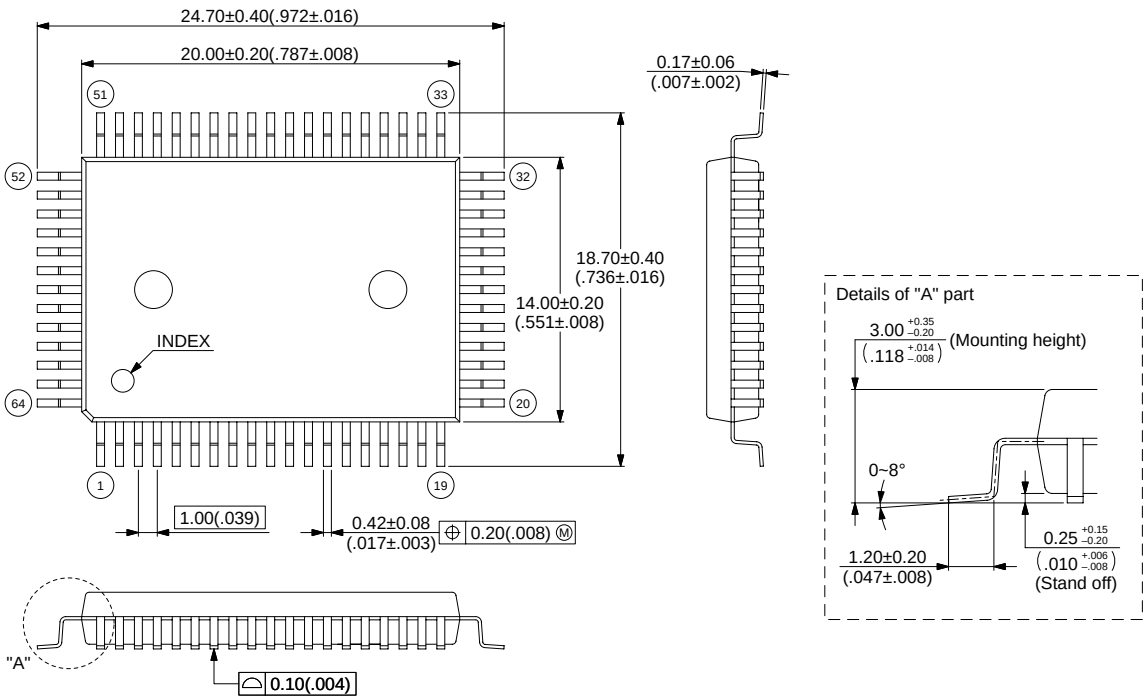
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F462PFM-G MB90F462APFM-G MB90F463APFM-G MB90462PFM-G-XXX MB90467PFM-G-XXX	64-pin Plastic LQFP (FPT-64P-M09)	
MB90F462PF-G MB90F462APF-G MB90F463APF-G MB90462PF-G-XXX MB90467PF-G-XXX	64-pin Plastic QFP (FPT-64P-M06)	
MB90F462P-G-SH MB90F462AP-G-SH MB90F463AP-G-SH MB90462P-G-XXX-SH MB90467P-G-XXX-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	

Note : XXX is the internal reference number for ROM code release.

■ PACKAGE DIMENSIONS

64-pin plastic QFP
(FPT-64P-M06)

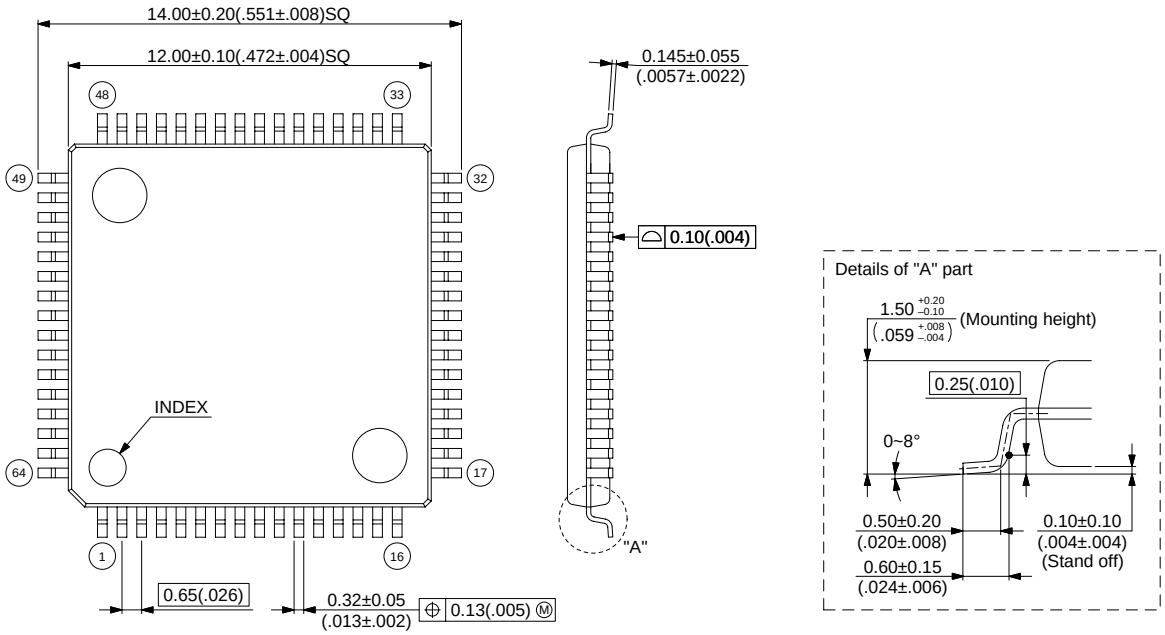


Dimensions in mm (inches)

(Continued)

(Continued)

64-pin plastic LQFP
(FPT-64P-M09)

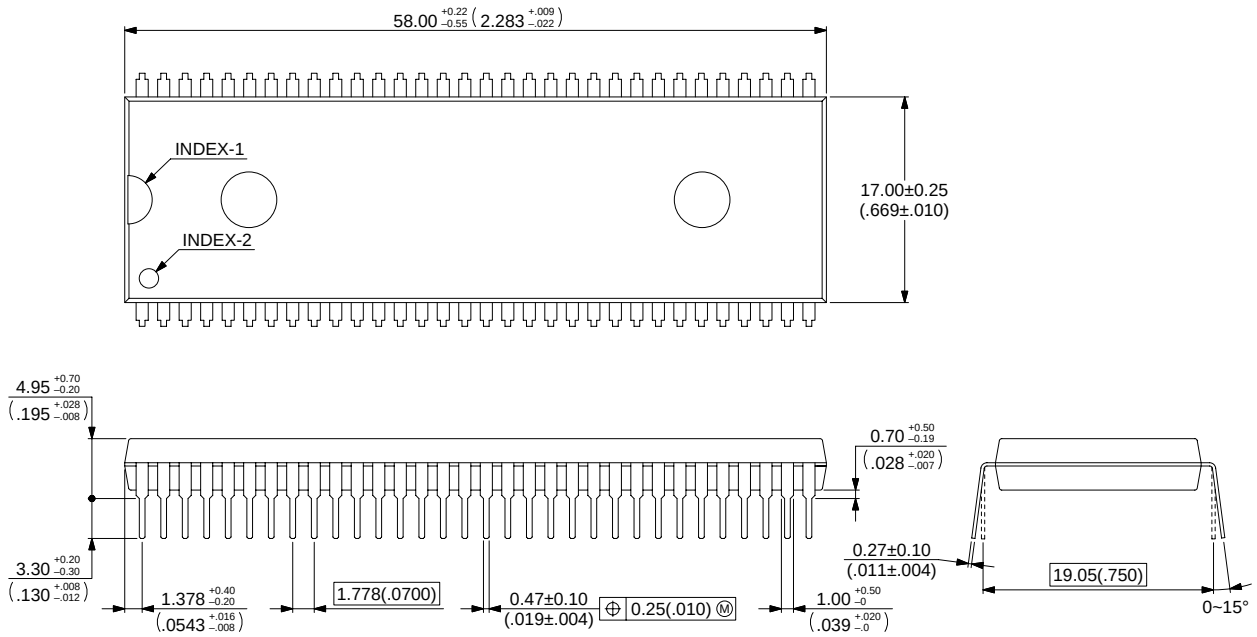


Dimensions in mm (inches)

(Continued)

(Continued)

64-pin plastic SH-DIP
(DIP-64P-M01)



Dimensions in mm (inches)

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