



# Multirate Clock and Data Recovery with Limiting Amplifier

MAX3872

## General Description

The MAX3872 is a compact, multirate clock and data recovery with limiting amplifier for OC-3, OC-12, OC-24, OC-48, OC-48 with FEC SONET/SDH and Gigabit Ethernet (1.25Gbps/2.5Gbps) applications. Without using an external reference clock, the fully integrated phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input. The input data is then retimed by the recovered clock, providing a clean data output. An additional serial input (SLBI±) is available for system loopback diagnostic testing. Alternatively, this input can be connected to a reference clock to maintain a valid clock output in the absence of data transitions. The device also includes a loss-of-lock (LOL) output.

The MAX3872 contains a vertical threshold control to compensate for optical noise due to EDFAs in DWDM transmission systems. The recovered data and clock outputs are CML with on-chip 50Ω back termination on each line. Its jitter performance exceeds all SONET/SDH specifications.

The MAX3872 operates from a single +3.3V supply and typically consumes 580mW. It is available in a 5mm x 5mm 32-pin thin QFN with exposed-pad package and operates over a -40°C to +85°C temperature range.

## Applications

- SONET/SDH Receivers and Regenerators
- Add/Drop Multiplexers
- Digital Cross-Connects
- SONET/SDH Test Equipment
- DWDM Transmission Systems
- Access Networks

Pin Configuration appears at end of data sheet.

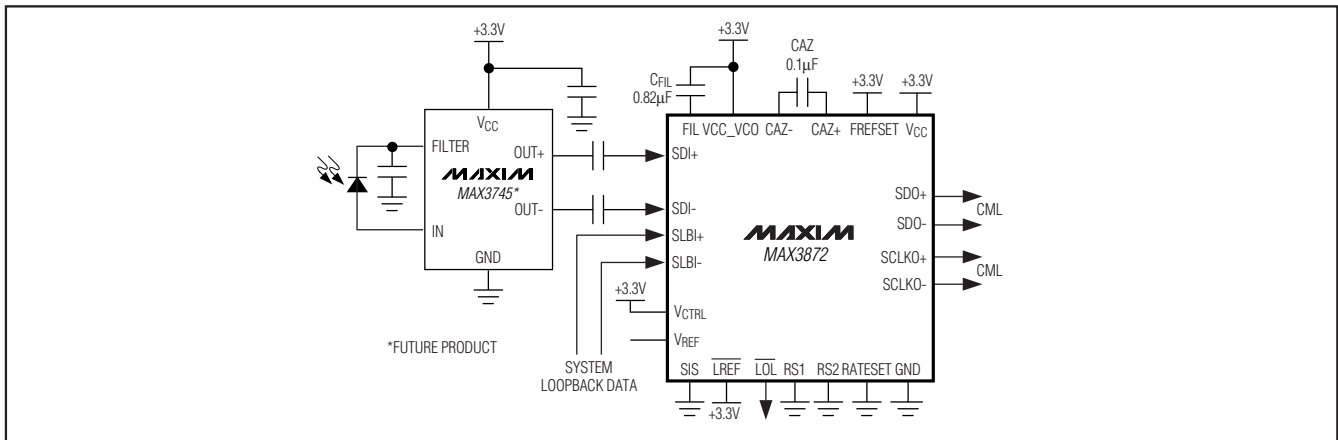
## Features

- ◆ Multirate Data Input: 2.667Gbps (FEC), 2.488Gbps, 1.244Gbps, 622.08Mbps, 155.52Mbps, 1.25Gbps/2.5Gbps (Ethernet)
- ◆ Reference Clock Not Required for Data Acquisition
- ◆ Exceeds ANSI, ITU, and Bellcore SONET/SDH Jitter Specifications
- ◆ 2.7mUI<sub>RMS</sub> Jitter Generation
- ◆ 10mV<sub>p-p</sub> Input Sensitivity Without Threshold Adjust
- ◆ 0.65UI<sub>p-p</sub> High-Frequency Jitter Tolerance
- ◆ ±170mV Input Threshold Adjust Range
- ◆ Clock Holdover Capability Using Frequency-Selectable Reference Clock
- ◆ Serial Loopback Input Available for System Diagnostic Testing
- ◆ Loss-of-Lock (LOL) Indicator

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3872EGJ	-40°C to +85°C	32 QFN	G3255-1

## Typical Application Circuit



# Multirate Clock and Data Recovery with Limiting Amplifier

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$ .....	-0.5V to +5.0V
Input Voltage Levels (SDI+, SDI-, SLBI+, SLBI-) .....	( $V_{CC} - 1.0V$ ) to ( $V_{CC} + 0.5V$ )
Input Current Levels (SDI+, SDI-, SLBI+, SLBI-).....	$\pm 20mA$
CML Output Current (SDO+, SDO-, SCLKO+, SCLKO-) .....	$\pm 22mA$
Voltage at LOL, LREF, SIS, FIL, RATESET, FREFSET, RS1, RS2, VCTRL, VREF, CAZ+, CAZ-.....	-0.5V to ( $V_{CC} + 0.5V$ )

Continuous Power Dissipation ( $T_A = +85^\circ C$ ) 32-Pin QFN (derate 21.3mW/ $^\circ C$ above +85 $^\circ C$ ) .....	1384mW
Operating Junction Temperature Range .....	-55 $^\circ C$ to +150 $^\circ C$
Storage Temperature Range .....	-55 $^\circ C$ to +150 $^\circ C$
Processing Temperature (die) .....	+400 $^\circ C$
Lead Temperature (soldering, 10s) .....	+300 $^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to +3.6V,  $T_A = -40^\circ C$  to +85 $^\circ C$ . Typical values at  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$I_{CC}$	(Note 2)		175	215	mA
<b>INPUT SPECIFICATIONS (SDI<math>\pm</math>, SLBI<math>\pm</math>)</b>						
Single-Ended Input Voltage Range	$V_{IS}$	Figure 1	$V_{CC} - 0.8$		$V_{CC} + 0.4$	V
Input Common-Mode Voltage		Figure 1	$V_{CC} - 0.4$		$V_{CC}$	V
Input Termination to $V_{CC}$	$R_{IN}$		42.5	50	57.5	$\Omega$
<b>THRESHOLD-SETTING SPECIFICATIONS (SDI<math>\pm</math>)</b>						
Differential Input Voltage Range (SDI $\pm$ )		Threshold adjust enabled	50		600	mV <sub>P-P</sub>
Threshold Adjustment Range	$V_{TH}$	Figure 2	-170		+170	mV
Threshold Control Voltage	$V_{CTRL}$	Figure 2 (Note 3)	0.3		2.1	V
Threshold Control Linearity				$\pm 5$		%
Threshold Setting Accuracy		Figure 2	-18		+18	mV
Threshold Setting Stability		$15mV \leq  V_{TH}  \leq 80mV$	-6		+6	mV
		$80mV <  V_{TH}  \leq 170mV$	-12		+12	
Maximum Input Current	$I_{CTRL}$		-10		+10	$\mu A$
Reference Voltage Output	$V_{REF}$		2.14	2.2	2.24	V
<b>CML OUTPUT SPECIFICATIONS (SDO<math>\pm</math>, SCLKO<math>\pm</math>)</b>						
CML Differential Output Swing		(Note 4)	600	800	1000	mV <sub>P-P</sub>
CML Differential Output Impedance	$R_O$		85	100	115	$\Omega$
CML Output Common-Mode Voltage		(Note 4)		$V_{CC} - 0.2$		V

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## DC ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = +3.0V to +3.6V, T<sub>A</sub> = -40°C to +85°C. Typical values at V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LVTTTL INPUT/OUTPUT SPECIFICATIONS (L<sub>OL</sub>, L<sub>REF</sub>, RATESET, RS1, RS2, FREFSET)</b>						
LVTTTL Input High Voltage	V <sub>IH</sub>		2.0			V
LVTTTL Input Low Voltage	V <sub>IL</sub>				0.8	V
LVTTTL Input Current			-10		+10	μA
LVTTTL Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = +20μA	2.4			V
LVTTTL Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = -1mA			0.4	V

**Note 1:** At -40°C, DC characteristics are guaranteed by design and characterization.

**Note 2:** CML outputs open.

**Note 3:** Voltage applied to V<sub>CTRL</sub> pin is from +0.3V to +2.1V when input threshold is adjusted from +170mV to -170mV.

**Note 4:** R<sub>L</sub> = 50Ω to V<sub>CC</sub>.

## AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, T<sub>A</sub> = -40°C to +85°C. Typical values are at V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Input Data Rate			Table 2			
Differential Input Voltage (SDI±)	V <sub>ID</sub>	Threshold adjust disabled, Figure 1 (Note 6)	10		1600	mV <sub>P-P</sub>
Differential Input Voltage (SLBI±)		BER ≤ 10 <sup>-10</sup>	50		800	mV <sub>P-P</sub>
Jitter Transfer Bandwidth	J <sub>BW</sub>	OC-3		80	130	kHz
		OC-12		370	500	
		OC-48		1500	2000	
Jitter Peaking	J <sub>p</sub>	f ≤ J <sub>BW</sub>			0.1	dB
Sinusoidal Jitter Tolerance OC-48		f = 100kHz	3.1	8.0		UI <sub>P-P</sub>
		f = 1MHz	0.62	0.93		
		f = 10MHz	0.44	0.65		
Sinusoidal Jitter Tolerance OC-12		f = 25kHz	2.9	8.3		UI <sub>P-P</sub>
		f = 250kHz	0.59	1.03		
		f = 2.5MHz	0.42	0.63		
Sinusoidal Jitter Tolerance OC-3		f = 6.5kHz	2.9	7.8		UI <sub>P-P</sub>
		f = 65kHz	0.59	1.05		
		f = 650kHz	0.42	0.64		
Sinusoidal Jitter Tolerance with Threshold Adjust Enabled OC-48 (Note 7)		f = 100kHz		7.1		UI <sub>P-P</sub>
		f = 1MHz		0.82		
		f = 10MHz		0.54		
Jitter Generation	J <sub>GEN</sub>	(Note 8)		2.7	4.0	mUI <sub>RMS</sub>
Differential Input Return Loss (SDI±, SLBI±)	-20log  S <sub>11</sub>	100kHz to 2.5GHz		16		dB
		2.5GHz to 4.0GHz		15		

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## AC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $V_{CC} = +3.3V$  and  $T_A = +25^{\circ}C$ , unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CML OUTPUT SPECIFICATIONS (SDO<math>_{\pm}</math>, SCLKO<math>_{\pm}</math>)</b>						
Output Edge Speed	$t_r, t_f$	20% to 80%			110	ps
CML Output Differential Swing		$R_C = 100\Omega$ differential	600	800	1000	mV <sub>P-P</sub>
Clock-to-Q Delay	$t_{CLK-Q}$	(Note 9)	-50		+50	ps
<b>PLL ACQUISITION/LOCK SPECIFICATIONS</b>						
Tolerated Consecutive Identical Digits		$BER \leq 10^{-10}$		2000		bits
Acquisition Time		Figure 4 (Note 10)		5.5		ms
$\overline{LOL}$ Assert Time		Figure 4	2.3		100.0	$\mu s$
Low-Frequency Cutoff for DC-Offset Cancellation		$CAZ = 0.1\mu F$		4		kHz
<b>CLOCK HOLDOVER SPECIFICATIONS</b>						
Reference Clock Frequency			Table 3			
Maximum VCO Frequency Drift		(Note 11)			400	ppm

**Note 5:** AC characteristics are guaranteed by design and characterization.

**Note 6:** Jitter tolerance is guaranteed ( $BER \leq 10^{-10}$ ) within this input voltage range. Input threshold adjust is disabled with VCTRL connected to  $V_{CC}$ .

**Note 7:** Measured at OC-48 data rate using a 100mV<sub>P-P</sub> differential swing with a 20mVDC offset and an edge speed of 145ps (4th-order Bessel filter with  $f_{3dB} = 1.8GHz$ ).

**Note 8:** Measured with 10mV<sub>P-P</sub> differential input, 2<sup>23</sup> - 1 PRBS pattern at OC-48 with bandwidth from 12kHz to 20MHz.

**Note 9:** Relative to the falling edge of the SCLKO+ (Figure 3).

**Note 10:** Measured using a 0.82 $\mu F$  loop-filter capacitor initialized to +3.6V.

**Note 11:** Measured at OC-48 data rate under  $\overline{LOL}$  condition with the CDR clock output set by the external reference clock.

## Timing Diagrams

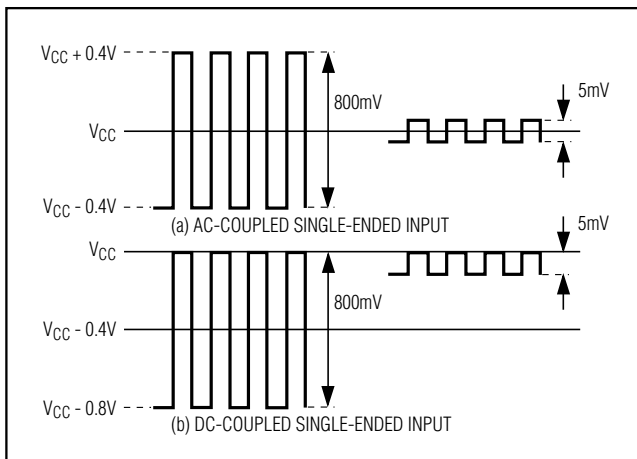


Figure 1. Definition of Input Voltage Swing

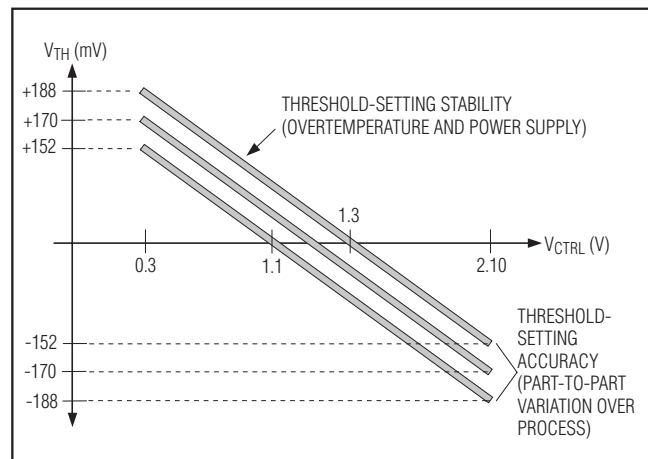


Figure 2. Relationship Between Control Voltage and Threshold Voltage

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## Timing Diagrams (continued)

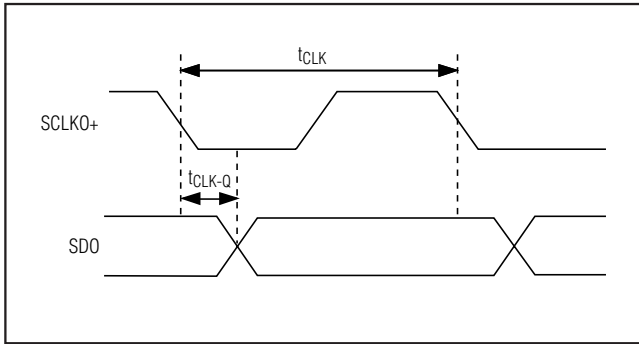


Figure 3. Definition of Clock-to-Q Delay

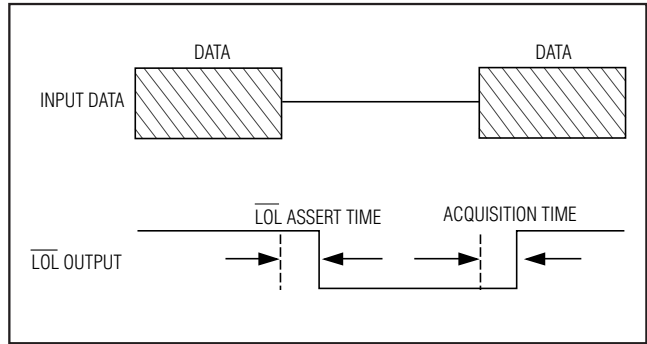
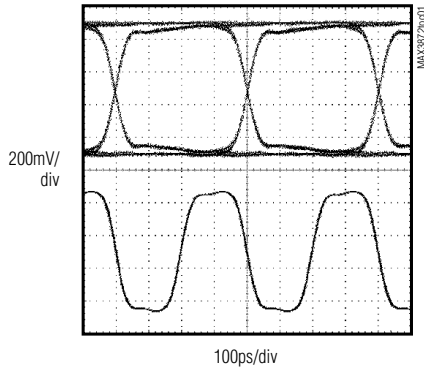


Figure 4.  $\overline{LOL}$  Assert Time and PLL Acquisition Time Measurement

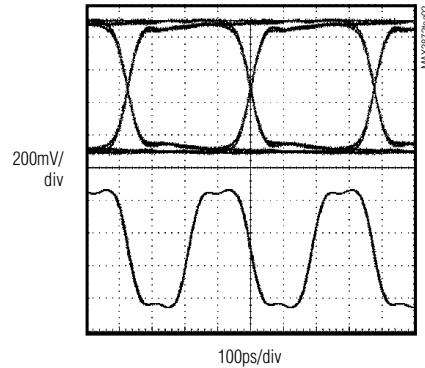
## Typical Operating Characteristics

( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

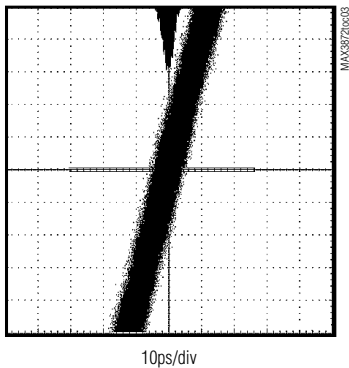
**RECOVERED CLOCK AND DATA  
(2.488Gbps, 2<sup>23</sup> - 1 PATTERN,  $V_{IN} = 10mV_{p-p}$ )**



**RECOVERED CLOCK AND DATA  
(2.67Gbps, 2<sup>23</sup> - 1 PATTERN,  $V_{IN} = 10mV_{p-p}$ )**

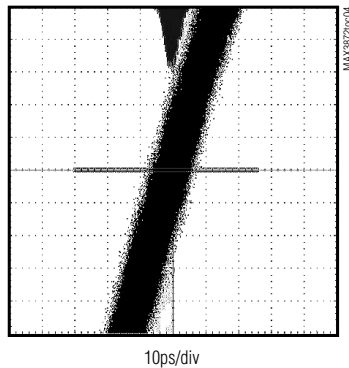


**RECOVERED CLOCK JITTER  
(2.488Gbps)**



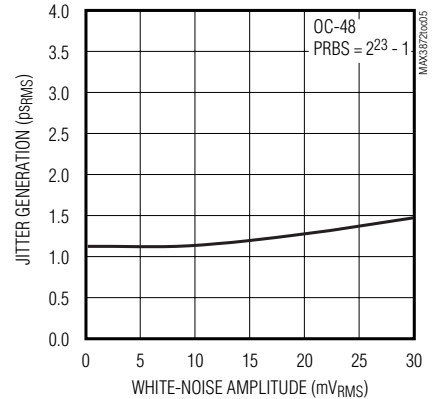
TOTAL WIDEBAND RMS JITTER = 1.60ps  
PEAK-TO-PEAK JITTER = 12.20ps

**RECOVERED CLOCK JITTER  
(622.08Mbps)**



TOTAL WIDEBAND RMS JITTER = 2.17ps  
PEAK-TO-PEAK JITTER = 15.80ps

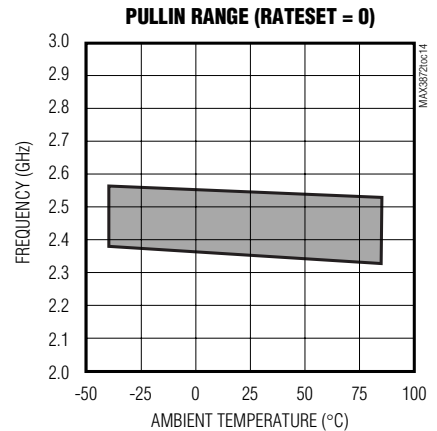
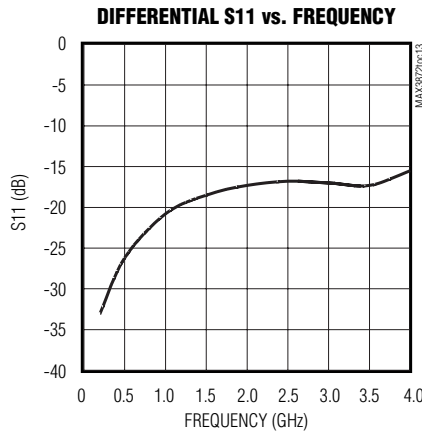
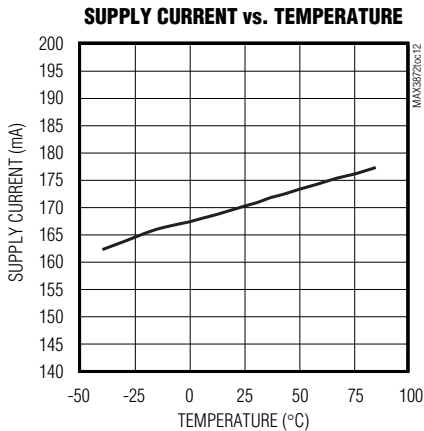
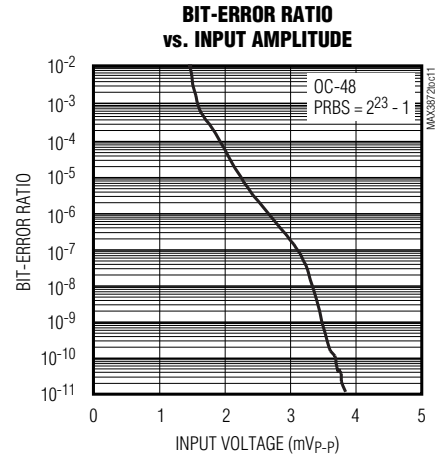
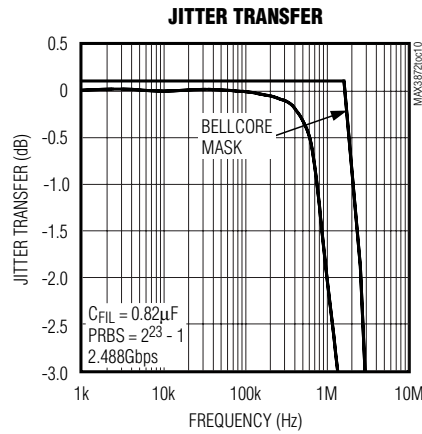
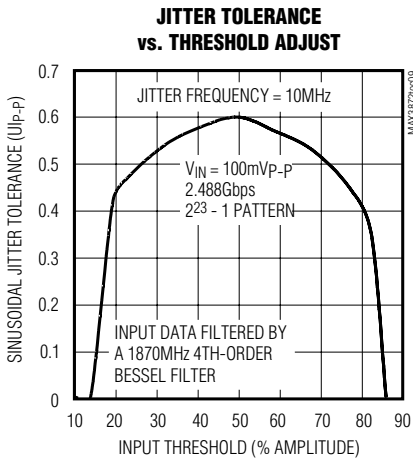
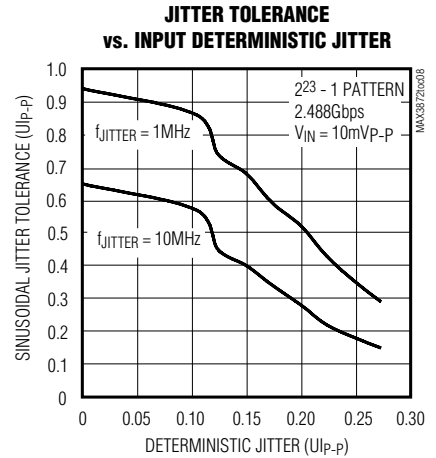
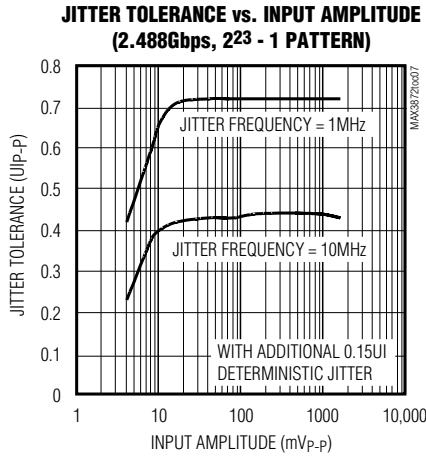
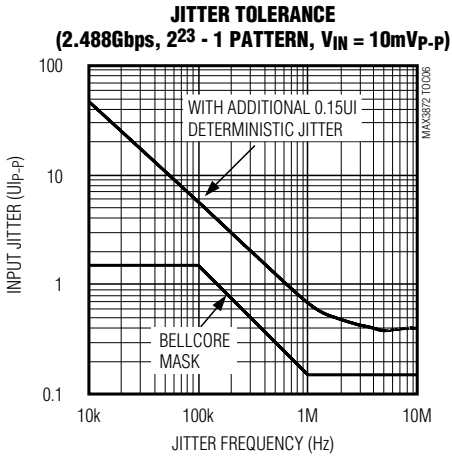
**JITTER GENERATION  
vs. POWER-SUPPLY WHITE NOISE**



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## Typical Operating Characteristics (continued)

(V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C, unless otherwise noted.)



# Multirate Clock and Data Recovery with Limiting Amplifier

## Pin Description

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PIN	NAME	FUNCTION
1, 4, 27	VCC	+3.3V Supply Voltage
2	SDI+	Positive Serial Data Input, CML
3	SDI-	Negative Serial Data Input, CML
5	SLBI+	Positive System Loopback Input or Reference Clock Input, CML
6	SLBI-	Negative System Loopback Input or Reference Clock Input, CML
7	SIS	Signal Selection Input, LVTTTL. Set low for normal operation, set high for system loopback.
8	$\overline{\text{LREF}}$	Lock to Reference Clock Input, LVTTTL. Set high for PLL lock to serial data, set low for PLL lock to reference clock.
9	$\overline{\text{LOL}}$	Loss-of-Lock Output, LVTTTL. Active low.
10, 11, 16, 25, 32	GND	Supply Ground
12	FIL	PLL Loop Filter Capacitor Input. Connect a 0.82 $\mu$ F capacitor between FIL and VCC_VCO.
13, 18	VCC_VCO	+3.3V Supply Voltage for the VCO
14	RS1	Multirate Select Input 1, LVTTTL (Table 2)
15	RS2	Multirate Select Input 2, LVTTTL (Table 2)
17	RATESET	VCO Frequency Select Input, LVTTTL (Table 2)
19	SCLKO-	Negative Serial Clock Output, CML
20	SCLKO+	Positive Serial Clock Output, CML
21, 24	VCC_OUT	+3.3V Supply Voltage for the CML Outputs
22	SDO-	Negative Serial Data Output, CML
23	SDO+	Positive Serial Data Output, CML
26	FREFSET	Reference Clock Frequency Select Input, LVTTTL (Tables 2 and 3)
28	CAZ+	Positive Capacitor Input for DC-Offset Cancellation Loop. Connect a 0.1 $\mu$ F capacitor between CAZ+ and CAZ-.
29	CAZ-	Negative Capacitor Input for DC-Offset Cancellation Loop. Connect a 0.1 $\mu$ F capacitor between CAZ+ and CAZ-.
30	VREF	+2.2V Bandgap Reference Voltage Output. Optionally used for threshold adjustment.
31	VCTRL	Analog Control Input for Threshold Adjustment. Connect to VCC to disable threshold adjust.
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical performance.





# Multirate Clock and Data Recovery with Limiting Amplifier

## Loop Filter

The phase detector and frequency detector outputs are summed into the loop filter. An external capacitor ( $C_{FIL}$ ) connected from  $FIL$  to  $VCC\_VCO$  is required to set the PLL damping ratio. Note that the PLL jitter bandwidth does not change as the external capacitor changes, but the jitter peaking, acquisition time, and loop stability are affected. See the *Design Procedure* section for guidelines on selecting this capacitor.

## VCOs with Programmable Dividers

The loop filter output controls the two on-chip VCOs. The VCOs provide low phase noise and are trimmed to the frequency of 2.488GHz and 2.667GHz. The  $RATESET$  pin is used to select the appropriate VCO. The VCO output is connected to programmable dividers controlled by inputs  $RS1$  and  $RS2$ . See Tables 2 and 3 for the proper settings.

## LOL Monitor

The  $\overline{LOL}$  output indicates a PLL lock failure, either because of excessive jitter present at the data input or because of loss of input data. The  $\overline{LOL}$  output is asserted low when the PLL loses lock.

## DC-Offset Cancellation Loop

A DC-offset cancellation loop is implemented to remove the DC offset of the limiting amplifier. To minimize the low-frequency pattern-dependent jitter associated with this DC-cancellation loop, the low-frequency cutoff is 10kHz (typ) with  $CAZ = 0.1\mu F$ , connected from  $CAZ+$  to  $CAZ-$ . The DC-offset cancellation loop operates only when threshold adjust is disabled.

## Design Procedure

### Decision Threshold Adjust

In applications in which the noise density is not balanced between logical zeros and ones (i.e., optical amplification using EDFA amplifiers), lower bit-error ratios (BERs) can be achieved by adjusting the input threshold. Varying the voltage at  $V_{CTRL}$  from +0.3V to +2.1V achieves a vertical decision threshold adjustment of +170mV to -170mV, respectively (Figure 2). Use the provided bandgap reference voltage output ( $V_{REF}$ ) with a voltage-divider circuit or the output of a DAC to set the voltage at  $V_{CTRL}$ .  $V_{REF}$  can be used to generate the voltage for  $V_{CTRL}$  (Figure 10). If threshold adjust is not required, disable it by connecting  $V_{CTRL}$  directly to  $VCC$  and leave  $V_{REF}$  floating.

## Modes of Operation

The MAX3872 has three operational modes controlled by the  $\overline{LREF}$  and  $SIS$  inputs. The three operational modes are normal, system loopback, and clock holdover. Normal operation mode requires a serial data stream at the  $SDI\pm$  input, system loopback mode requires a serial data stream at the  $SLBI\pm$  input, and clock holdover mode requires a reference clock signal at the  $SLBI\pm$  inputs. See Table 1 for the required  $\overline{LREF}$  and  $SIS$  settings. Once an operational mode is chosen, the remaining logic inputs ( $RATESET$ ,  $RS1$ ,  $RS2$ , and  $FREFSET$ ) program the input data rate or reference clock frequency.

### Normal and System Loopback Settings

Three pins ( $RS1$ ,  $RS2$ , and  $RATESET$ ) are available for setting the  $SDI\pm$  and  $SLBI\pm$  input to receive the appropriate data rate. The  $FREFSET$  pin can be set to a zero or 1 while in normal or system loopback mode (Table 2).

### Clock Frequencies in Holdover Mode

Set the incoming reference clock frequency and outgoing serial clock frequency by setting  $RS1$ ,  $RS2$ ,  $RATESET$ , and  $FREFSET$  appropriately (Table 3).

Table 1. Operational Modes

MODE	$\overline{LREF}$	SIS
Normal	1	0
System loopback	1	1
Clock holdover	0	1 or 0

Table 2. Data Rate Settings

INPUT DATA RATE (bps)	RS1	RS2	RATESET	FREFSET
2.667G	0	0	1	1 or 0
2.488G/2.5G	0	0	0	1 or 0
1.25G/1.244G	1	1	0	1 or 0
666.51M	0	1	1	1 or 0
622.08M	0	1	0	1 or 0
166.63M	1	0	1	1 or 0
155.52M	1	0	0	1 or 0

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Table 3. Holdover Frequency Settings

REFERENCE CLOCK FREQUENCY (MHz)	SCLKO FREQUENCY	RS1	RS2	RATESET	FREFSET
666.51	2.667GHz	0	0	1	0
666.51	666.51MHz	0	1	1	0
666.51	166.63MHz	1	0	1	0
622.08/625	1.244/1.25GHz	1	1	0	0
622.08/625	2.488GHz/2.5GHz	0	0	0	0
622.08	622.08MHz	0	1	0	0
622.08	155.52MHz	1	0	0	0
166.63	2.67GHz	0	0	1	1
166.63	666.51MHz	0	1	1	1
166.63	166.63MHz	1	0	1	1
155.52/156.25	1.244/1.25GHz	1	1	0	1
155.52/156.25	2.488GHz/2.5GHz	0	0	0	1
155.52	622.08MHz	0	1	0	1
155.52	155.52MHz	1	0	0	1

### Setting the Loop Filter

The MAX3872 is designed for regenerator and receiver applications. Its fully integrated PLL is a classic 2nd-order feedback system, with a jitter transfer bandwidth ( $J_{BW}$ ) below 2.0MHz. The external capacitor ( $C_{FIL}$ ) connected from FIL to VCC\_VCO sets the PLL loop damping. Note that the PLL jitter transfer bandwidth does not change as  $C_{FIL}$  changes, but the jitter peaking, acquisition time, and loop stability are affected. Figures 6 and 7 show the open-loop and closed-loop transfer functions.

The PLL zero frequency,  $f_z$ , is a function of external capacitor  $C_{FIL}$ , and can be approximated according to:

$$f_z = \frac{1}{2\pi(650\Omega)C_{FIL}}$$

For an overdamped system ( $f_z / J_{BW} < 0.25$ ), the jitter peaking ( $J_P$ ) of a 2nd-order system can be approximated by:

$$J_P = 20 \log \left( 1 + \frac{f_z}{J_{BW}} \right)$$

where  $J_{BW}$  is the jitter transfer bandwidth for a given data rate.

The recommended value of  $C_{FIL} = 0.82\mu\text{F}$  is to guarantee a maximum jitter peaking of less than 0.1dB for all data rates. Decreasing  $C_{FIL}$  from the recommended value decreases acquisition time, with the tradeoff of increased peaking. For data rates greater than OC-3,  $C_{FIL}$  can be less than  $0.82\mu\text{F}$  and still meet the jitter-peaking specification.

Excessive reduction of  $C_{FIL}$  might cause PLL instability.  $C_{FIL}$  must be a low-TC, high-quality capacitor of type X7R or better.

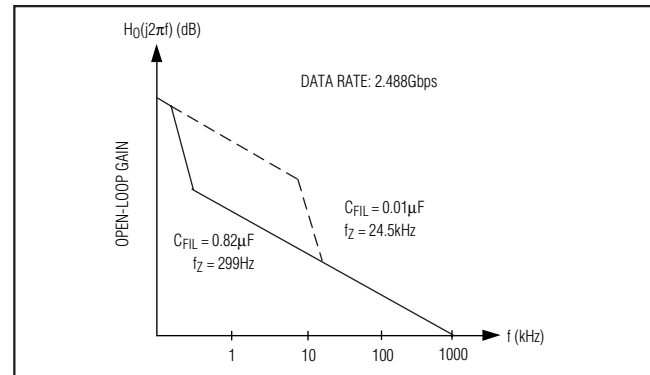


Figure 6. Open-Loop Transfer Function

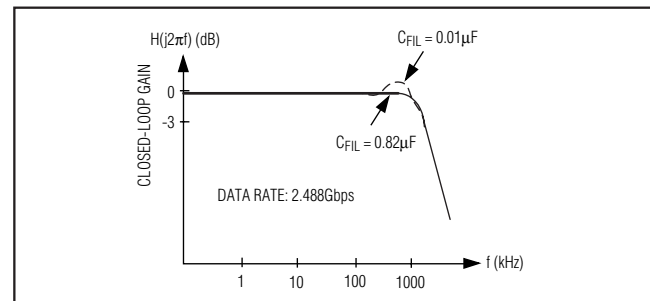


Figure 7. Closed-Loop Transfer Function

# Multirate Clock and Data Recovery with Limiting Amplifier

## Input Terminations

The SDI± and SLBI± inputs of the MAX3872 are current-mode logic (CML) compatible. The inputs all provide internal 50Ω termination to reduce the required number of external components. AC-coupling is recommended. See Figure 8 for the input structure. For additional information on logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML*.

## Output Terminations

The MAX3872 uses CML for its high-speed digital outputs (SDO± and SCLKO±). The configuration of the output circuit includes internal 50Ω back terminations to VCC. See Figure 9 for the output structure. CML outputs can be terminated by 50Ω to VCC, or by 100Ω differential impedance. For additional information on logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML*.

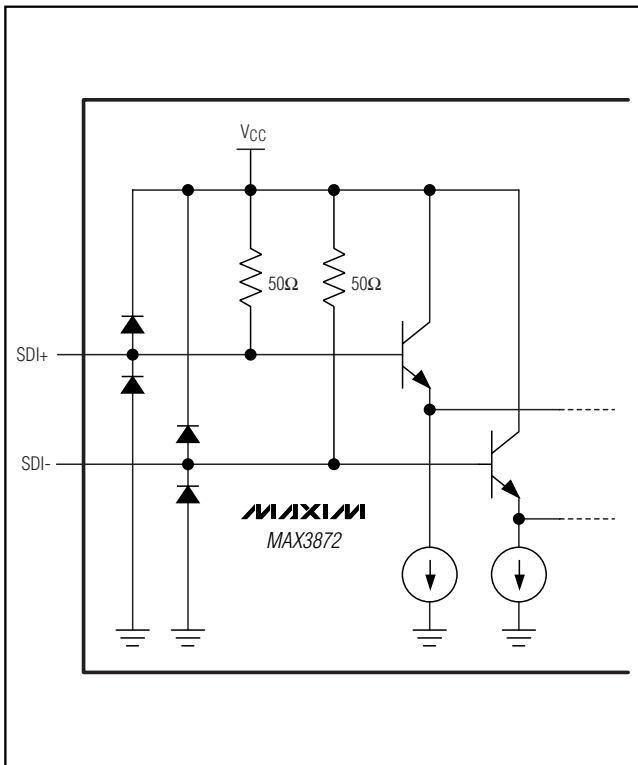


Figure 8. CML Input Model

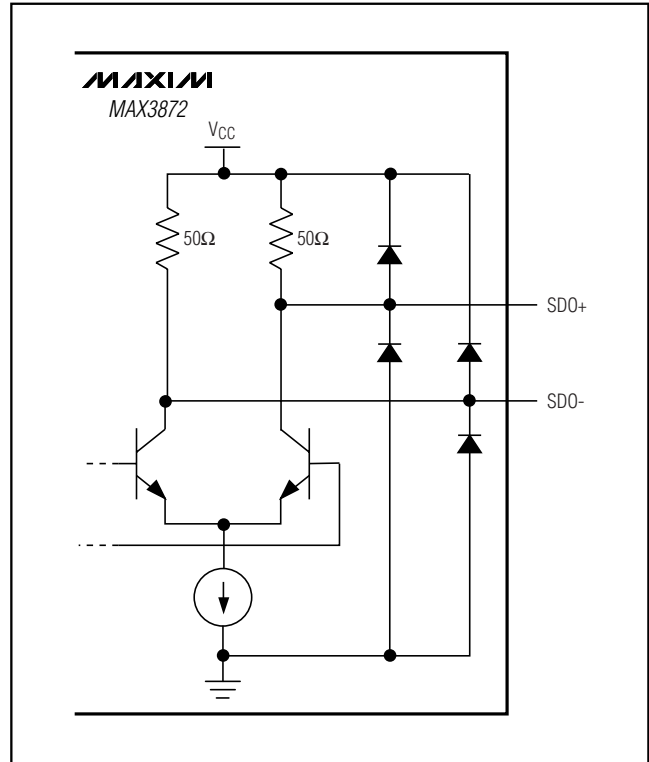


Figure 9. CML Output Model

## Applications Information

### Clock Holdover Capability

Clock holdover is required in some applications in which a valid clock must be provided to the upstream device in the absence of data transitions. To provide this function, an external reference clock signal must be applied to the SLBI± inputs and the proper control signals set (see the *Modes of Operation* section). To enter holdover mode automatically when there are no transitions applied to the SDI± inputs,  $\overline{\text{LOL}}$  or the system  $\overline{\text{LOS}}$  can be directly connected to LREF.

### System Loopback

The MAX3872 is designed to allow system loopback testing. When the device is set for system loopback mode, the serial output data of a transmitter may be directly connected to the SLBI inputs to run system diagnostics. See Table 1 for selecting system loopback operation mode. While in system loopback mode, LREF should not be connected to  $\overline{\text{LOL}}$ .

# Multirate Clock and Data Recovery with Limiting Amplifier

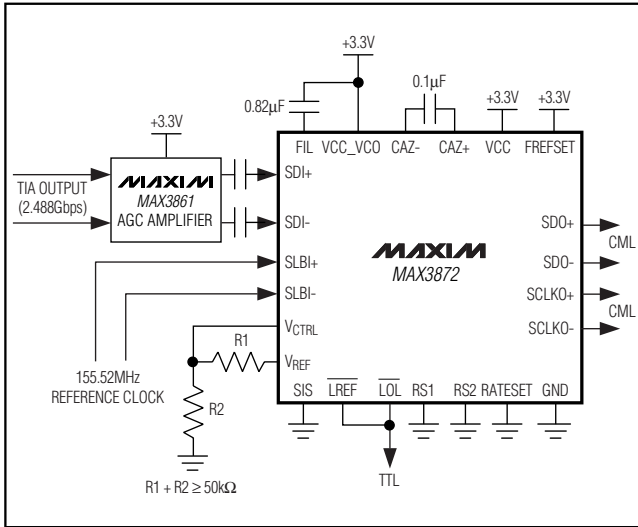


Figure 10. Interfacing with the MAX3861 AGC Using Threshold Adjust

### Consecutive Identical Digits (CIDs)

The MAX3872 has a low phase and frequency drift in the absence of data transitions. As a result, long runs of consecutive zeros and ones can be tolerated while maintaining a BER better than  $10^{-10}$ . The CID tolerance is tested using a  $2^{13} - 1$  PRBS with long runs of ones and zeros inserted in the pattern. A CID tolerance of 2000 bits is typical.

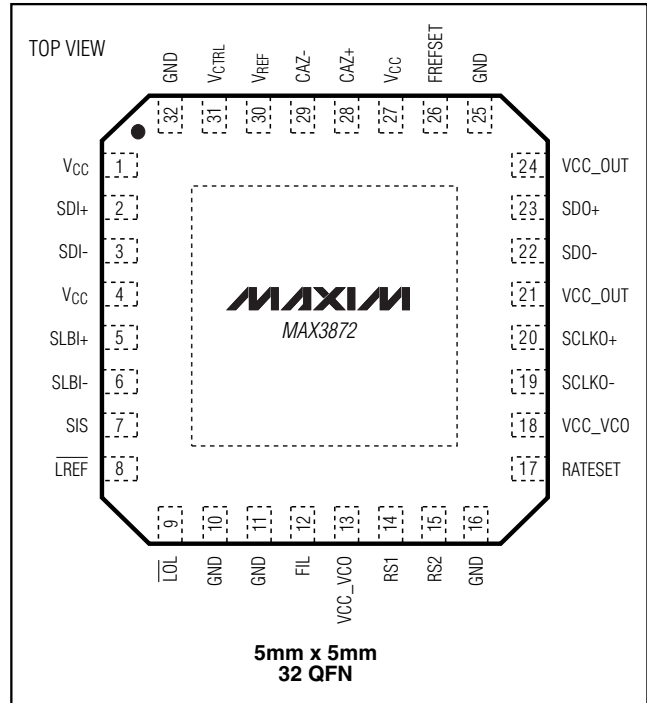
### Exposed Pad (EP) Package

The EP 32-pin QFN incorporates features that provide a very-low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3872 and should be soldered to the circuit board for proper thermal and electrical performance.

### Layout Considerations

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3872 high-speed inputs and outputs. Power-supply decoupling should be placed as close to VCC as possible. To reduce feedthrough, isolate the input signals from the output signals. If a bare die is used, mount the back of die to ground (GND) potential.

## Pin Configuration



## Chip Information

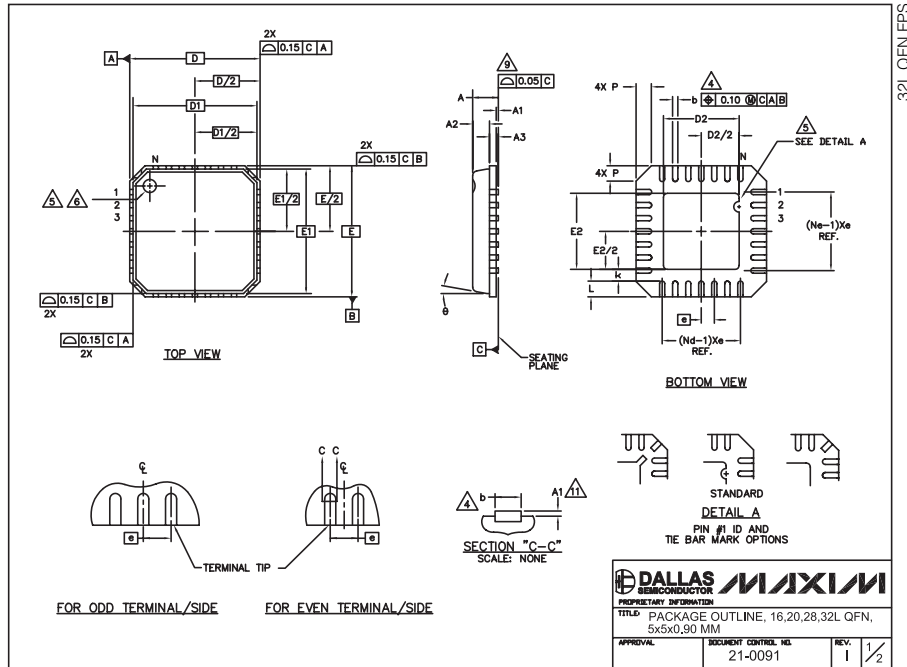
TRANSISTOR COUNT: 5142  
 PROCESS: SiGe BiPOLAR  
 SUBSTRATE: SOI

# Multirate Clock and Data Recovery with Limiting Amplifier

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX3872



COMMON DIMENSIONS												
PKG SYMBOL	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
*	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
g	0"			0"			12"			0"		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

**NOTES:**

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -- 1994.
3. N IS THE NUMBER OF TERMINALS.  
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

**DALLAS SEMICONDUCTOR** **MAXIM**

PROPRIETARY INFORMATION  
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0,90 MM  
APPROVAL: \_\_\_\_\_ DOCUMENT CONTROL NO: 21-0091 REV: 1 2/2

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