

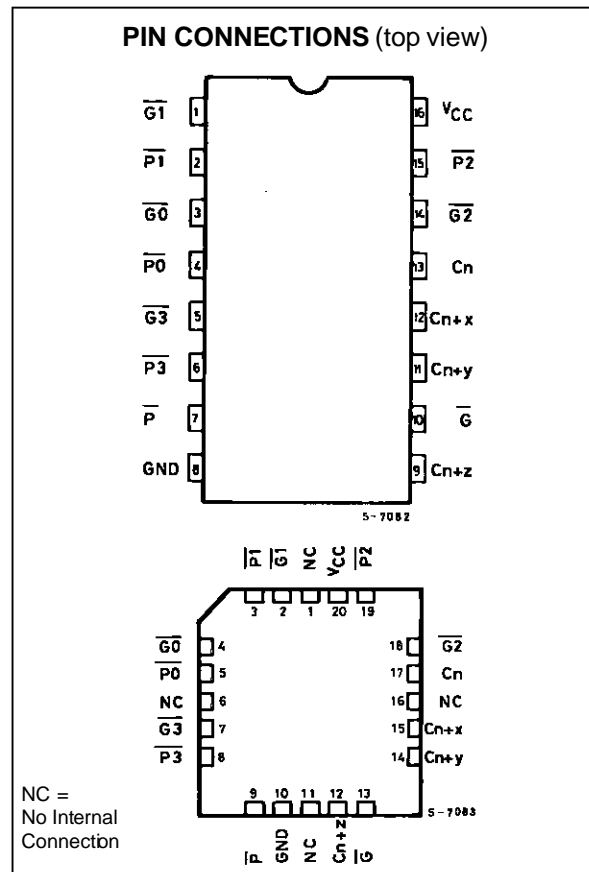
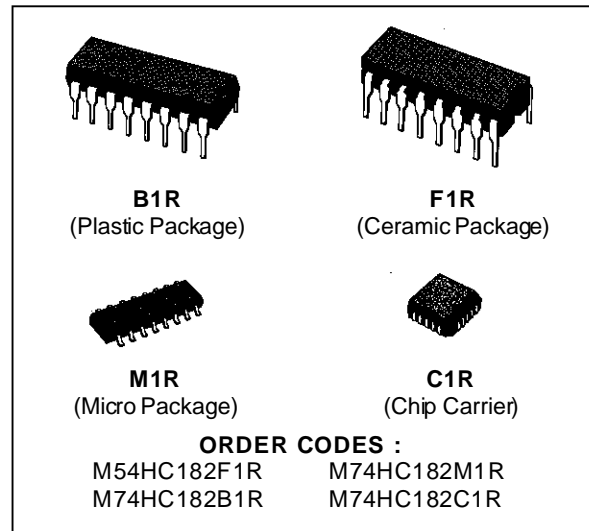
FUNCTION LOOK AHEAD CARRY GENERATOR

- HIGH SPEED
 $t_{PD} = 14 \text{ ns (TYP.) at } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V to } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS182

DESCRIPTION

The M54/74HC182 is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated in silicon gate CMOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuit are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin connection table. When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALUs are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator. All inputs are equipped with protection circuits against static discharge and transient excess voltage.



FUNCTION TABLES

FOR \overline{G} OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	\overline{G}
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
ALL OTHER COMBINATIONS							H

FOR \overline{P} OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	\overline{P}
L	L	L	L	L
ALL OTHER COMBINATIONS				H

FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
ALL OTHER COMBINATIONS			L

FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
ALL OTHER COMBINATIONS					L

FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
ALL OTHER COMBINATIONS							L

$$C_{n+x} = G0 + P0C_n$$

$$C_{n+y} = G1 + P1G0 + P1P0C_n$$

$$C_{n+z} = G2 + P2G1 + P2P1G0 + P2P1P0C_n$$

$$G = \overline{G3} + G3 + P3G2 + P3P2G1 + P3P2P1G0$$

$$P = P3P2P1P0$$

or

$$C_{n+x} = \overline{Y0} + (X0 + C_n)$$

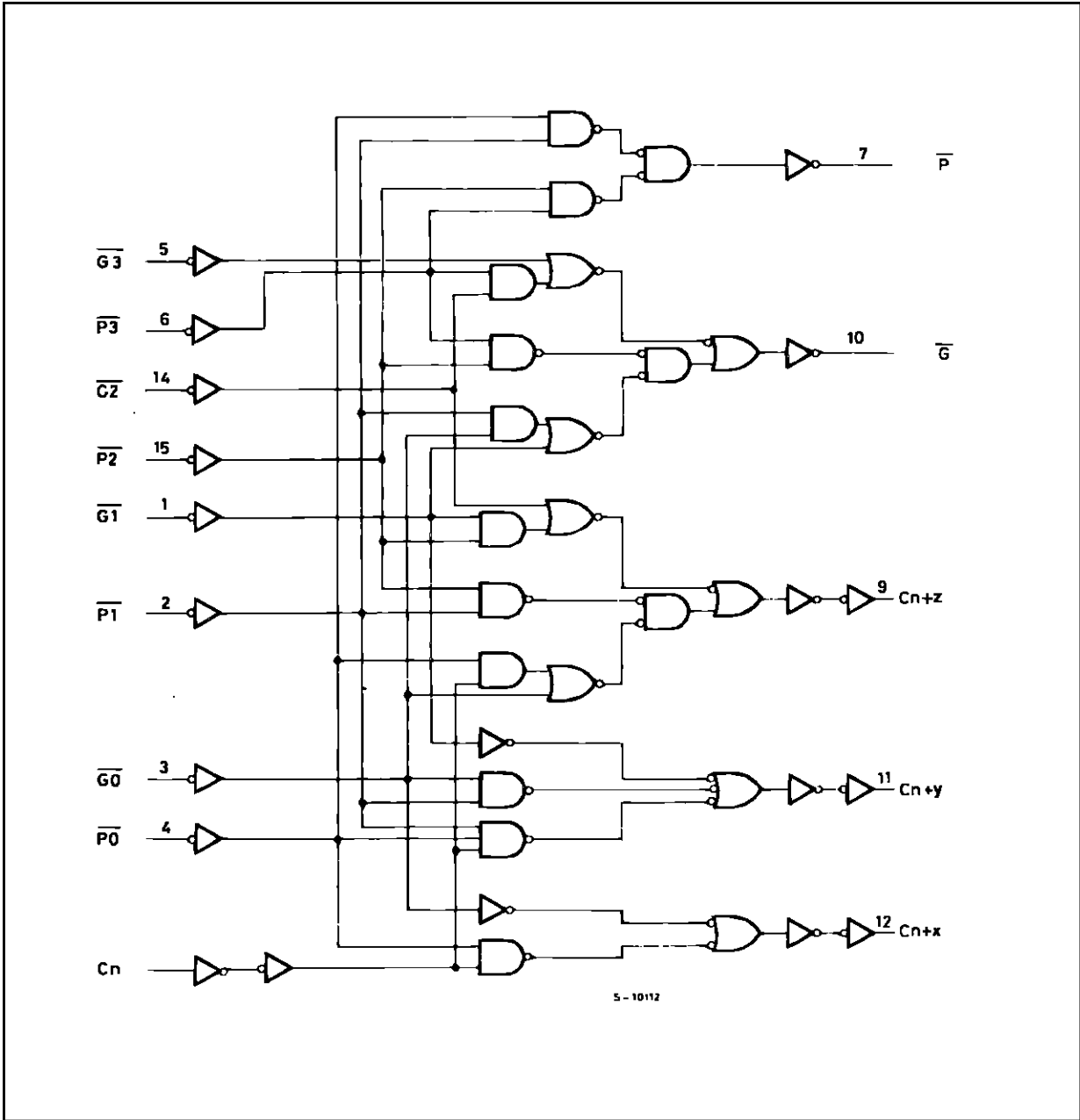
$$C_{n+y} = \overline{Y1} + [X1 + Y0(X0 + C_n)]$$

$$C_{n+z} = \overline{Y2} + \{X2 + Y1[X1 + Y0(X0 + C_n)]\}$$

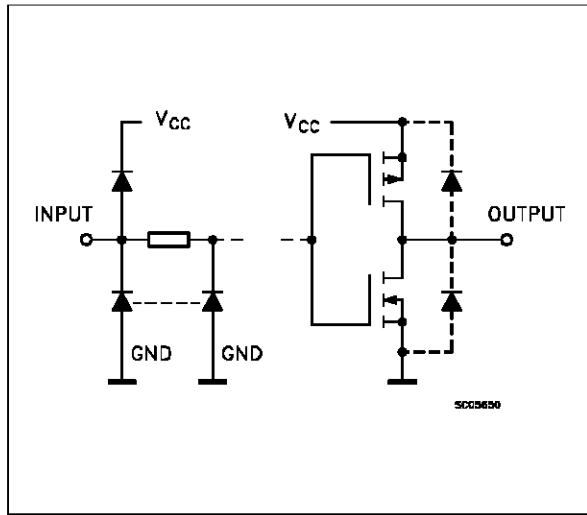
$$G = Y3 + (X3 + Y2)(X3 + X2 + Y1)(X3 + X2 + X1 + Y0)$$

$$P = X3 + X2 + X1 + X0$$

LOGIC DIAGRAM



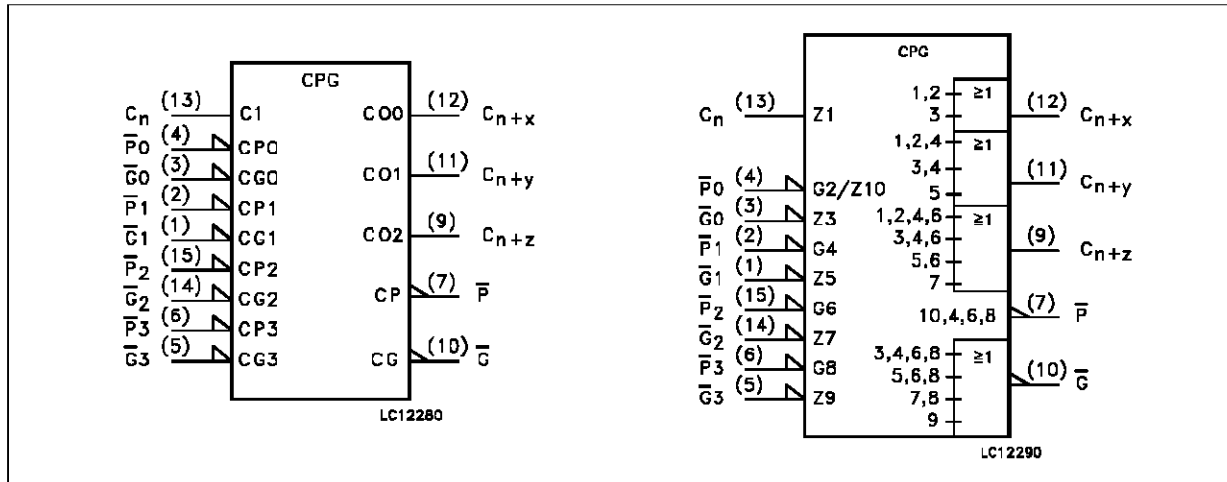
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	G0 to G3	Carry Generate Inputs (Active LOW)
4, 2, 15, 6	P0 to P3	Carry Propagate Inputs (Active LOW)
7	P	Carry Propagate Output (Active LOW)
9	Cn+z	Function Output
10	G	Carry Generate Output (Active LOW)
11	Cn+y	Function Output
12	Cn+x	Function Output
13	Cn	
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
 (*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V	0 to 1000	ns
		V _{CC} = 4.5 V	0 to 500	
		V _{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value						Unit				
				T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC					
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.			
V _{IH}	High Level Input Voltage	2.0					1.5			1.5		V		
		4.5					3.15			3.15				
		6.0					4.2			4.2				
V _{IL}	Low Level Input Voltage	2.0							0.5		0.5	V		
		4.5							1.35		1.35			
		6.0							1.8		1.8			
V _{OH}	High Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA			1.9	2.0		1.9		V		
		4.5					4.4	4.5		4.4	4.4			
		6.0					5.9	6.0		5.9	5.9			
		4.5					4.18	4.31		4.13	4.10			
		6.0					5.68	5.8		5.63	5.60			
V _{OL}	Low Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA				0.0	0.1		0.1	V		
		4.5						0.0	0.1		0.1			
		6.0						0.0	0.1		0.1			
		4.5						0.17	0.26		0.37		0.40	
		6.0						0.18	0.26		0.37		0.40	
I _I	Input Leakage Current	6.0							±0.1		±1		±1	μA
I _{OZ}	3 State Output Off State Current	6.0							±0.5		±5.0		±10	μA
I _{CC}	Quiescent Supply Current	6.0							4		40		80	μA

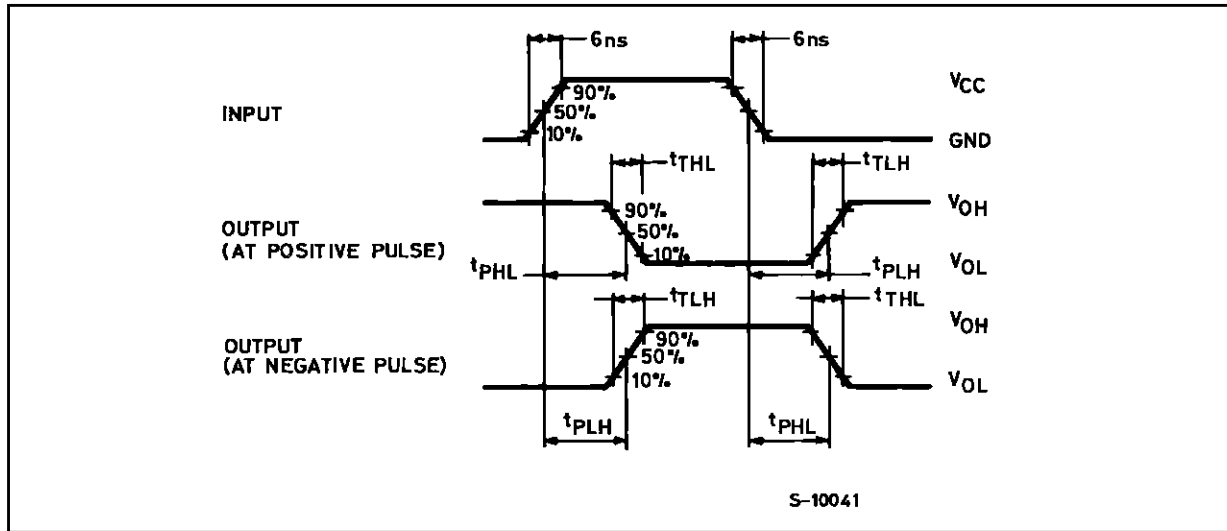
M54/M74HC182

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

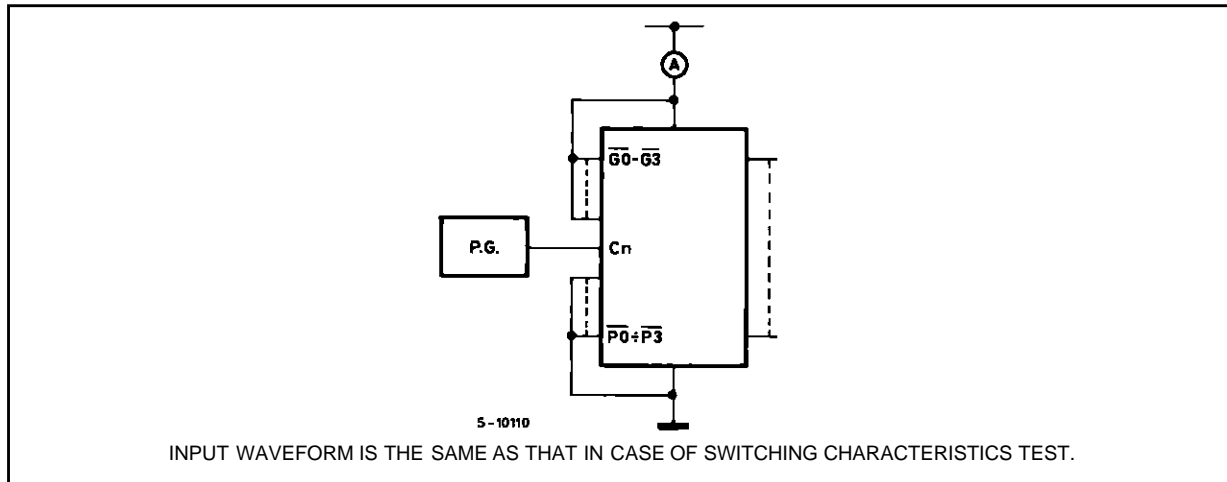
Symbol	Parameter	Test Conditions		Value						Unit	
		V_{CC} (V)		$T_A = 25 \text{ }^\circ\text{C}$ 54HC and 74HC			$-40 \text{ to } 85 \text{ }^\circ\text{C}$ 74HC		$-55 \text{ to } 125 \text{ }^\circ\text{C}$ 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($G_n, P_n - C_n + xyz$)	2.0			62	135		170		205	ns
		4.5			17	27		34		41	
		6.0			13	23		29		35	
t_{PLH} t_{PHL}	Propagation Delay Time ($G_n, P_n - G$)	2.0			72	150		190		225	ns
		4.5			19	30		38		45	
		6.0			14	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($P_n - P$)	2.0			62	135		170		205	ns
		4.5			17	27		34		41	
		6.0			13	23		29		35	
t_{PLH} t_{PHL}	Propagation Delay Time ($C_n - C_n + xyz$)	2.0			62	135		170		205	ns
		4.5			17	27		34		41	
		6.0			13	23		29		35	
C_{IN}	Input Capacitance				5	10		10		10	pF
$C_{PD} (*)$	Power Dissipation Capacitance				61						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

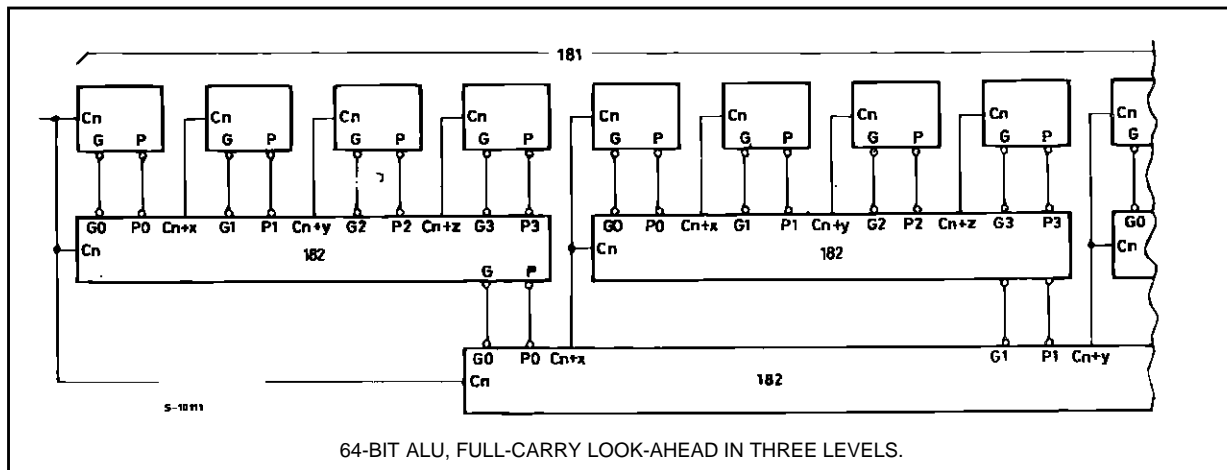
SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{cc} (Opr.)

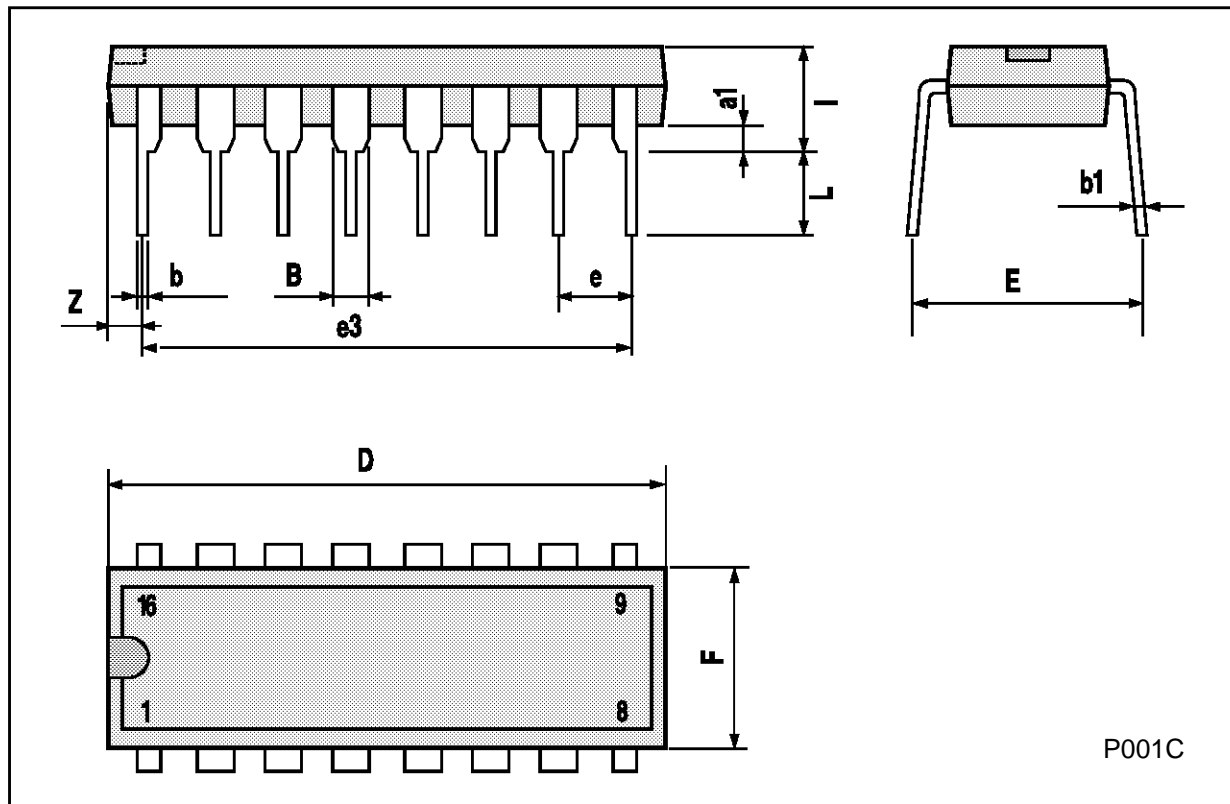


TYPICAL APPLICATION



Plastic DIP16 (0.25) MECHANICAL DATA

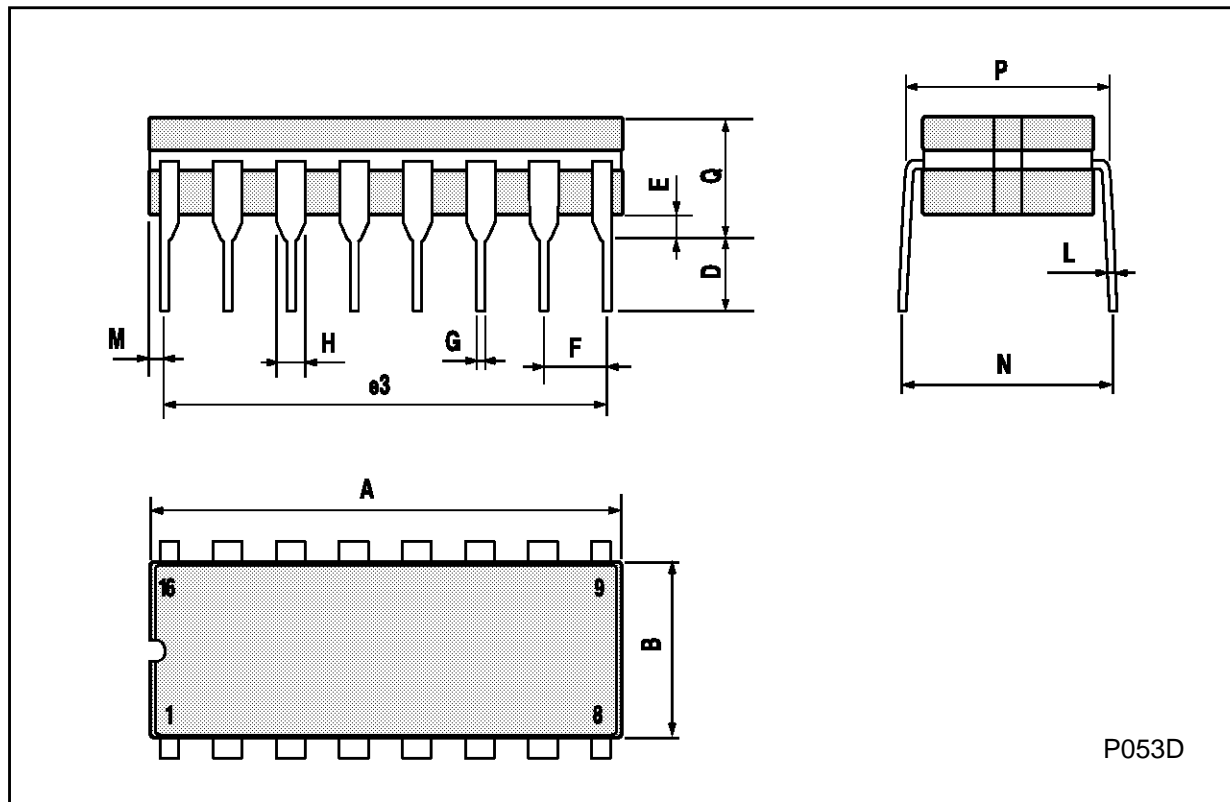
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

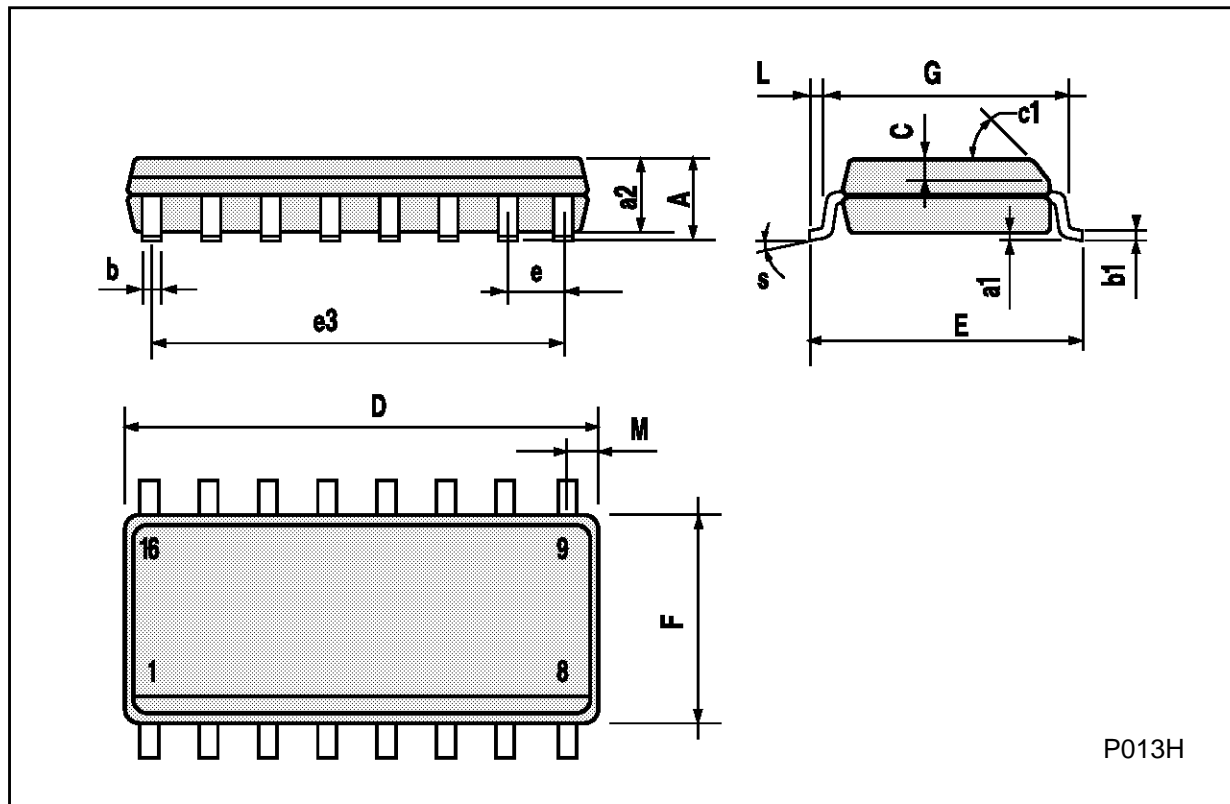
Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1994 SGS-THOMSON Microelectronics - All Rights Reserved

SGS-THOMSON Microelectronics GROUP OF COMPANIES
Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands -
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A