

24-Bit No Latency $\Delta\Sigma$ ™ ADC with Differential Input and Reference in MSOP

FEATURES

- 24-Bit ADC in an MS10 Package
- Low Supply Current (4 μ A in Autosleep Mode and 200 μ A in Conversion Mode)
- Differential Input and Differential Reference with GND to V_{CC} Common Mode Range
- 4ppm INL, No Missing Codes
- 4ppm Full-Scale Error and 1ppm Offset
- 0.29ppm Noise
- No Latency: Digital Filter Settles in a Single Cycle. Each Conversion Is Accurate, Even After an Input Step
- Single Supply 2.7V to 5.5V Operation
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter

APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain Gauge Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

DESCRIPTION

June 2000

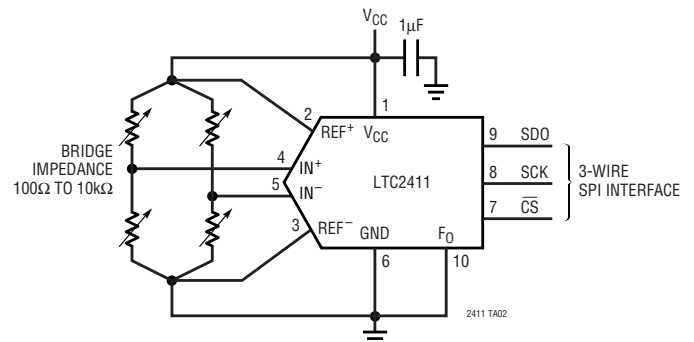
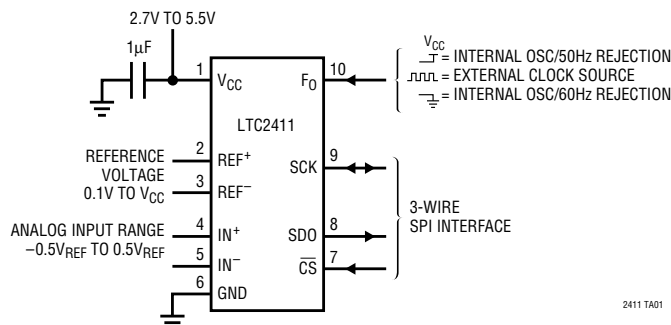
The LTC[®]2411 is a 2.7V to 5.5V micropower 24-bit differential $\Delta\Sigma$ analog to digital converter with an integrated oscillator, 4ppm INL and 0.29ppm RMS noise. It uses delta-sigma technology and provides single cycle settling time for multiplexed applications. Through a single pin, the LTC2411 can be configured for better than 110dB differential mode rejection at 50Hz or 60Hz \pm 2%, or it can be driven by an external oscillator for a user defined rejection frequency. The internal oscillator requires no external frequency setting components.

The converter accepts any external differential reference voltage from 0.1V to V_{CC} for flexible ratiometric and remote sensing measurement configurations. The full-scale differential input range is from $-0.5V_{REF}$ to $0.5V_{REF}$. The reference common mode voltage, V_{REFCM} , and the input common mode voltage, V_{INCM} , may be independently set anywhere within the GND to V_{CC} range of the LTC2411. The DC common mode input rejection is better than 140dB.

The LTC2411 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.

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TYPICAL APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND	-0.3V to 7V
Analog Input Pins Voltage to GND	-0.3V to ($V_{CC} + 0.3V$)
Reference Input Pins Voltage to GND	-0.3V to ($V_{CC} + 0.3V$)
Digital Input Voltage to GND	-0.3V to ($V_{CC} + 0.3V$)
Digital Output Voltage to GND	-0.3V to ($V_{CC} + 0.3V$)
Operating Temperature Range	
LTC2411C	0°C to 70°C
LTC2411I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>V_{CC} 1 □ □ 10 F_O REF^+ 2 □ □ 9 SCK REF^- 3 □ □ 8 SDO IN^+ 4 □ □ 7 CS IN^- 5 □ □ 6 GND</p> <p>MS10 PACKAGE 10-LEAD PLASTIC MSOP</p> <p>$T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 120^{\circ}C/W$</p>	ORDER PART NUMBER
	LTC2411CMS LTC2411IMS
	MS10 PART MARKING
	LTNS LTNT

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	$0.1V \leq V_{REF} \leq V_{CC}$, $-0.5 \cdot V_{REF} \leq V_{IN} \leq 0.5 \cdot V_{REF}$, (Note 5)	●	24		Bits
Integral Nonlinearity	$REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$, (Note 6) $5V \leq V_{CC} \leq 5.5V$, $REF^+ = 5V$, $REF^- = GND$, $V_{INCM} = 2.5V$, (Note 6)	●	3 4	14	ppm of V_{REF} ppm of V_{REF}
Offset Error	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^+ = IN^- \leq V_{CC}$, (Note 14)	●	5	20	μV
Offset Error Drift	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^+ = IN^- \leq V_{CC}$		50		nV/ $^{\circ}C$
Positive Full-Scale Error	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.75REF^+$, $IN^- = 0.25 \cdot REF^+$	●	4	12	ppm of V_{REF}
Positive Full-Scale Error Drift	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.75REF^+$, $IN^- = 0.25 \cdot REF^+$		0.04		ppm of $V_{REF}/^{\circ}C$
Negative Full-Scale Error	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.25 \cdot REF^+$, $IN^- = 0.75 \cdot REF^+$	●	4	12	ppm of V_{REF}
Negative Full-Scale Error Drift	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.25 \cdot REF^+$, $IN^- = 0.75 \cdot REF^+$		0.04		ppm of $V_{REF}/^{\circ}C$
Total Unadjusted Error	$REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$ $5V \leq V_{CC} \leq 5.5V$, $REF^+ = 5V$, $REF^- = GND$, $V_{INCM} = 2.5V$		5 10		ppm of V_{REF} ppm of V_{REF}
Output Noise	$5V \leq V_{CC} \leq 5.5V$, $REF^+ = 5V$, $V_{REF^-} = GND$, $GND \leq IN^+ = IN^- \leq 5V$, (Note 13)		1.45		μV_{RMS}

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common Mode Rejection DC	$2.5\text{V} \leq \text{REF}^+ \leq V_{\text{CC}}$, $\text{REF}^- = \text{GND}$, $\text{GND} \leq \text{IN}^- = \text{IN}^+ \leq 5\text{V}$	●	130	140		dB
Input Common Mode Rejection 60Hz $\pm 2\%$	$2.5\text{V} \leq \text{REF}^+ \leq V_{\text{CC}}$, $\text{REF}^- = \text{GND}$, $\text{GND} \leq \text{IN}^- = \text{IN}^+ \leq 5\text{V}$, (Note 7)	●	140			dB
Input Common Mode Rejection 50Hz $\pm 2\%$	$2.5\text{V} \leq \text{REF}^+ \leq V_{\text{CC}}$, $\text{REF}^- = \text{GND}$, $\text{GND} \leq \text{IN}^- = \text{IN}^+ \leq 5\text{V}$, (Note 8)	●	140			dB
Input Normal Mode Rejection 60Hz $\pm 2\%$	(Note 7)	●	110	140		dB
Input Normal Mode Rejection 50Hz $\pm 2\%$	(Note 8)	●	110	140		dB
Reference Common Mode Rejection DC	$2.5\text{V} \leq \text{REF}^+ \leq V_{\text{CC}}$, $\text{GND} \leq \text{REF}^- \leq 2.5\text{V}$, $V_{\text{REF}} = 2.5\text{V}$, $\text{IN}^- = \text{IN}^+ = \text{GND}$	●	130	140		dB
Power Supply Rejection, DC	$\text{REF}^+ = 2.5\text{V}$, $\text{REF}^- = \text{GND}$, $\text{IN}^- = \text{IN}^+ = \text{GND}$			110		dB
Power Supply Rejection, 60Hz $\pm 2\%$	$\text{REF}^+ = 2.5\text{V}$, $\text{REF}^- = \text{GND}$, $\text{IN}^- = \text{IN}^+ = \text{GND}$, (Note 7)			120		dB
Power Supply Rejection, 50Hz $\pm 2\%$	$\text{REF}^+ = 2.5\text{V}$, $\text{REF}^- = \text{GND}$, $\text{IN}^- = \text{IN}^+ = \text{GND}$, (Note 8)			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage		●	$\text{GND} - 0.3\text{V}$		$V_{\text{CC}} + 0.3\text{V}$	V
IN^-	Absolute/Common Mode IN^- Voltage		●	$\text{GND} - 0.3\text{V}$		$V_{\text{CC}} + 0.3\text{V}$	V
V_{IN}	Input Differential Voltage Range ($\text{IN}^+ - \text{IN}^-$)		●	$-V_{\text{REF}}/2$		$V_{\text{REF}}/2$	V
REF^+	Absolute/Common Mode REF^+ Voltage		●	0.1		V_{CC}	V
REF^-	Absolute/Common Mode REF^- Voltage		●	GND		$V_{\text{CC}} - 0.1\text{V}$	V
V_{REF}	Reference Differential Voltage Range ($\text{REF}^+ - \text{REF}^-$)		●	0.1		V_{CC}	V
$C_S (\text{IN}^+)$	IN^+ Sampling Capacitance				6		pF
$C_S (\text{IN}^-)$	IN^- Sampling Capacitance				6		pF
$C_S (\text{REF}^+)$	REF^+ Sampling Capacitance				6		pF
$C_S (\text{REF}^-)$	REF^- Sampling Capacitance				6		pF
$I_{\text{DC_LEAK}} (\text{IN}^+)$	IN^+ DC Leakage Current	$\overline{C_S} = V_{\text{CC}}$, $\text{IN}^+ = \text{GND}$	●	-10	1	10	nA
$I_{\text{DC_LEAK}} (\text{IN}^-)$	IN^- DC Leakage Current	$\overline{C_S} = V_{\text{CC}}$, $\text{IN}^- = \text{GND}$	●	-10	1	10	nA
$I_{\text{DC_LEAK}} (\text{REF}^+)$	REF^+ DC Leakage Current	$\overline{C_S} = V_{\text{CC}}$, $\text{REF}^+ = 5\text{V}$	●	-10	1	10	nA
$I_{\text{DC_LEAK}} (\text{REF}^-)$	REF^- DC Leakage Current	$\overline{C_S} = V_{\text{CC}}$, $\text{REF}^- = \text{GND}$	●	-10	1	10	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage CS, F ₀	$2.7V \leq V_{CC} \leq 5.5V$	●	2.5		V
		$2.7V \leq V_{CC} \leq 3.3V$		2.0		V
V_{IL}	Low Level Input Voltage CS, F ₀	$4.5V \leq V_{CC} \leq 5.5V$	●		0.8	V
		$2.7V \leq V_{CC} \leq 5.5V$			0.6	V
V_{IH}	High Level Input Voltage SCK	$2.7V \leq V_{CC} \leq 5.5V$ (Note 9)	●	2.5		V
		$2.7V \leq V_{CC} \leq 3.3V$ (Note 9)		2.0		V
V_{IL}	Low Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 9)	●		0.8	V
		$2.7V \leq V_{CC} \leq 5.5V$ (Note 9)			0.6	V
I_{IN}	Digital Input Current CS, F ₀	$0V \leq V_{IN} \leq V_{CC}$	●	-10	10	μA
I_{IN}	Digital Input Current SCK	$0V \leq V_{IN} \leq V_{CC}$ (Note 9)	●	-10	10	μA
C_{IN}	Digital Input Capacitance CS, F ₀			10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)		10		pF
V_{OH}	High Level Output Voltage SDO	$I_O = -800\mu\text{A}$	●	$V_{CC} - 0.5V$		V
V_{OL}	Low Level Output Voltage SDO	$I_O = 1.6\text{mA}$	●		0.4V	V
V_{OH}	High Level Output Voltage SCK	$I_O = -800\mu\text{A}$ (Note 10)	●	$V_{CC} - 0.5V$		V
V_{OL}	Low Level Output Voltage SCK	$I_O = 1.6\text{mA}$ (Note 10)	●		0.4V	V
I_{OZ}	Hi-Z Output Leakage SDO		●	-10	10	μA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{CC}	Supply Voltage		●	2.7	5.5	V	
I_{CC}	Supply Current		●				
		Conversion Mode	●		200	300	μA
		Sleep Mode	●		4	10	μA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
f_{EOSC}	External Oscillator Frequency Range	●	2.56		2000	kHz	
t_{HEO}	External Oscillator High Period	●	0.25		390	μs	
t_{LEO}	External Oscillator Low Period	●	0.25		390	μs	
t_{CONV}	Conversion Time	$F_0 = 0\text{V}$	●	130.86	133.53	136.20	ms
		$F_0 = V_{\text{CC}}$	●	157.03	160.23	163.44	ms
		External Oscillator (Note 11)	●	20510/ f_{EOSC} (in kHz)			ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10)		19.2		kHz	
		External Oscillator (Notes 10, 11)		$f_{\text{EOSC}}/8$		kHz	
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45	55	%	
f_{ESCK}	External SCK Frequency Range	(Note 9)	●		2000	kHz	
t_{LESCK}	External SCK Low Period	(Note 9)	●	250		ns	
t_{HESCK}	External SCK High Period	(Note 9)	●	250		ns	
$t_{\text{DOUT_ISCK}}$	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12)	●	1.64	1.67	1.70	ms
		External Oscillator (Notes 10, 11)	●	256/ f_{EOSC} (in kHz)			ms
$t_{\text{DOUT_ESCK}}$	External SCK 32-Bit Data Output Time	(Note 9)	●	32/ f_{ESCK} (in kHz)			ms
t_1	$\overline{\text{CS}} \downarrow$ to SDO Low Z		●	0	200	ns	
t_2	$\overline{\text{CS}} \uparrow$ to SDO High Z		●	0	200	ns	
t_3	$\overline{\text{CS}} \downarrow$ to SCK \downarrow	(Note 10)	●	0	200	ns	
t_4	$\overline{\text{CS}} \downarrow$ to SCK \uparrow	(Note 9)	●	50		ns	
t_{KQMAX}	SCK \downarrow to SDO Valid		●		220	ns	
t_{KQMIN}	SDO Hold After SCK \downarrow	(Note 5)	●	15		ns	
t_5	SCK Set-Up Before $\overline{\text{CS}} \downarrow$		●	50		ns	
t_6	SCK Hold After $\overline{\text{CS}} \downarrow$		●		50	ns	

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: $V_{\text{CC}} = 2.7$ to 5.5V unless otherwise specified.

$V_{\text{REF}} = \text{REF}^+ - \text{REF}^-$, $V_{\text{REFCM}} = (\text{REF}^+ + \text{REF}^-)/2$;

$V_{\text{IN}} = \text{IN}^+ - \text{IN}^-$, $V_{\text{INCM}} = (\text{IN}^+ + \text{IN}^-)/2$.

Note 4: F_0 pin tied to GND or to V_{CC} or to external conversion clock source with $f_{\text{EOSC}} = 153600\text{Hz}$ unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: $F_0 = 0\text{V}$ (internal oscillator) or $f_{\text{EOSC}} = 153600\text{Hz} \pm 2\%$ (external oscillator).

Note 8: $F_0 = V_{\text{CC}}$ (internal oscillator) or $f_{\text{EOSC}} = 128000\text{Hz} \pm 2\%$ (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance $C_{\text{LOAD}} = 20\text{pF}$.

Note 11: The external oscillator is connected to the F_0 pin. The external oscillator frequency, f_{EOSC} , is expressed in kHz.

Note 12: The converter uses the internal oscillator.

$F_0 = 0\text{V}$ or $F_0 = V_{\text{CC}}$.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND (Pin 1) with a 10 μ F tantalum capacitor in parallel with 0.1 μ F ceramic capacitor as close to the part as possible.

REF⁺ (Pin 2), REF⁻ (Pin 3): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF⁺, is maintained more positive than the reference negative input, REF⁻, by at least 0.1V.

IN⁺ (Pin 4), IN⁻ (Pin 5): Differential Analog Input. The voltage on these pins can have any value between GND - 0.3V and V_{CC} + 0.3V. Within these limits the converter bipolar input range ($V_{IN} = IN^+ - IN^-$) extends from $-0.5 \cdot (V_{REF})$ to $0.5 \cdot (V_{REF})$. Outside this input range the converter produces unique overrange and underrange output codes.

GND (Pin 6): Ground. Connect this pin to a ground plane through a low impedance connection.

CS (Pin 7): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as CS is HIGH. A LOW-to-HIGH transition on CS during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 8): Three-State Digital Output. During the Data Output period this pin is used as the serial data output. When the chip select CS is HIGH ($CS = V_{CC}$) the SDO pin is in a high impedance state. During the Conversion and Sleep periods this pin is used as the conversion status output. The conversion status can be observed by pulling CS LOW.

SCK (Pin 9): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as the digital output for the internal serial interface clock during the Data Output period. In External Serial Clock Operation mode, SCK is used as the digital input for the external serial interface clock during the Data Output period. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock Operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of CS.

F₀ (Pin 10): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F₀ pin is connected to V_{CC} ($F_0 = V_{CC}$), the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F₀ pin is connected to GND ($F_0 = 0V$), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F₀ is driven by an external clock signal with a frequency f_{EOSC} , the converter uses this signal as its system clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

FUNCTIONAL BLOCK DIAGRAM

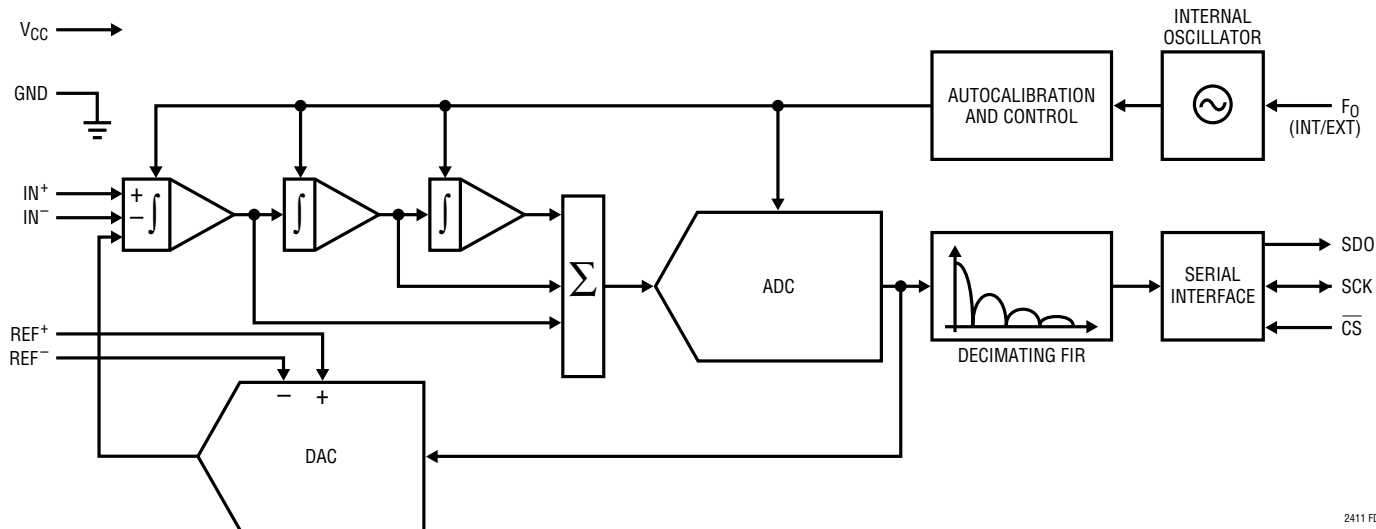


Figure 1

TEST CIRCUITS



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2411 is a low power, delta-sigma analog-to-digital converter with an easy to use 3-wire serial interface (see Figure 1). Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 2). The 3-wire interface consists of serial data output (SDO), serial clock (SCK) and chip select (\overline{CS}).

Initially, the LTC2411 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as \overline{CS} is HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

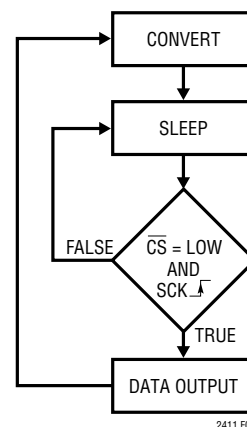


Figure 2. LTC2411 State Transition Diagram

APPLICATIONS INFORMATION

Once \overline{CS} is pulled LOW, the device begins outputting the conversion result. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 32 bits are read out of the ADC or when \overline{CS} is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the \overline{CS} and SCK pins, the LTC2411 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50 or 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2411 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2411 achieves a minimum of 110dB rejection at the line frequency (50Hz or 60Hz $\pm 2\%$).

Ease of Use

The LTC2411 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

The LTC2411 performs offset and full-scale calibrations in every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2411 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 1.9V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 1ms. The POR signal clears all internal registers. Following the POR signal, the LTC2411 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the REF^+ and REF^- pins covers the entire range from GND to V_{CC} . For correct converter operation, the REF^+ pin must always be more positive than the REF^- pin.

The LTC2411 can accept a differential reference voltage from 0.1V to V_{CC} . The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the converter's overall INL performance. A reduced reference voltage will also improve the converter performance when operated with an external conversion clock (external F_0 signal) at substantially higher output data rates.

APPLICATIONS INFORMATION

Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the IN^+ and IN^- input pins extending from $GND - 0.3V$ to $V_{CC} + 0.3V$. Outside these limits the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits the LTC2411 converts the bipolar differential input signal, $V_{IN} = IN^+ - IN^-$, from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range the converter indicates the overrange or the underrange condition using distinct output codes.

Input signals applied to IN^+ and IN^- pins may extend by 300mV below ground and above V_{CC} . In order to limit any fault current, resistors of up to 5k may be added in series with the IN^+ and IN^- pins without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between these series resistors and the corresponding pins as low as possible; therefore, the resistors should be located as close as practical to the pins. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if $V_{REF} = 5V$. This error has a very strong temperature dependency.

Output Data Format

The LTC2411 serial output data stream is 32 bits long. The first 3 bits represent status information indicating the sign and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution. The third and fourth bits together are also used to indicate an underrange condition (the differential input voltage is below $-FS$) or an overrange condition (the differential input voltage is above $+FS$).

Bit 31 (first output bit) is the end of conversion (\overline{EOC}) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the \overline{CS} pin is LOW.

This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0 , this bit is HIGH. If V_{IN} is <0 , this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides the underrange or overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above $+FS$. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below $-FS$.

The function of these bits is summarized in Table 1.

Table 1. LTC2411 Status Bits

Input Range	Bit 31 \overline{EOC}	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB
$V_{IN} \geq 0.5 \cdot V_{REF}$	0	0	1	1
$0V \leq V_{IN} < 0.5 \cdot V_{REF}$	0	0	1	0
$-0.5 \cdot V_{REF} \leq V_{IN} < 0V$	0	0	0	1
$V_{IN} < -0.5 \cdot V_{REF}$	0	0	0	0

Bits 28-5 are the 24-bit conversion result MSB first.

Bit 5 is the least significant bit (LSB).

Bits 4-0 are sub LSBs below the 24-bit level. Bits 4-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever \overline{CS} is HIGH, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, \overline{CS} must first be driven LOW. \overline{EOC} is seen at the SDO pin of the device once \overline{CS} is pulled LOW. \overline{EOC} changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 (\overline{EOC}) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched

APPLICATIONS INFORMATION

on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as EOC (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the IN⁺ and IN⁻ pins is maintained within the $-0.3V$ to $(V_{CC} + 0.3V)$ absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$. For differential input voltages greater than $+FS$, the conversion result is clamped to the value corresponding to the $+FS + 1LSB$. For differential input voltages below $-FS$, the conversion result is clamped to the value corresponding to $-FS - 1LSB$.

Frequency Rejection Selection (F₀)

The LTC2411 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for $50Hz \pm 2\%$ or $60Hz \pm 2\%$. For 60Hz rejection, F₀ should be connected to GND while for 50Hz rejection the F₀ pin should be connected to V_{CC}.

The selection of 50Hz or 60Hz rejection can also be made by driving F₀ to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be

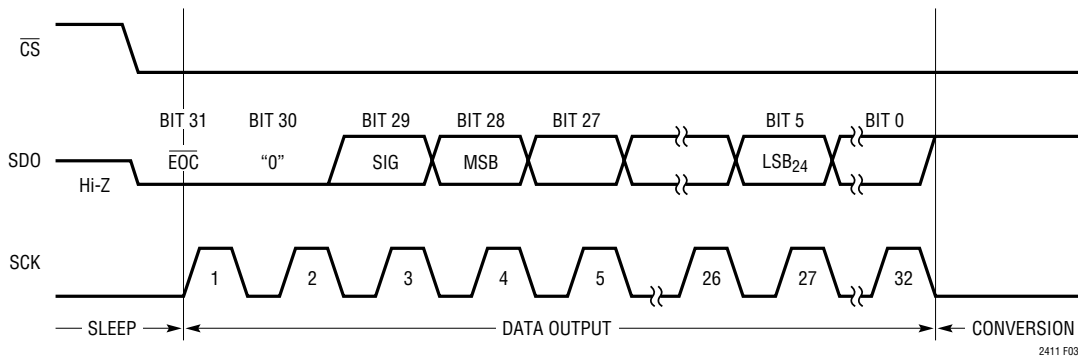


Figure 3. Output Data Timing

Table 2. LTC2411 Output Data Format

Differential Input Voltage V_{IN}^*	Bit 31 EOC	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB	Bit 27	Bit 26	Bit 25	...	Bit 0
$V_{IN}^* \geq 0.5 \cdot V_{REF}^{**}$	0	0	1	1	0	0	0	...	0
$0.5 \cdot V_{REF}^{**} - 1LSB$	0	0	1	0	1	1	1	...	1
$0.25 \cdot V_{REF}^{**}$	0	0	1	0	1	0	0	...	0
$0.25 \cdot V_{REF}^{**} - 1LSB$	0	0	1	0	0	1	1	...	1
0	0	0	1	0	0	0	0	...	0
-1LSB	0	0	0	1	1	1	1	...	1
$-0.25 \cdot V_{REF}^{**}$	0	0	0	1	1	0	0	...	0
$-0.25 \cdot V_{REF}^{**} - 1LSB$	0	0	0	1	0	1	1	...	1
$-0.5 \cdot V_{REF}^{**}$	0	0	0	1	0	0	0	...	0
$V_{IN}^* < -0.5 \cdot V_{REF}^{**}$	0	0	0	0	1	1	1	...	1

*The differential input voltage $V_{IN} = IN^+ - IN^-$.

**The differential reference voltage $V_{REF} = REF^+ - REF^-$.

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synchronized with an outside source, the LTC2411 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_0 pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC} , the LTC2411 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560 \pm 4\%$ and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 4.

Whenever an external clock is not present at the F_0 pin, the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2411 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

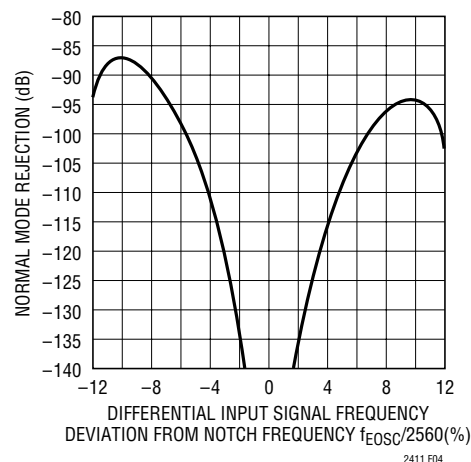


Figure 4. LTC2411 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

Table 3 summarizes the duration of each state and the achievable output data rate as a function of F_0 .

SERIAL INTERFACE PINS

The LTC2411 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

Table 3. LTC2411 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	$F_0 = \text{LOW}$ (60Hz Rejection)	133ms, Output Data Rate ≤ 7.5 Readings/s
		$F_0 = \text{HIGH}$ (50Hz Rejection)	160ms, Output Data Rate ≤ 6.2 Readings/s
	External Oscillator	$F_0 = \text{External Oscillator}$ with Frequency f_{EOSC} kHz ($f_{EOSC}/2560$ Rejection)	$20510/f_{EOSC}$ s, Output Data Rate $\leq f_{EOSC}/20510$ Readings/s
SLEEP			As Long As $\overline{\text{CS}} = \text{HIGH}$ Until $\overline{\text{CS}} = \text{LOW}$ and $\text{SCK} \uparrow$
DATA OUTPUT	Internal Serial Clock	$F_0 = \text{LOW/HIGH}$ (Internal Oscillator)	As Long As $\overline{\text{CS}} = \text{LOW}$ But Not Longer Than 1.67ms (32 SCK cycles)
		$F_0 = \text{External Oscillator}$ with Frequency f_{EOSC} kHz	As Long As $\overline{\text{CS}} = \text{LOW}$ But Not Longer Than $256/f_{EOSC}$ ms (32 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{\text{CS}} = \text{LOW}$ But Not Longer Than $32/f_{SCK}$ ms (32 SCK cycles)

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Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 9) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2411 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the \overline{CS} pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 8), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When \overline{CS} (Pin 7) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If \overline{CS} is LOW during the convert or sleep state, SDO will output \overline{EOC} . If \overline{CS} is LOW during the conversion phase, the \overline{EOC} bit appears HIGH on the SDO pin. Once the conversion is complete, \overline{EOC} goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS} = \text{LOW}$.

Chip Select Input (\overline{CS})

The active LOW chip select, \overline{CS} (Pin 7), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the \overline{CS} signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2411 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the \overline{CS} pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with $\overline{CS} = \text{LOW}$).

Finally, \overline{CS} can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding \overline{CS} will force the ADC to continuously convert at the maximum output rate selected by F_0 .

SERIAL INTERFACE TIMING MODES

The LTC2411's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator ($F_0 = \text{LOW}$ or $F_0 = \text{HIGH}$) or an external oscillator connected to the F_0 pin. Refer to Table 4 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a \overline{CS} signal to monitor and control the state of the conversion cycle, see Figure 5.

Table 4. LTC2411 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	\overline{CS} and SCK	\overline{CS} and SCK	Figures 5, 6
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 7
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS} \downarrow$	$\overline{CS} \downarrow$	Figures 8, 9
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 10

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The serial clock mode is selected on the falling edge of \overline{CS} . To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each \overline{CS} falling edge.

The serial data output pin (SDO) is Hi-Z as long as \overline{CS} is HIGH. At any time during the conversion cycle, \overline{CS} may be pulled LOW in order to monitor the state of the converter. While \overline{CS} is pulled LOW, \overline{EOC} is output to the SDO pin. $\overline{EOC} = 1$ while a conversion is in progress and $\overline{EOC} = 0$ if the device is in the sleep state. Independent of \overline{CS} , the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC} = 0$), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while \overline{CS} is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. \overline{EOC} can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC} = 1$) indicating a conversion is in progress.

At the conclusion of the data cycle, \overline{CS} may remain LOW and \overline{EOC} monitored as an end-of-conversion interrupt. Alternatively, \overline{CS} may be driven HIGH setting SDO to Hi-Z.

As described above, \overline{CS} may be pulled LOW at any time in order to monitor the conversion status.

Typically, \overline{CS} remains LOW during the data output state. However, the data output state may be aborted by pulling \overline{CS} HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 6. On the rising edge of \overline{CS} , the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 7. \overline{CS} may be permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 1ms after V_{CC} exceeds 1.9V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

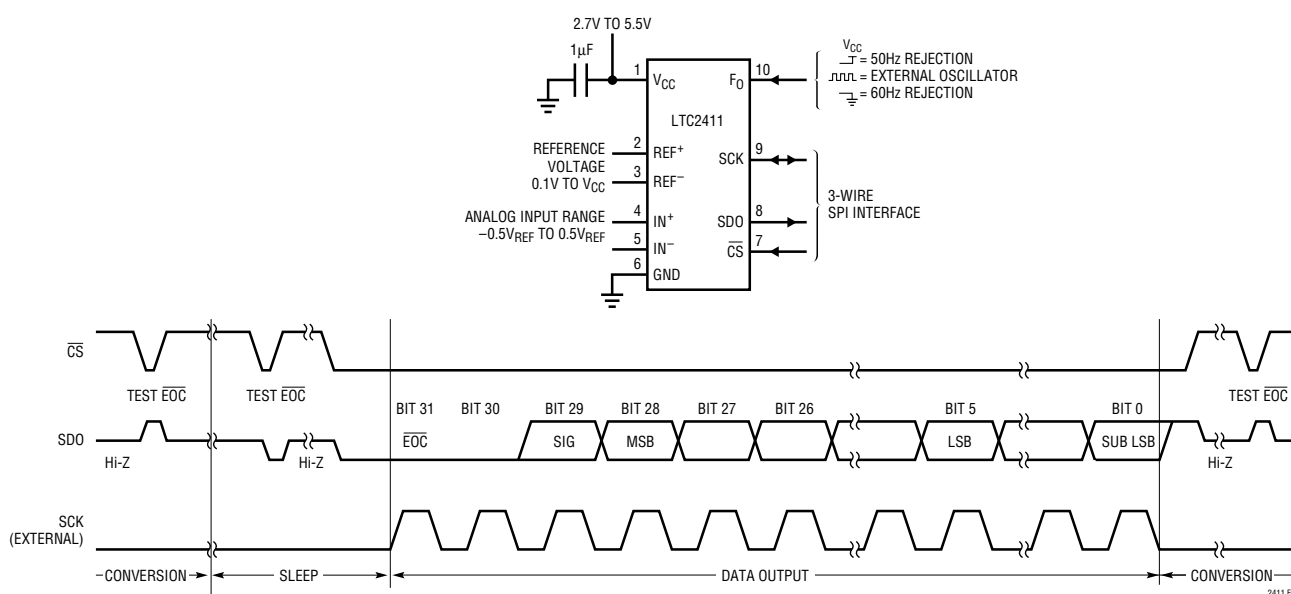


Figure 5. External Serial Clock, Single Cycle Operation

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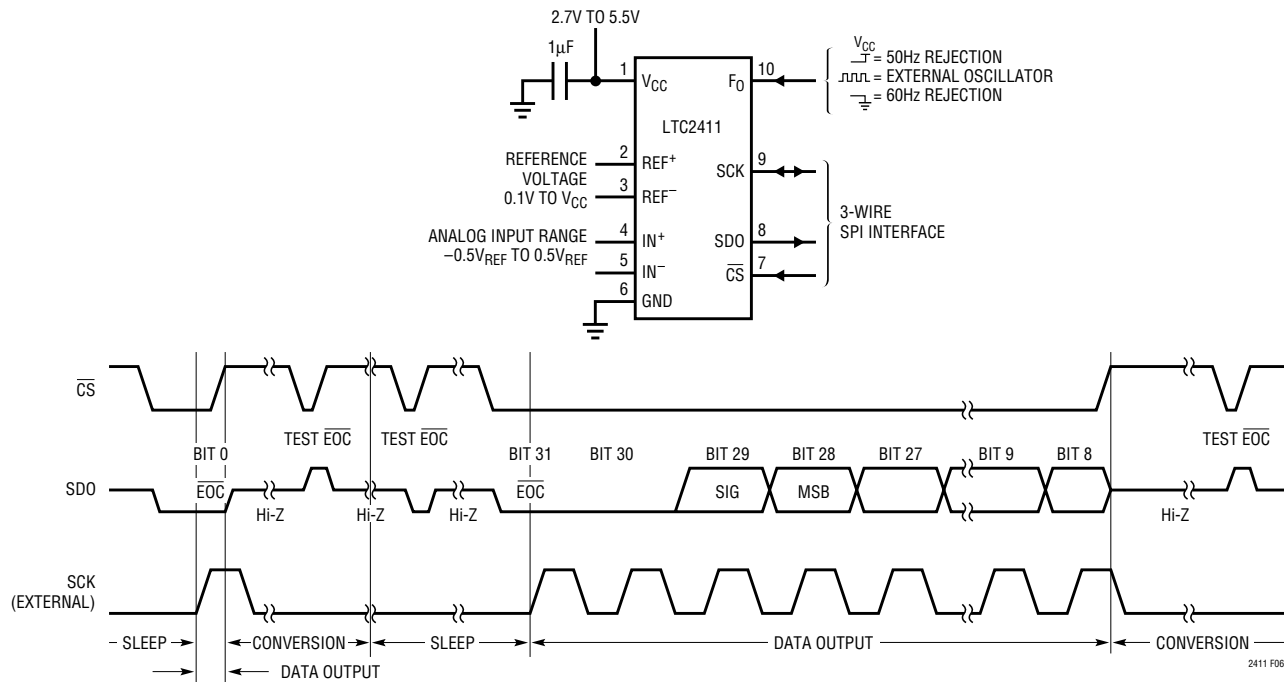


Figure 6. External Serial Clock, Reduced Data Output Length

Since \overline{CS} is tied LOW, the end-of-conversion (\overline{EOC}) can be continuously monitored at the SDO pin during the convert and sleep states. \overline{EOC} may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC} = 1$ while the conversion is in progress and $\overline{EOC} = 0$ once the conversion enters the low power sleep state. On the falling edge of \overline{EOC} , the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. \overline{EOC} can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH ($\overline{EOC} = 1$) indicating a new conversion has begun.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a \overline{CS} signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of \overline{CS} . The device will not

enter the internal serial clock mode if SCK is driven LOW on the falling edge of \overline{CS} . An internal weak pull-up resistor is active on the SCK pin during the falling edge of \overline{CS} ; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as \overline{CS} is HIGH. At any time during the conversion cycle, \overline{CS} may be pulled LOW in order to monitor the state of the converter. Once \overline{CS} is pulled LOW, SCK goes LOW and \overline{EOC} is output to the SDO pin. $\overline{EOC} = 1$ while a conversion is in progress and $\overline{EOC} = 0$ if the device is in the sleep state.

When testing \overline{EOC} , if the conversion is complete ($\overline{EOC} = 0$), the device will exit the sleep state and enter the data output state if \overline{CS} remains LOW. In order to prevent the device from exiting the low power sleep state, \overline{CS} must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of \overline{CS} (if $\overline{EOC} = 0$) or $t_{EOCtest}$ after \overline{EOC} goes LOW (if \overline{CS} is LOW during the falling edge of \overline{EOC}). The value of $t_{EOCtest}$ is $23\mu s$ if the device is using its internal oscillator ($F_0 = \text{logic LOW or HIGH}$). If F_0 is driven by an external oscillator of

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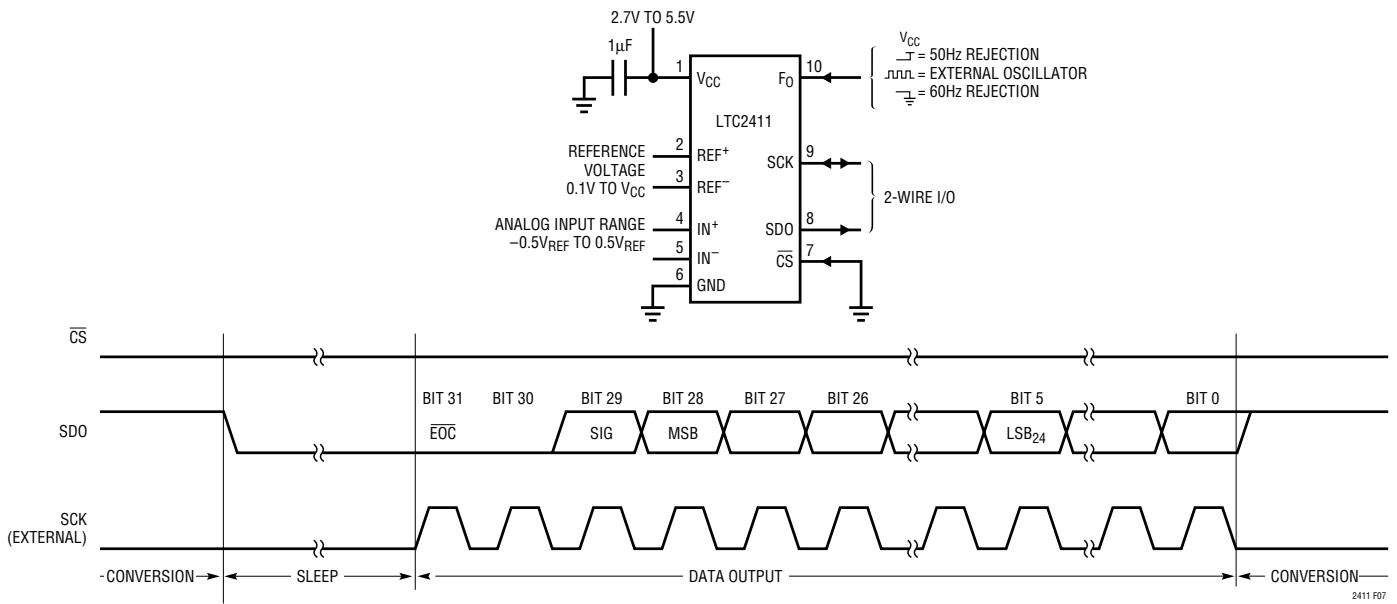


Figure 7. External Serial Clock, CS = 0 Operation

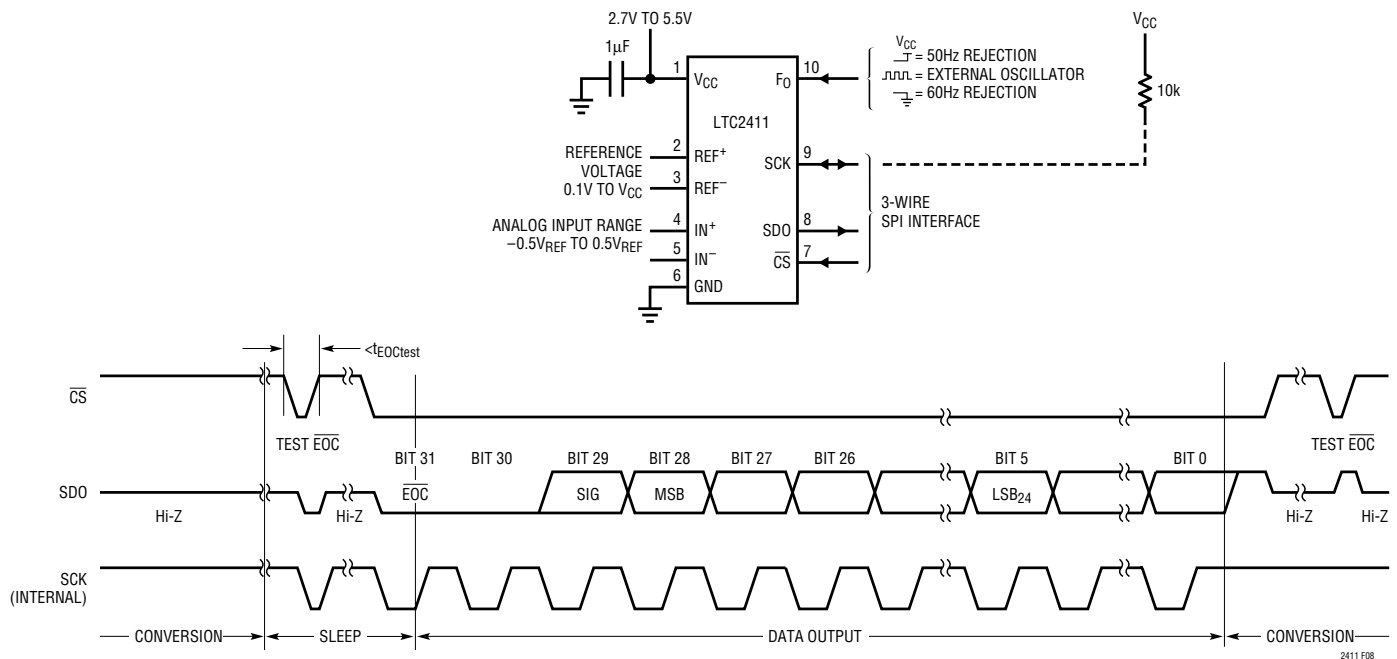


Figure 8. Internal Serial Clock, Single Cycle Operation

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frequency f_{EOSC} , then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If \overline{CS} is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

If \overline{CS} remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. \overline{EOC} can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC} = 1$), SCK stays HIGH and a new conversion starts.

Typically, \overline{CS} remains LOW during the data output state. However, the data output state may be aborted by pulling \overline{CS} HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. On the rising edge of \overline{CS} , the device aborts the data output state and immediately initiates a

new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If \overline{CS} is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of \overline{CS} . This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling \overline{CS} HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2411's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2411's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of \overline{CS} , the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next \overline{CS} falling edge, the device will remain in the internal SCK timing mode.

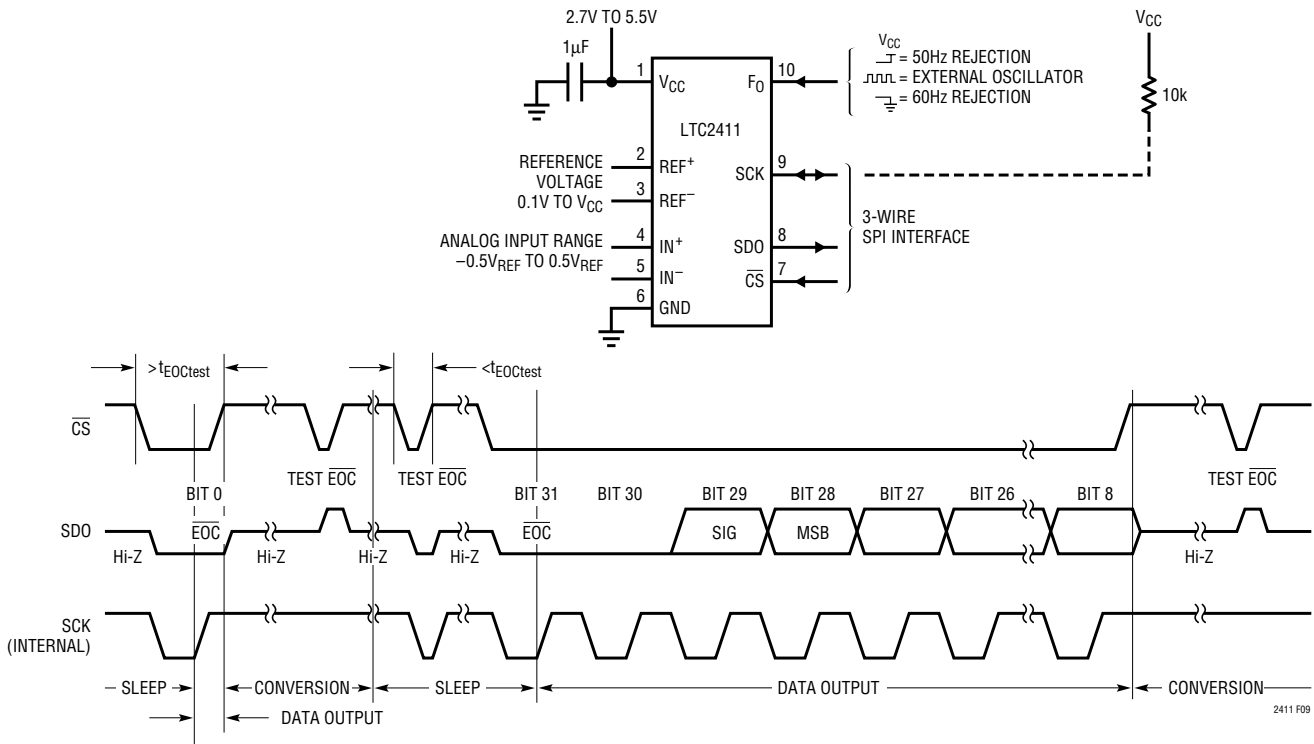


Figure 9. Internal Serial Clock, Reduced Data Output Length

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A similar situation may occur during the sleep state when \overline{CS} is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC} = 0$), SCK will go LOW. Once \overline{CS} goes HIGH (within the time period defined above as $t_{\overline{EOC}test}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before \overline{CS} goes low again. This is not a concern under normal conditions where \overline{CS} remains LOW after detecting $\overline{EOC} = 0$. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. \overline{CS} may be permanently tied to ground, simplifying the user interface or isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 1ms after V_{CC} exceeds 1.9V. An internal

weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC} = 1$). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC} = 0$) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. \overline{EOC} can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC} = 1$) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

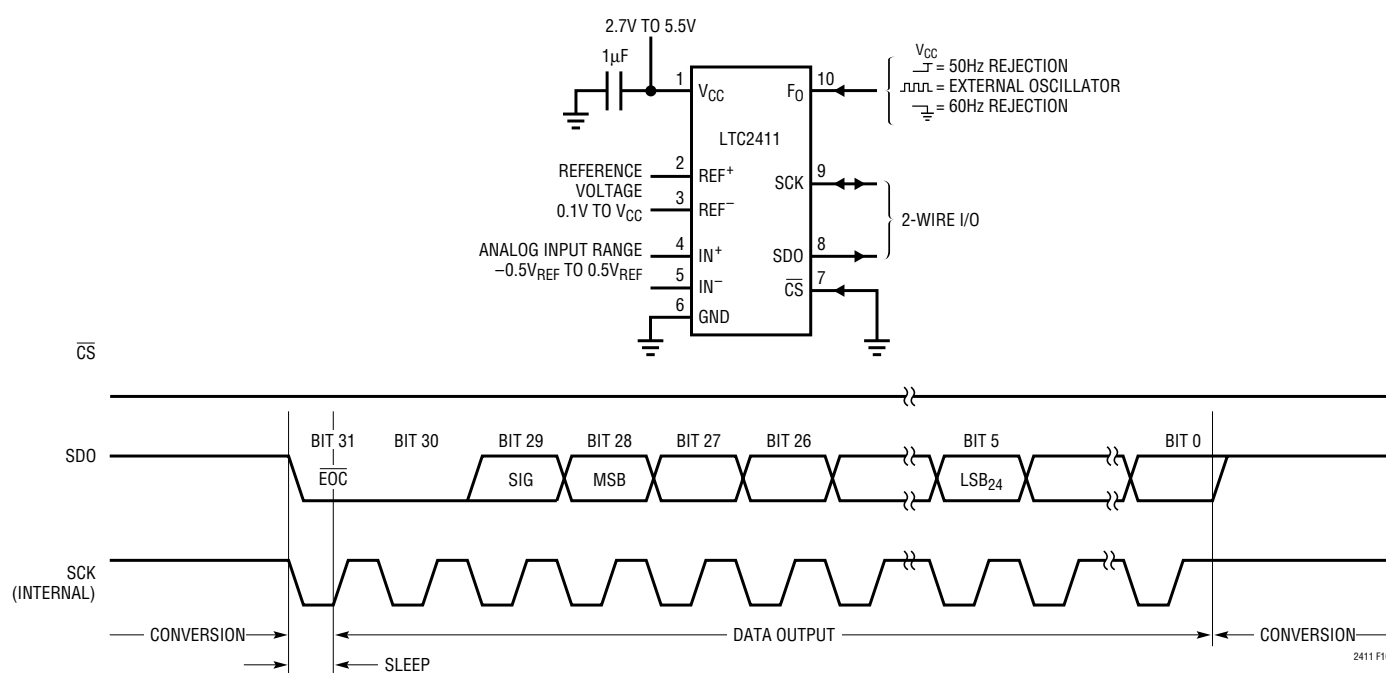


Figure 10. Internal Serial Clock, $\overline{CS} = 0$ Continuous Operation

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BRIDGE APPLICATIONS

Typical strain gauge based bridges deliver only 2mV/Volt of excitation. As the maximum reference voltage of the LTC2411 is 5V, remote sensing of applied excitation without additional circuitry requires that excitation be limited to 5V. This gives only 10mV full scale, which can be resolved to 1 part in 5000 without averaging. For many solid state sensors, this is comparable to the sensor. Averaging 64 samples however reduces the noise level by a factor of eight, bringing the resolving power to 1 part in 40000, comparable to better weighing systems. Hysteresis and creep effects in the load cells are typically much greater than this. Most applications that require strain measurements to this level of accuracy are measuring slowly changing phenomena, hence the time required to average a large number of readings is usually not an issue. For those systems that require accurate measurement of a small incremental change on a significant tare weight, the lack of history effects in the LTC2400 family is of great benefit.

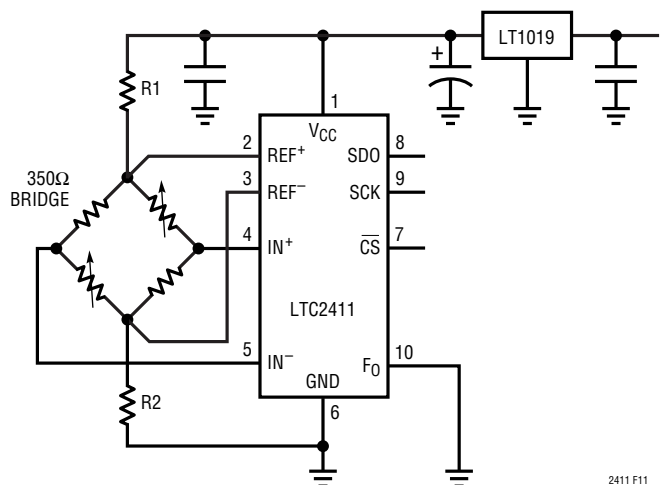
For those applications that cannot be fulfilled by the LTC2411 alone, compensating for error in external amplification can be done effectively due to the “no latency” feature of the LTC2411. No latency operation allows samples of the amplifier offset and gain to be interleaved with weighing measurements. The use of correlated double sampling allows suppression of 1/f noise, offset and thermocouple effects within the bridge. Correlated double sampling involves alternating the polarity of excitation and dealing with the reversal of input polarity mathematically. Alternatively, bridge excitation can be increased to as much as $\pm 10V$, if one of several precision attenuation techniques is used to produce a precision divide operation on the reference signal. Another option is the use of a reference within the 5V input range of the LTC2411 and developing excitation via fixed gain, or LTC1043 based voltage multiplication, along with remote feedback in the excitation amplifiers, as shown in Figures 16 and 18.

Figure 11 shows an example of a simple bridge connection. Note that it is suitable for any bridge application where measurement speed is not of the utmost importance. For many applications where large vessels are weighed, the average weight over an extended period of

time is of concern and short term weight is not readily determined due to movement of contents, or mechanical resonance. Often, large weighing applications involve load cells located at each load bearing point, the output of which can be summed passively prior to the signal processing circuitry, actively with amplification prior to the ADC, or can be digitized via multiple ADC channels and summed mathematically. The mathematical summation of the output of multiple LTC2411's provides the benefit of a root square reduction in noise. The low power consumption of the LTC2411 makes it attractive for multidrop communication schemes where the ADC is located within the load-cell housing.

A direct connection to a load cell is perhaps best incorporated into the load-cell body, as minimizing the distance to the sensor largely eliminates the need for protection devices, RFI suppression and wiring. The LTC2411 exhibits extremely low temperature dependent drift. As a result, exposure to external ambient temperature ranges does not compromise performance. The incorporation of any amplification considerably complicates thermal stability, as input offset voltages and currents, temperature coefficient of gain settling resistors all become factors.

The circuit in Figure 12 shows an example of a simple amplification scheme. This example produces a differential output with a common mode voltage of 2.5V, as determined by the bridge. The use of a true three amplifier



R1 AND R2 CAN BE USED TO INCREASE TOLERABLE AC COMPONENT ON REF SIGNALS

Figure 11. Simple Bridge Connection

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instrumentation amplifier is not necessary, as the LTC2411 has common mode rejection far beyond that of most amplifiers. The LTC1051 is a dual autozero amplifier that can be used to produce a gain of 30 before its input referred noise dominates the LTC2411 noise. This example shows a gain of 34, that is determined by a feedback network built using a resistor array containing 8 individual resistors. The resistors are organized to optimize temperature tracking in the presence of thermal gradients. The second LTC1051 buffers the low noise input stage from the transient load steps produced during conversion.

The gain stability and accuracy of this approach is very good, due to a statistical improvement in resistor matching due to individual error contribution being reduced. A gain of 34 may seem low, when compared to common practice in earlier generations of load-cell interfaces, however the accuracy of the LTC2411 changes the rationale. Achieving high gain accuracy and linearity at higher gains may prove difficult, while providing little benefit in terms of noise reduction.

At a gain of 100, the gain error that could result from typical open-loop gain of 160dB is -1ppm , however, worst-case is at the minimum gain of 116dB, giving a gain

error of -158ppm . Worst-case gain error at a gain of 34, is -54ppm . The use of the LTC1051A reduces the worst-case gain error to -33ppm . The advantage of gain higher than 34, then becomes dubious, as the input referred noise sees little improvement¹ and gain accuracy is potentially compromised.

Note that this 4-amplifier topology has advantages over the typical integrated 3-amplifier instrumentation amplifier in that it does not have the high noise level common in the output stage that usually dominates when an instrumentation amplifier is used at low gain. If this amplifier is used at a gain of 10, the gain error is only 10ppm and input referred noise is reduced to $0.15\mu\text{V}_{\text{RMS}}$. The buffer stages can also be configured to provide gain of up to 50 with high gain stability and linearity.

Figure 13 shows an example of a single amplifier used to produce single-ended gain. This topology is best used in applications where the gain setting resistor can be made to match the temperature coefficient of the strain gauges. If the bridge is composed of precision resistors, with only one or two variable elements, the reference arm of the

¹Input referred noise for $A_V = 34$ for approximately $0.05\mu\text{V}_{\text{RMS}}$, whereas at a gain of 50, it would be $0.048\mu\text{V}_{\text{RMS}}$.

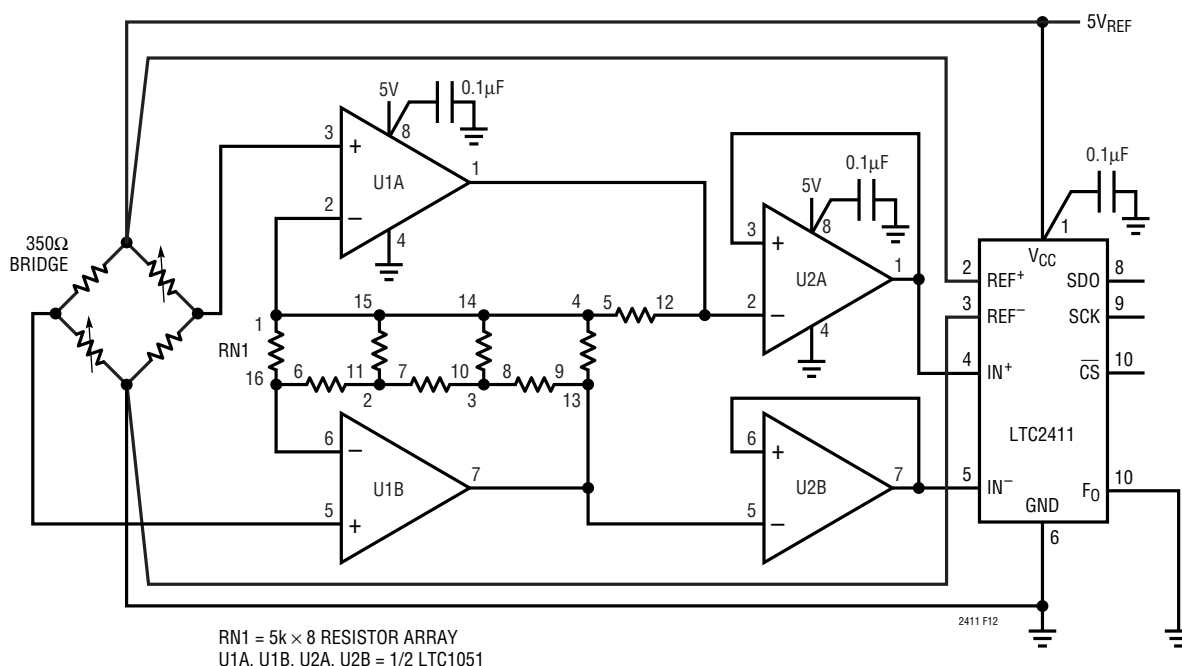


Figure 12. Using Autozero Amplifiers to Reduce Input Referred Noise

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bridge can be made to act in conjunction with the feedback resistor to determine the gain. If the feedback resistor is incorporated into the design of the load cell, using resistors which match the temperature coefficient of the load-cell elements, good results can be achieved without the need for resistors with a high degree of absolute accuracy. The common mode voltage in this case, is again a function of the bridge output. Differential gain as used with a 350Ω bridge is $A_V = 1 + R_2/(R_1 + 175\Omega)$. Common mode gain is half the differential gain. The maximum differential signal that can be used is $1/4 V_{REF}$, as opposed to $1/2 V_{REF}$ in the 2-amplifier topology above.

Remote Half Bridge Interface

As opposed to full bridge applications, typical half bridge applications must contend with nonlinearity in the bridge output, as signal swing is often much greater. Applications include RTD's, thermistors and other resistive elements that undergo significant changes over their span. For single variable element bridges, the nonlinearity of the half bridge output can be eliminated completely; if the reference arm of the bridge is used as the reference to the ADC, as shown in Figure 14. The LTC2411 can accept inputs up to $1/2 V_{REF}$. Hence, the reference resistor R1 must be at least 2x the highest value of the variable resistor.

In the case of 100Ω platinum RTD's, this would suggest a value of 800Ω for R1. Such a low value for R1 is not advisable due to self-heating effects. A value of 25.5k is shown for R1, reducing self-heating effects to acceptable levels for most sensors.

The basic circuit shown in Figure 14 shows connections for a full 4-wire connection to the sensor, which may be located remotely. The differential input connections will reject induced or coupled 60Hz interference, however, the reference inputs do not have the same rejection. If 60Hz or other noise is present on the reference input, a low pass filter is recommended as shown in Figure 15. Note that you cannot place a large capacitor directly at the junction of R1 and R2, as it will store charge from the sampling process. A better approach is to produce a low pass filter decoupled from the input lines with a high value resistor (R3).

The use of a third resistor in the half bridge, between the variable and fixed elements gives essentially the same result as the two resistor version, but has a few benefits. If, for example, a 25k reference resistor is used to set the excitation current with a 100Ω RTD, the negative reference input is sampling the same external node as the positive input, but may result in errors if used with a long cable. For short cable applications, the errors may be acceptably low. If instead the single 25k resistor is re-

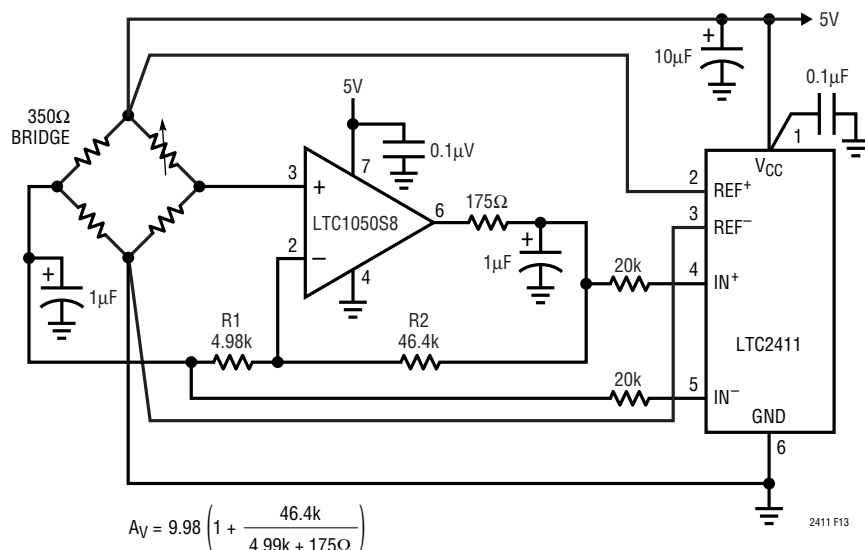


Figure 13. Bridge Amplification Using a Single Amplifier

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placed with a 10k 5% and a 10k 0.1% reference resistor, the noise level introduced at the reference, at least at higher frequencies, will be reduced. A filter can be introduced into the network, in the form of one or more capacitors, or ferrite beads, as long as the sampling pulses are not translated into an error. The reference voltage is also reduced, but this is not undesirable, as it will decrease the value of the LSB, although, not the input referred noise level.

The circuit shown in Figure 15 shows a more rigorous example of Figure 14, with increased noise suppression and more protection for remote applications.

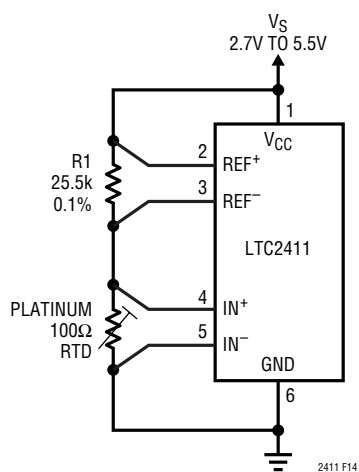


Figure 14. Remote Half Bridge Interface

Figure 16 shows an example of gain in the excitation circuit and remote feedback from the bridge. The LTC1043s provide voltage multiplication, providing $\pm 10V$ from a 5V reference with only 1ppm error. The amplifiers are used at unity-gain and, hence, introduce a very little error due to gain error or due to offset voltages. A $1\mu V/^\circ C$ offset voltage drift translates into 0.05ppm/ $^\circ C$ gain error. Simpler alternatives, with the amplifiers providing gain using resistor arrays for feedback, can produce results that are similar to bridge sensing schemes via attenuators. Note that the amplifiers must have high open-loop gain or gain error will be a source of error. The fact that input offset voltage has relatively little effect on overall error may lead one to use low performance amplifiers for this application. Note that the gain of a device such as an LF156, (25V/mV over temperature) will produce a worst-case error of $-180ppm$ at a noise gain of 3, such as would be encountered in an inverting gain of 2, to produce $-10V$ from a 5V reference.

The error associated with the 10V excitation would be $-80ppm$. Hence, overall reference error could be as high as 130ppm, the average of the two.

Figure 18 shows a similar scheme to provide excitation using resistor arrays to produce precise gain. The circuit is configured to provide 10V and $-5V$ excitation to the bridge, producing a common mode voltage at the input to the LTC2411 of 2.5V, maximizing the AC input range for applications where induced 60Hz could reach amplitudes up to $2V_{RMS}$.

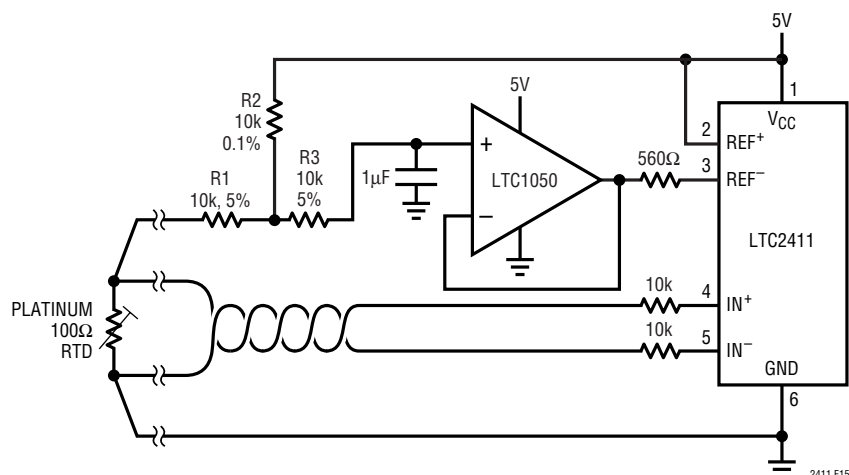


Figure 15. Remote Half Bridge Sensing with Noise Suppression on Reference

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The last two example circuits could be used where multiple bridge circuits are involved and bridge output can be multiplexed onto a single LTC2411, via an inexpensive multiplexer such as the 74HC4052.

Figure 17 shows the use of an LTC2411 with a differential multiplexer. This is an inexpensive multiplexer that will contribute some error due to leakage if used directly with the output from the bridge, or if resistors are inserted as

a protection mechanism from overvoltage. Although the bridge output may be within the input range of the A/D and multiplexer in normal operation, some thought should be given to fault conditions that could result in full excitation voltage at the inputs to the multiplexer or ADC. The use of amplification prior to the multiplexer will largely eliminate errors associated with channel leakage developing error voltages in the source impedance.

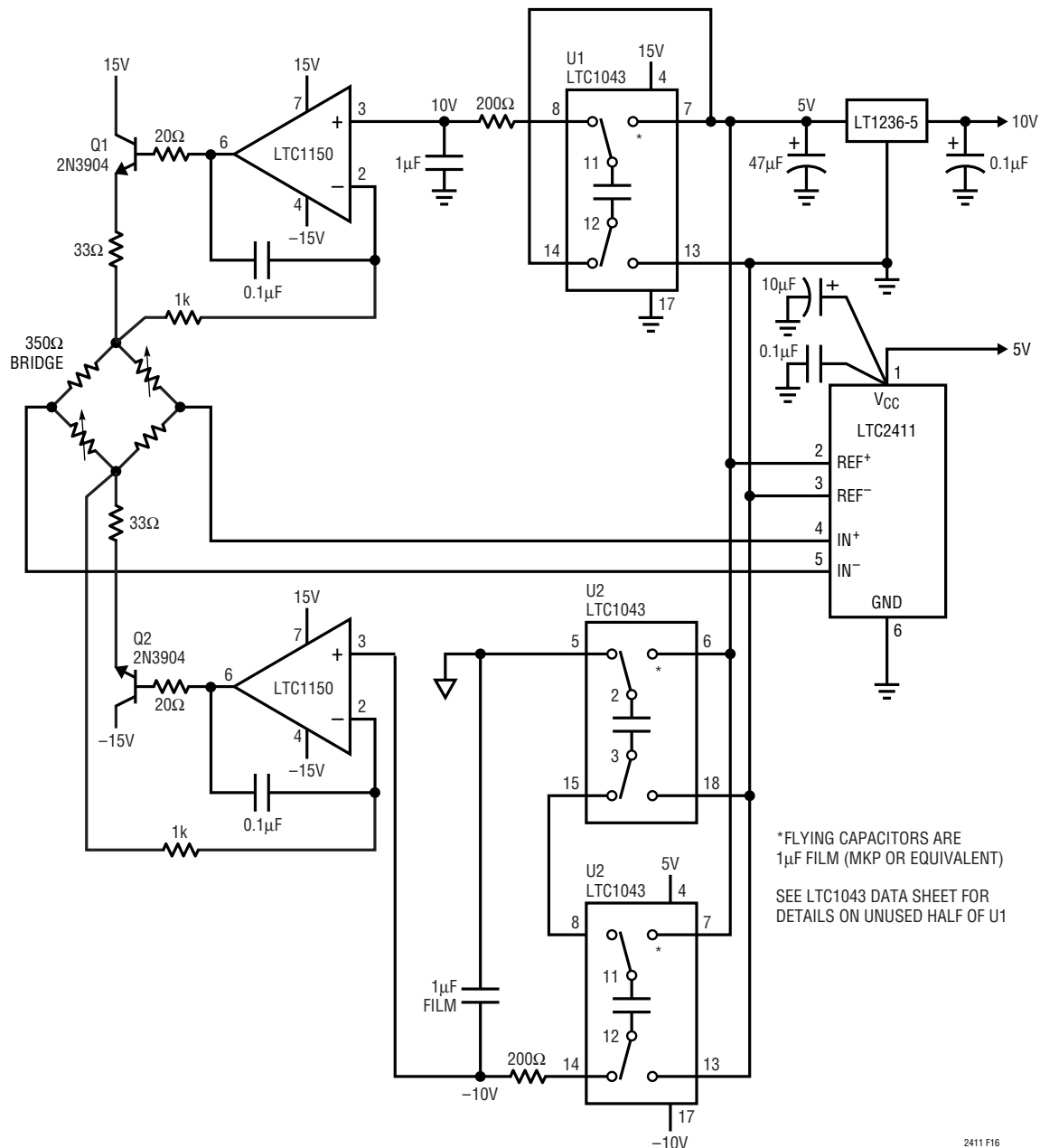


Figure 16. LTC1043 Provides Precise 3X Reference for Excitation Voltages

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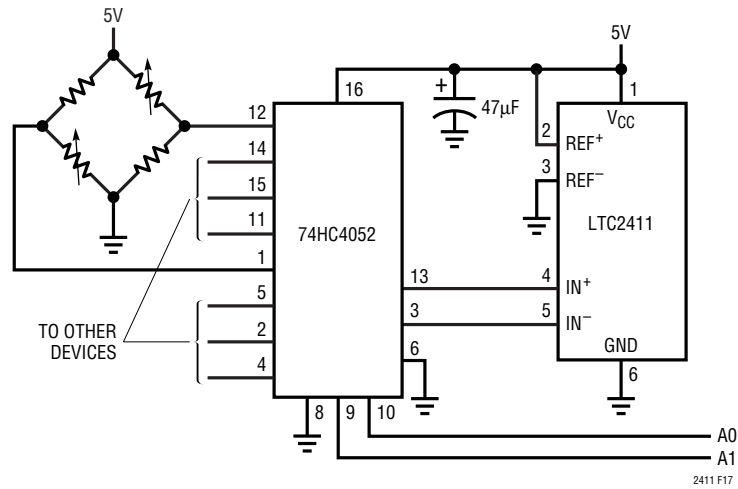
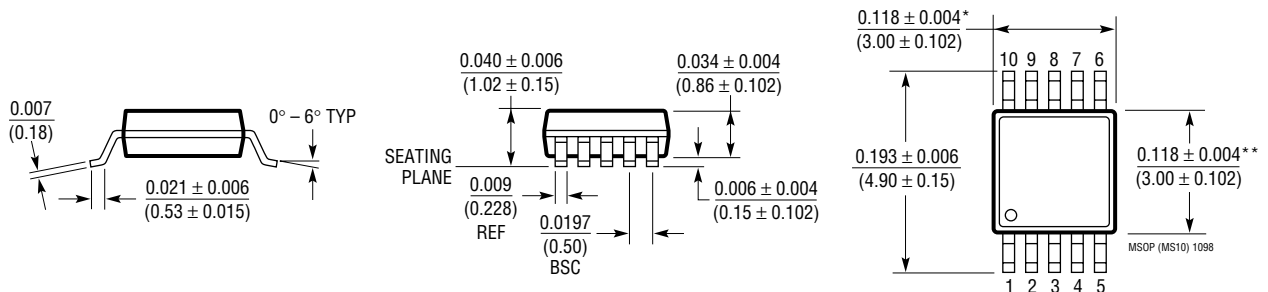


Figure 17. Use a Differential Multiplexer to Expand Channel Capability

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS10 Package 10-Lead Plastic MSOP (LTC DWG # 05-08-1661)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

