ISP1104

Advanced Universal Serial Bus transceiver

Rev. 01 — 26 August 2002 **Product data**

1. General description

The ISP1104 Universal Serial Bus (USB) transceiver is fully compliant with the *Universal Serial Bus Specification Rev. 2.0 (full-speed section)*. It is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, Personal Digital Assistants (PDAs) and Information Appliances (IAs).

It allows USB Application Specific Integrated Circuits (ASICs) and Programmable Logic Devices (PLDs) with power supply voltages from 1.65 to 3.6 V to interface with the physical layer of the USB. It has an integrated 5 V to 3.3 V voltage regulator for direct powering via the USB supply line V_{BUS}. It has an integrated voltage detector to detect the presence of the V_{BUS} line voltage ($V_{CC(5.0)}$). When V_{BUS} ($V_{CC(5.0)}$) is lost, the pins (D+, D–) can be shared with other serial protocols.

The ISP1104 can transmit and receive USB data at full-speed (12 Mbit/s). It allows single and differential input modes selectable by a MODE input.

The ISP1104 is available in the HBCC16 package.

2. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0 (full-speed section)*
- Integrated 5 V to 3.3 V voltage regulator for powering via USB line V_{BUS}
- V_{BUS} presence indication on pin VBUSDET
- Used as USB device transceiver or USB transceiver
- Supports full-speed (12 Mbit/s) serial data rate
- Stable RCV output during SE0 condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports I/O voltage range from 1.65 to 3.6 V
- ±12 kV ESD protection at pins D+, D-, $V_{CC(5.0)}$ and GND
- Full industrial operating temperature range from –40 to +85 °C
- Available in HBCC16 package.

3. Applications

- Portable electronic devices, such as:
  - Mobile phone
  - Digital still camera
  - Personal Digital Assistant (PDA)
  - Information Appliance (IA).

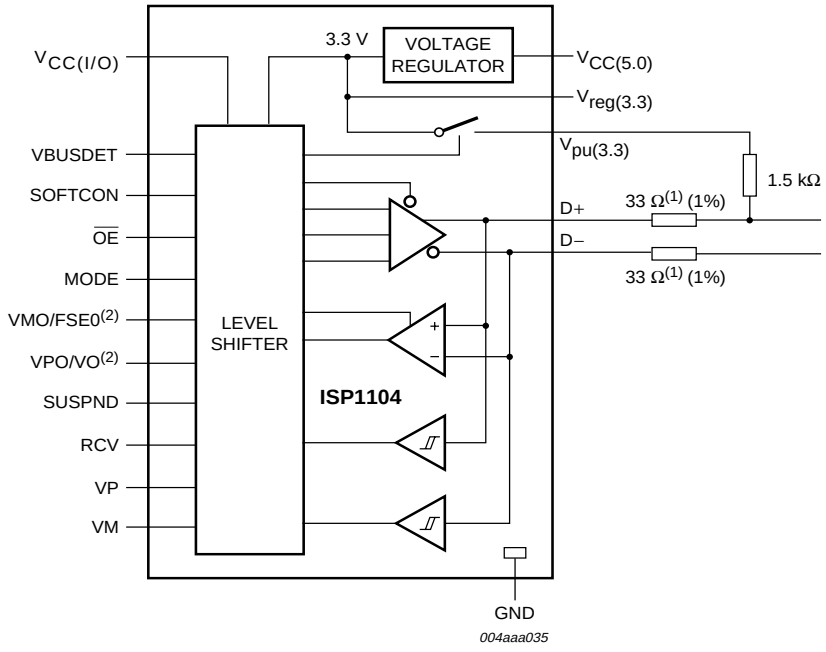
4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1104W[1]	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2

[1] The ground terminal of the ISP1104W is connected to the exposed diepad (heatsink).

5. Functional diagram



(1) Use a resistor of 39 Ω ±1% for a USB v2.0 compliant output impedance range.

(2) Pin function depends on the device function, see Section 7.2.

Fig 1. Functional diagram.

6. Pinning information

6.1 Pinning

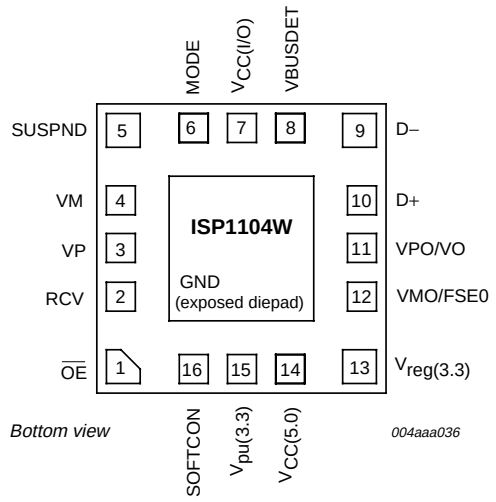


Fig 2. Pinning diagram HBCC16.

6.2 Pin description

Table 2: Pin description

Symbol[1]	Pin	Type	Description
$\overline{OE}$	1	I	input for output enable (CMOS level with respect to $V_{CC(I/O)}$, active LOW); enables the transceiver to transmit data on the USB bus
RCV	2	O	differential data receiver output (CMOS level with respect to $V_{CC(I/O)}$); driven LOW when input SUSPND is HIGH; the output state of RCV is preserved and stable during an SE0 condition
VP	3	O	single-ended D+ receiver output (CMOS level with respect to $V_{CC(I/O)}$); for external detection of single-ended zero (SE0), error conditions and speed of connected device; driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$
VM	4	O	single-ended D– receiver output (CMOS level with respect to $V_{CC(I/O)}$); for external detection of single-ended zero (SE0), error conditions and speed of connected device; driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$
SUSPND	5	I	suspend input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level
MODE	6	I	mode input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables the differential input mode (VPO, VMO) whereas a LOW level enables a single-ended input mode (VO, FSE0); see Table 4 and Table 5
GND	-[2]	-	ground supply

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
$V_{CC(I/O)}$	7	-	Supply voltage for digital I/O pins (1.65 to 3.6 V). When $V_{CC(I/O)}$ is not connected, the pins (D+, D–) are in three-state. This supply pin is totally independent of $V_{CC(5.0)}$ and $V_{reg(3.3)}$ and must never exceed the $V_{reg(3.3)}$ voltage.
VBUSDET	8	O	V_{BUS} indicator output (CMOS level with respect to $V_{CC(I/O)}$). When V_{BUS} is above 4.0 V, then the output is HIGH and when V_{BUS} is below 3.6 V, then the output is LOW.
D–	9	AI/O	negative USB data bus connection (analog, differential)
D+	10	AI/O	positive USB data bus connection (analog, differential); connect a 1.5 kΩ resistor to pin $V_{pu(3.3)}$
VPO/VO	11	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger); see Table 4 and Table 5
VMO/FSE0	12	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger); see Table 4 and Table 5
$V_{reg(3.3)}$	13	-	regulated supply voltage output (3.0 to 3.6 V); a decoupling capacitor of at least 0.1 µF is required
$V_{CC(5.0)}$	14	-	supply voltage input (4.0 to 5.5 V); can be connected directly to the USB supply line V_{BUS}
$V_{pu(3.3)}$	15	-	pull-up supply voltage (3.3 V ± 10%); connect an external 1.5 kΩ resistor on D+ (full-speed); pin function is controlled by input SOFTCON: **SOFTCON = LOW —** $V_{pu(3.3)}$ floating (high impedance); ensures zero pull-up current **SOFTCON = HIGH —** $V_{pu(3.3)}$ = 3.3 V; internally connected to $V_{reg(3.3)}$
SOFTCON	16	I	software controlled USB connection input; a HIGH level applies 3.3 V to pin $V_{pu(3.3)}$, which is connected to an external 1.5 kΩ pull-up resistor; this allows USB connect or disconnect signalling to be controlled by software

[1] Symbol names with an overscore (e.g. $\overline{NAME}$) indicate active LOW signals.

[2] Down bonded to the exposed diepad.

7. Functional description

7.1 Function selection

Table 3: Function table

SUSPND	$\overline{OE}$	(D+, D–)	RCV	VP/VM	Function
L	L	driving and receiving	active	active	normal driving (differential receiver active)
L	H	receiving[1]	active	active	receiving
H	L	driving	inactive[2]	active	driving during 'suspend' (differential receiver inactive)
H	H	high-Z[1]	inactive[2]	active	low-power state

[1] Signal levels on pins (D+, D–) are determined by other USB devices and external pull-up or pull-down resistors.

[2] In the 'suspend' mode (pin SUSPND = HIGH), the differential receiver is inactive and the output RCV is always LOW. Out-of-suspend ('K') signalling is detected via the single-ended receivers VP and VM.

7.2 Operating functions

Table 4: Driving function using single-ended input data interface [($\overline{OE}$ = L) (MODE = L)]

FSE0	VO	Data
L	L	differential logic 0
L	H	differential logic 1
H	L	SE0
H	H	SE0

Table 5: Driving function using differential input data interface [($\overline{OE}$ = L) (MODE = H)]

VMO	VPO	Data
L	L	SE0
L	H	differential logic 1
H	L	differential logic 0
H	H	illegal state

Table 6: Receiving function ($\overline{OE}$ = H)

(D+, D–)	RCV	VP[1]	VM[1]
differential logic 0	L	L	H
differential logic 1	H	H	L
SE0	RCV*[2]	L	L

[1] VP = VM = H indicates the sharing mode ($V_{CC(5.0)}$ is disconnected).

[2] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is stable during the SE0 period.

7.3 Power supply configurations

The ISP1104 can be used with different power supply configurations, which can be changed dynamically. Table 8 provides an overview of the power supply configuration.

Normal mode — Both $V_{CC(I/O)}$ and $V_{CC(5.0)}$ are connected. For 5 V operation, $V_{CC(5.0)}$ is connected to a 5 V source (4.0 to 5.5 V). The internal voltage regulator then produces 3.3 V for USB connections. $V_{CC(I/O)}$ is independently connected to a voltage source (1.65 to 3.6 V), depending on the supply voltage of the external circuit.

Disable mode — $V_{CC(I/O)}$ is not connected and $V_{CC(5.0)}$ is connected. In this mode, the internal circuits of the ISP1104 ensure that the (D+, D–) pins are in three-state and the power consumption drops to the low-power (suspended) state level. Some hysteresis is built into the detection of $V_{CC(I/O)}$ lost.

Sharing mode — $V_{CC(I/O)}$ is connected and $V_{CC(5.0)}$ is below 3.6 V. In this mode, pins (D+, D–) are made three-state and the ISP1104 allows external signals of up to 3.6 V to share the (D+, D–) lines. The internal circuits of the ISP1104 ensure that virtually no current (maximum 10 μA) is drawn via the (D+, D–) lines. The power consumption through pin $V_{CC(I/O)}$ and pin $V_{CC(5.0)}$ drops to the low-power (suspended) state level. Pins VP and VM are driven HIGH and pins VBUSDET and RCV are driven LOW to indicate this mode. Some hysteresis is built into the detection of $V_{CC(5.0)}$ lost.

Table 7: Pin states in the Disable or Sharing mode

Pins	Disable mode	Sharing mode
$V_{CC(5.0)}$	5 V input	below 3.6 V
$V_{reg(3.3)}$	3.3 V output	pulled-down
$V_{CC(I/O)}$	not present	1.65 to 3.6 V input
$V_{pu(3.3)}$	high impedance (off)	high impedance (off)
D+, D–	high impedance	high impedance
VP, VM	invalid[1]	H
RCV	invalid[1]	L
VBUSDET	invalid[1]	L
VPO/VO, VMO/FSE0, MODE, SUSPND, $\overline{OE}$, SOFTCON	high impedance	high impedance

[1] High impedance or driven LOW.

Table 8: Power supply configuration overview

$V_{CC(5.0)}$	$V_{CC(I/O)}$	Configuration	Special characteristics
connected	connected	Normal mode	-
connected	not connected	Disable mode	(D+, D–) and $V_{pu(3.3)}$ high impedance; VP, VM, RCV: invalid[1]
not connected	connected	Sharing mode	(D+, D–) and $V_{pu(3.3)}$ high impedance; VP, VM driven HIGH; RCV driven LOW; VBUSDET driven LOW; $V_{reg(3.3)}$ pulled-down

[1] High impedance or driven LOW.

8. Electrostatic discharge (ESD)

8.1 ESD protection

The pins that are connected to the USB connector (D+, D-, $V_{CC(5.0)}$ and GND) have a minimum of ±12 kV ESD protection. The ±12 kV measurement is limited by the test equipment. Capacitors of 4.7 µF connected from $V_{reg(3.3)}$ to GND and $V_{CC(5.0)}$ to GND are required to achieve this ±12 kV ESD protection (see Figure 3).

The ISP1104 can withstand ±12 kV using the Human Body Model and ±5 kV using the Contact Discharge Method as specified in *IEC 61000-4-2*.

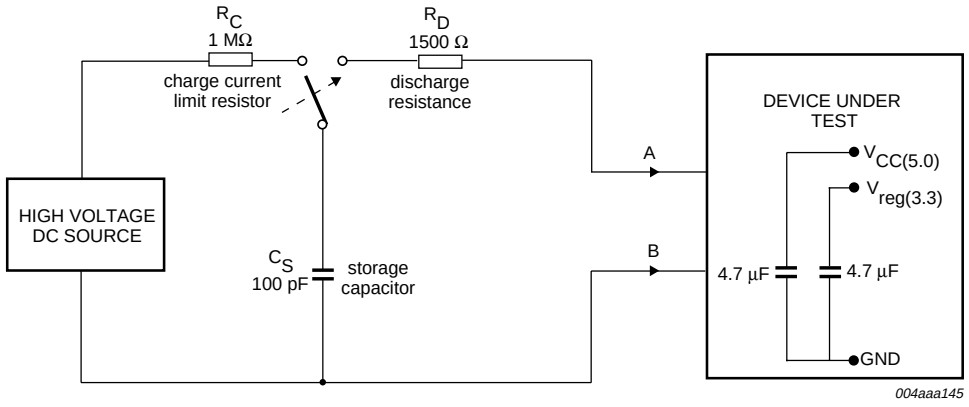


Fig 3. Human Body ESD test model.

8.2 ESD test conditions

For a detailed report on test set-up and results, send a request to **wired.support@philips.com**.

9. Limiting values

Table 9: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5.0)}$	supply voltage		–0.5	+6.0	V
$V_{CC(I/O)}$	I/O supply voltage		–0.5	+4.6	V
V_I	DC input voltage		–0.5	$V_{CC(I/O)}$ + 0.5	V
$I_{latchup}$	latch-up current	V_I = –1.8 to +5.4 V	-	100	mA
V_{esd}	electrostatic discharge voltage	I_{LI} < 1 µA			
		pins (D+, D–), $V_{CC(5.0)}$ and GND	-	±12000[1]	V
		other pins	-	±2000	V
T_{stg}	storage temperature		–40	+125	°C

[1] Testing equipment limits measurement to only ±12 kV. Capacitors needed on $V_{CC(5.0)}$ and $V_{reg(3.3)}$ (see Section 8).

10. Recommended operating conditions

Table 10: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5.0)}$	supply voltage		4.0	5.0	5.5	V
$V_{CC(I/O)}$	I/O supply voltage		1.65	-	3.6	V
V_I	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{I(AI/O)}$	input voltage on type AI/O pins (D+, D–)		0	-	3.6	V
T_{amb}	ambient temperature		–40	-	+85	°C

11. Static characteristics

Table 11: Static characteristics: supply pins

$V_{CC(5.0)}$ = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{reg(3.3)}$	regulated supply voltage output	internal regulator option; $I_{load} \leq 300$ µA	[1]	3.0[2]	3.3	3.6	V
I_{CC}	operating supply current	transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins (D+, D–)		-	4	8[3]	mA
$I_{CC(I/O)}$	operating I/O supply current	transmitting and receiving at 12 Mbit/s		-	1	2[3]	mA
$I_{CC(idle)}$	supply current during full-speed idle and SE0	idle: V_{D+} > 2.7 V, V_{D-} < 0.3 V; SE0: V_{D+} < 0.3 V, V_{D-} < 0.3 V	[4]	-	-	500	µA
$I_{CC(I/O)(static)}$	static I/O supply current	idle, SE0 or suspend		-	-	20	µA
$I_{CC(susp)}$	suspend supply current	SUSPND = H	[4]	-	-	100	µA
$I_{CC(dis)}$	disable mode supply current	$V_{CC(I/O)}$ not connected	[4]	-	-	100	µA

Table 11: Static characteristics: supply pins…*continued*

$V_{CC(5.0)}$ = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(I/O)(sharing)}$	sharing mode I/O supply current	$V_{CC(5.0)}$ not connected	-	-	20	µA
$I_{Dx(sharing)}$	sharing mode load current on pins (D+, D−)	$V_{CC(5.0)}$ not connected; SOFTCON = L; V_{Dx} = 3.6 V	-	-	10	µA
$V_{th(VCC(5.0))}$	supply voltage detection threshold	1.65 V ≤ $V_{CC(I/O)}$ ≤ 3.6 V				
		supply lost	-	-	3.6	V
		supply present	4.1	-	-	V
$V_{hys(VCC(5.0))}$	supply voltage detection hysteresis	$V_{CC(I/O)}$ = 1.8 V	-	70	-	mV
$V_{th(VCC(I/O))}$	I/O supply voltage detection threshold	$V_{reg(3.3)}$ = 2.7 to 3.6 V				
		supply lost	-	-	0.5	V
		supply present	1.4	-	-	V
$V_{hys(VCC(I/O))}$	I/O supply voltage detection hysteresis	$V_{reg(3.3)}$ = 3.3 V	-	0.45	-	V

[1] I_{load} includes the pull-up resistor current via pin $V_{pu(3.3)}$.

[2] The minimum voltage is 2.7 V in the ‘suspend’ mode.

[3] Characterized only, not tested in production.

[4] Excluding any load current and $V_{pu(3.3)}$ or V_{sw} source current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typ.).

Table 12: Static characteristics: digital pins

$V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 to 3.6 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.6V_{CC(I/O)}$	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	$V_{CC(I/O)}$ − 0.15	-	-	V
		I_{OH} = 2 mA	$V_{CC(I/O)}$ − 0.4	-	-	V
Leakage current						
I_{LI}	input leakage current		-	-	±1[1]	µA
Capacitance						
C_{IN}	input capacitance	pin to GND	-	-	10	pF
Example 1: $V_{CC(I/O)}$ = 1.8 V ± 0.15 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.5	V
V_{IH}	HIGH-level input voltage		1.2	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V

Table 12: Static characteristics: digital pins…*continued*

$V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	1.5	-	-	V
		I_{OH} = 2 mA	1.25	-	-	V
Example 2: $V_{CC(I/O)}$ = 2.5 V ± 0.2 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.7	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.15	-	-	V
		I_{OH} = 2 mA	1.9	-	-	V
Example 3: $V_{CC(I/O)}$ = 3.3 V ± 0.3 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.9	V
V_{IH}	HIGH-level input voltage		2.15	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.85	-	-	V
		I_{OH} = 2 mA	2.6	-	-	V

[1] If $V_{CC(I/O)} \geq V_{reg(3.3)}$, then the leakage current will be higher than the specified value.

Table 13: Static characteristics: analog I/O pins (D+, D−)

$V_{CC(5.0)}$ = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
Differential receiver						
V_{DI}	differential input sensitivity	$\lvert V_{I(D+)} - V_{I(D-)} \rvert$	0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range	0.8	-	2.5	V
Single-ended receiver						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
Output levels						
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to +3.6 V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	2.8[1]	-	3.6	V
Leakage current						
I_{LZ}	OFF-state leakage current		-	-	±1	µA

Table 13: Static characteristics: analog I/O pins (D+, D–) *...continued*

$V_{CC(5.0)}$ = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Capacitance							
C_{IN}	transceiver capacitance	pin to GND		-	-	20	pF
Resistance							
Z_{DRV}	driver output impedance	steady-state drive	[2]	34	39	44	Ω
Z_{DRV2}	driver output impedance for USB 2.0	steady-state drive	[3]	40.5	45	49.5	Ω
Z_{INP}	input impedance			10	-	-	MΩ
R_{SW}	internal switch resistance at pin $V_{pu(3.3)}$			-	-	10	Ω
Termination							
V_{TERM}	termination voltage for upstream port pull-up (R_{pu})		[4]	3.0[5]	-	3.6	V

[1] $V_{OH(min)} = V_{reg(3.3)} - 0.2$ V.

[2] Includes external resistors of 33 Ω ±1% on both pins D+ and D–.

[3] Includes external resistors of 39 Ω ±1% on both pin D+ and D–. This range complies with *Universal Serial Bus Specification Rev. 2.0*.

[4] This voltage is available at pins $V_{reg(3.3)}$ and $V_{pu(3.3)}$.

[5] The minimum voltage is 2.7 V in the 'suspend' mode.

12. Dynamic characteristics

Table 14: Dynamic characteristics: analog I/O pins (D+, D–)

$V_{CC(5.0)}$ = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; see Figure 10; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
t_{FR}	rise time	C_L = 50 to 125 pF; 10% to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 4		4	-	20	ns
t_{FF}	fall time	C_L = 50 to 125 pF; 90% to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 4		4	-	20	ns
FRFM	differential rise/fall time matching (t_{FR}/t_{FF})	excluding the first transition from the Idle state		90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state; see Figure 7	[1]	1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	driver propagation delay (VPO/VO, VMO/FSE0 to D+, D–)	LOW-to-HIGH; see Figure 7		-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (VPO/VO, VMO/FSE0 to D+, D–)	HIGH-to-LOW; see Figure 7		-	-	18	ns
t_{PHZ}	driver disable delay ($\overline{OE}$ to D+, D–)	HIGH-to-OFF; see Figure 5		-	-	15	ns

Table 14: Dynamic characteristics: analog I/O pins (D+, D–) *...continued*

$V_{CC(5.0)}$ = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; see Figure 10; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLZ}	driver disable delay ($\overline{OE}$ to D+, D–)	LOW-to-OFF; see Figure 5	-	-	15	ns
t_{PZH}	driver enable delay ($\overline{OE}$ to D+, D–)	OFF-to-HIGH; see Figure 5	-	-	15	ns
t_{PZL}	driver enable delay ($\overline{OE}$ to D+, D–)	OFF-to-LOW; see Figure 5	-	-	15	ns
Receiver timings						
Differential receiver						
$t_{PLH(rcv)}$	propagation delay (D+, D– to RCV)	LOW-to-HIGH; see Figure 6	-	-	15	ns
$t_{PHL(rcv)}$	propagation delay (D+, D– to RCV)	HIGH-to-LOW; see Figure 6	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	propagation delay (D+, D– to VP, VM)	LOW-to-HIGH; see Figure 6	-	-	18	ns
$t_{PHL(se)}$	propagation delay (D+, D– to VP, VM)	HIGH-to-LOW; see Figure 6	-	-	18	ns

[1] Characterized only, not tested. Limits guaranteed by design.

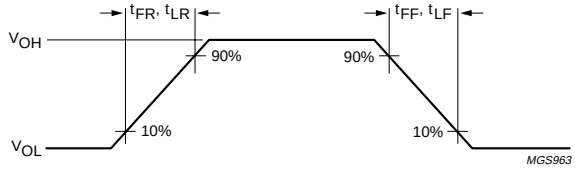


Fig 4. Rise and fall times.

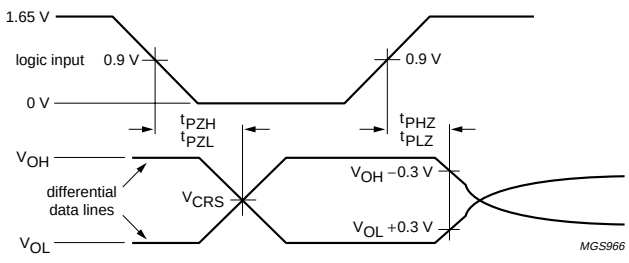


Fig 5. Timing of $\overline{OE}$ to D+, D–.

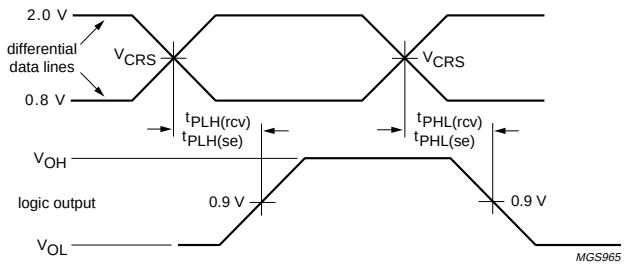


Fig 6. Timing of D+, D– to RCV, VP, VM.

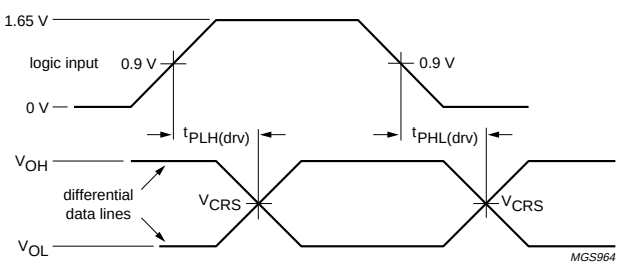
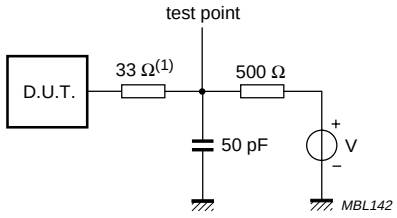


Fig 7. Timing of VPO/VO, VMO/FSE0 to D+, D–.

13. Test information



V = 0 V for t_{PZH} and t_{PHZ}.

V = $V_{reg(3.3)}$ for t_{PZL} and t_{PLZ}.

(1) Complies with USB 1.1. For USB 2.0, a resistor of 39 Ω ±1% must be used.

Fig 8. Load for enable and disable times.

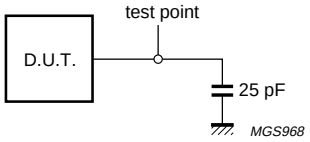
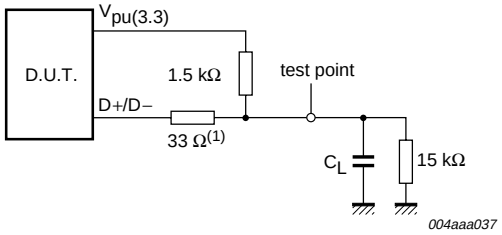


Fig 9. Load for VM, VP and RCV.



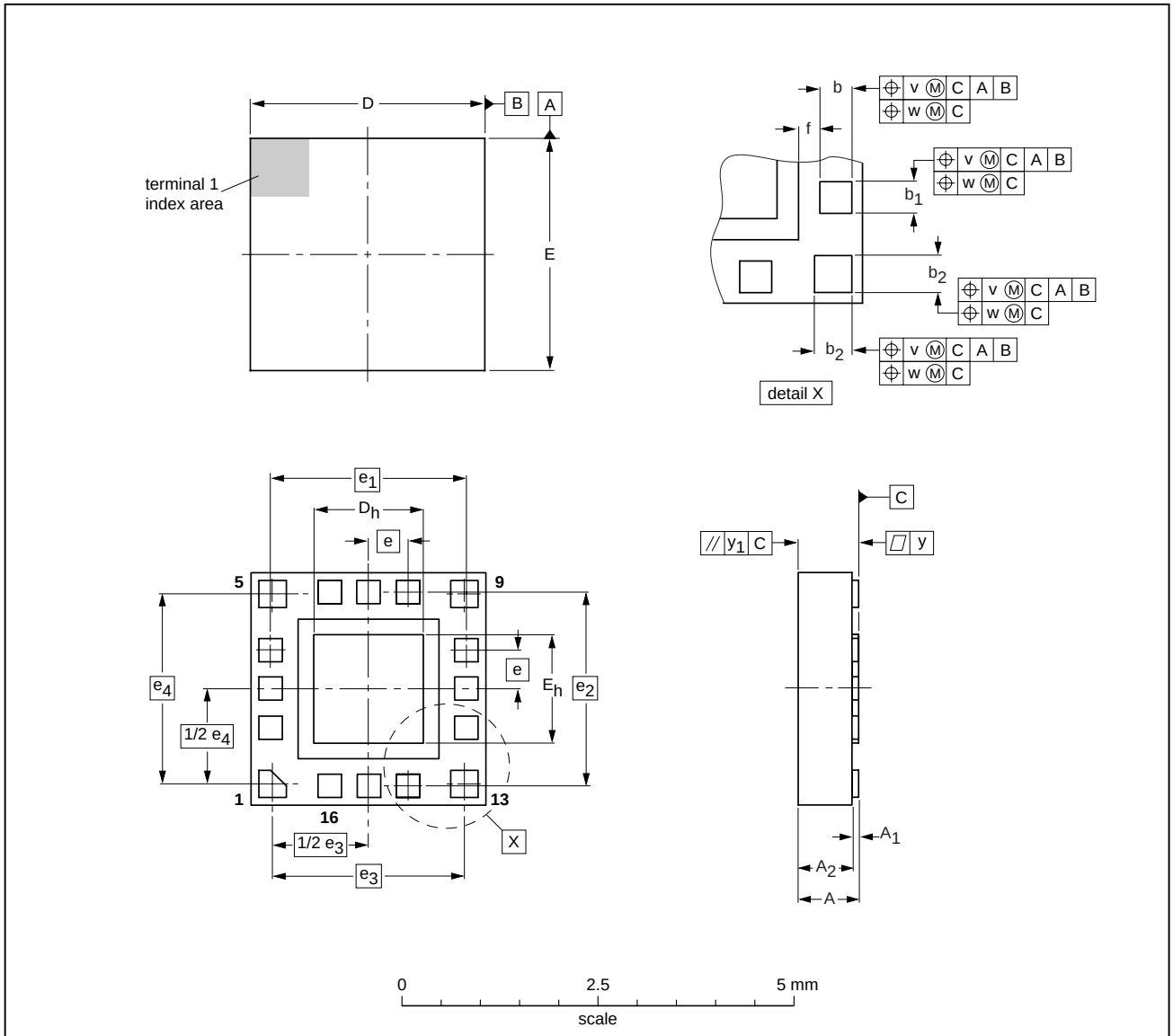
Load capacitance C_L = 50 pF (minimum or maximum timing).

(1) Complies with USB 1.1. For USB 2.0, a resistor of 39 Ω ±1% must be used.

Fig 10. Load for D+, D–.

14. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm **SOT639-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	f	v	w	y	y_1
mm	0.8	0.10 0.05	0.7 0.6	0.33 0.27	0.33 0.27	0.38 0.32	3.1 2.9	1.45 1.35	3.1 2.9	1.45 1.35	0.5	2.5	2.5	2.45	2.45	0.23 0.17	0.08	0.1	0.05	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT639-2		MO-217				01-11-13

Fig 11. HBCC16 package outline.

15. Packaging

The ISP1104W (HBCC16 package) is delivered on a Type A carrier tape, see Figure 12. The tape dimensions are given in Table 15.

The reel diameter is 330 mm. The reel is made of polystyrene (PS) and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is ±0.02 mm. The camber must not exceed 1 mm in 100 mm.

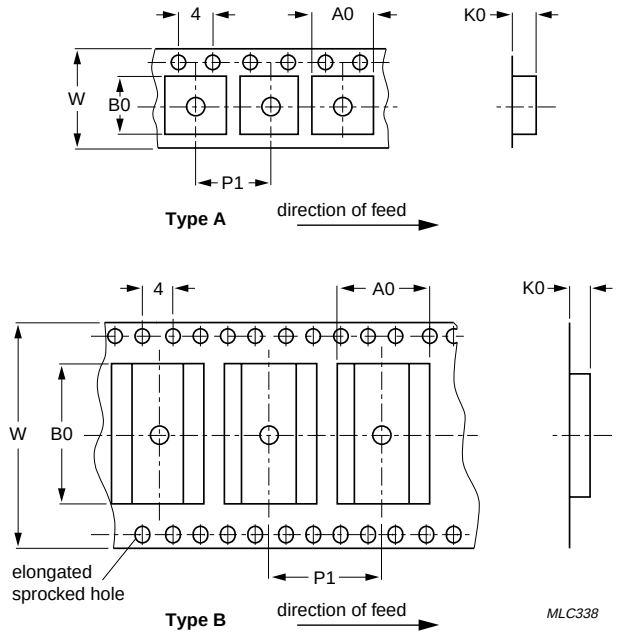


Fig 12. Carrier tape dimensions.

Table 15: Type A carrier tape dimensions for the ISP1104W

Dimension	Value	Unit
A0	3.3	mm
B0	3.3	mm
K0	1.1	mm
P1	8.0	mm
W	12.0 ±0.3	mm

16. Soldering

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Package related soldering information

Table 16: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

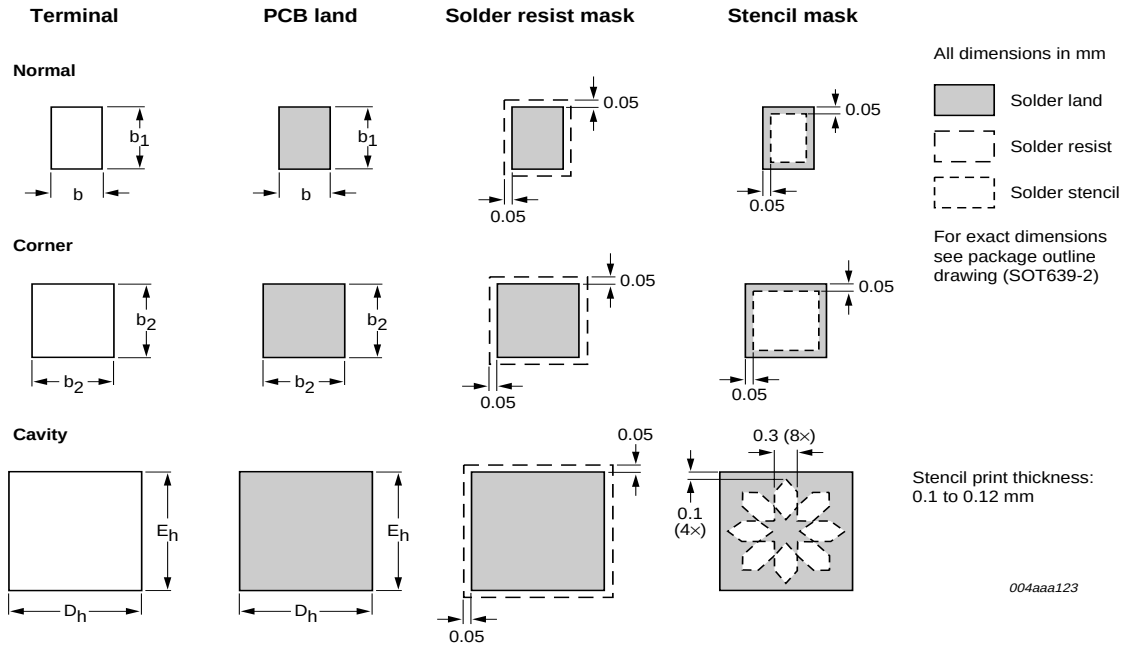
[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

17. Additional soldering information

17.1 (H)BCC packages: footprint

The surface material of the terminals on the resin protrusion consists of a 4-layer metal structure (Au, Pd, Ni and Pd). The Au + Pd layer (0.1 µm min.) ensures solderability, the Ni layer (5 µm min.) prevents diffusion, and the Pd layer on top (0.5 µm min.) ensures effective wire bonding.



Cavity: exposed diepad, either functioning as heatsink or as ground connection; only for HBCC packages.

Fig 13. (H)BCC footprint and solder resist mask dimensions.

17.2 (H)BCC packages: reflow soldering profile

The conditions for reflow soldering of (H)BCC packages are as follows:

- **Preheating time**: minimum 90 s at T = 145 to 155 °C
- **Soldering time**: minimum 90 s (BCC) or minimum 100 s (HBCC) at T > 183 °C
- **Peak temperature**:
  - Ambient temperature: $T_{amb(max)}$ = 260 °C
  - Device surface temperature: $T_{case(max)}$ = 255 °C.

18. Revision history

Table 17: Revision history

Rev	Date	CPCN	Description
01	20020826	-	Product data (9397 750 09784)

19. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397 750 09784

Contents

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