HM6288 Series

16384-word × 4-bit High Speed CMOS Static RAM

HITACHI

Description

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword × 4-bit. It realizes high speed access time (25/35 ns) and low power consumption, using CMOS process technology. It is most advantageous for the field where high speed and high density memory is required, such as cache memory for mainframes or 32-bit MPUs. The HM6288, packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting. A low power version retains data with battery backup.

Features

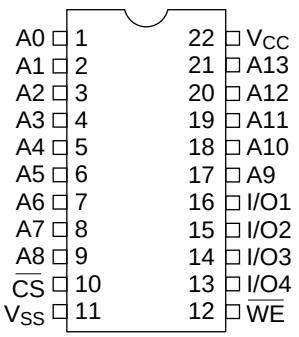
- Single 5 V supply arid high density plastic package
- High speed: fast access time 25/35 ns (max)
- Low power dissipation:
  Active mode 300 mW (typ)
  Standby mode 100 μW (typ)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times.
- Directly TTL compatible all inputs and outputs

Ordering lnformation

Type No.	Access Time	Package
HM6288P-25 HM6288P-35	25 ns 35 ns	300-mil, 22-pin plastic DIP (DP-22NB)
HM6288LP-25 HM6288LP-35	25 ns 35 ns	
HM6288JP25 HM6288JP-35	25 ns 35 ns	300-mil, 24-pin SOJ (CP-24D)
HM6288LJP-25 HM6288LJP-35	25 ns 35 ns	

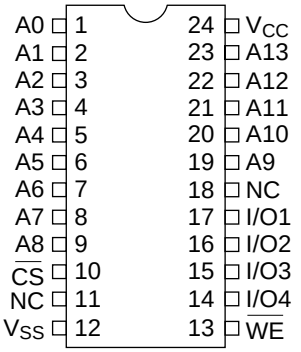
Pin Arrangement

HM6288P Series



(Top view)

HM6288JP Series

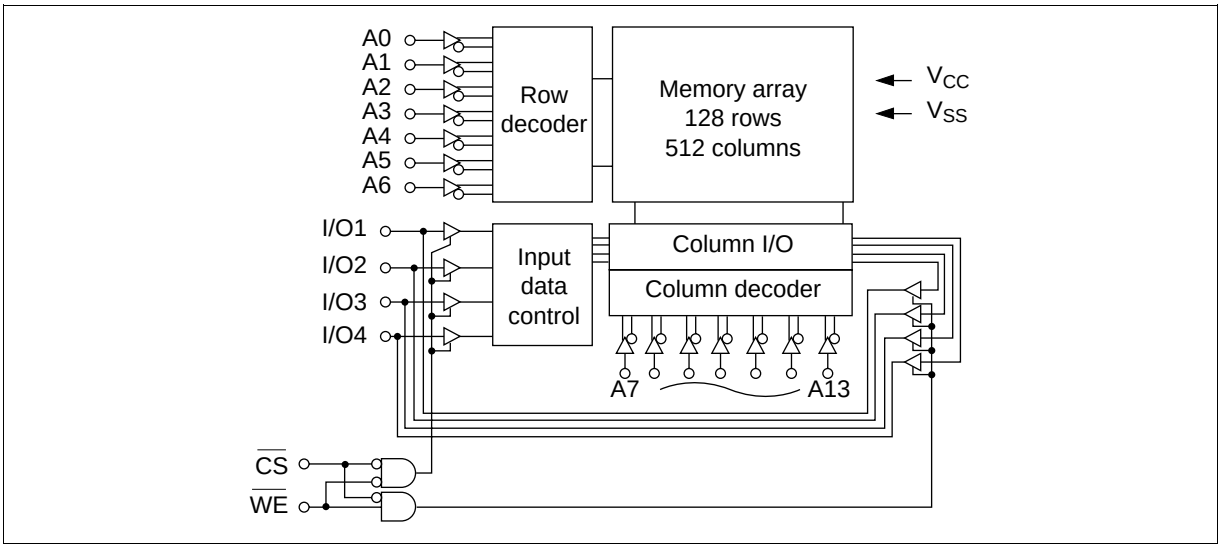


(Top view)

Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	lnput/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle 1, 2
L	L	Write	I_{CC}	Din	Write cycle 1, 2

Note: ×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5* to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Temperature under bias	Tbias	–10 to +85	°C

Note: V_T min.: –2.0 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5 *1	—	0.8	V

Note: 1. V_{IL} min.: –2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max, Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min. cycle
Standby V_{CC} current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby V_{CC} current 1	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2V, 0 V ≤ Vin ≤ 0.2V or V_{CC} – 0.2V ≤ Vin
	I_{SB1}*2	—	0.02	0.1	mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. L-version

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

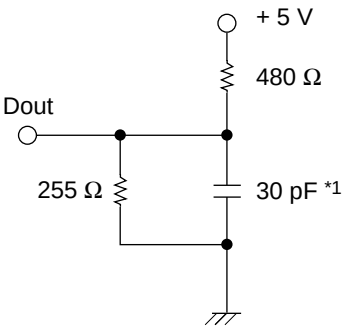
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

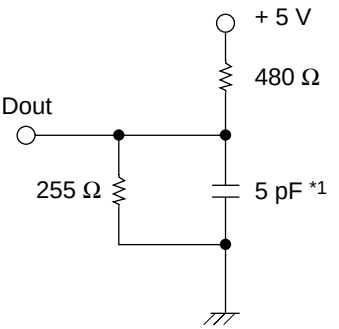
AC Characteristics

Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 5 ns
- Output load: See figure



Output load (A)



Output load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

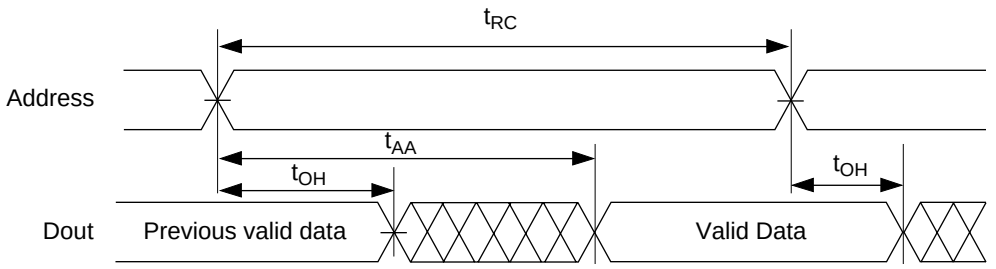
Note: 1. Including scope and jig.

Read Cycle

		HM6288-25		HM6288-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to output in low-Z	t_{LZ} *1	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ} *1	0	12	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

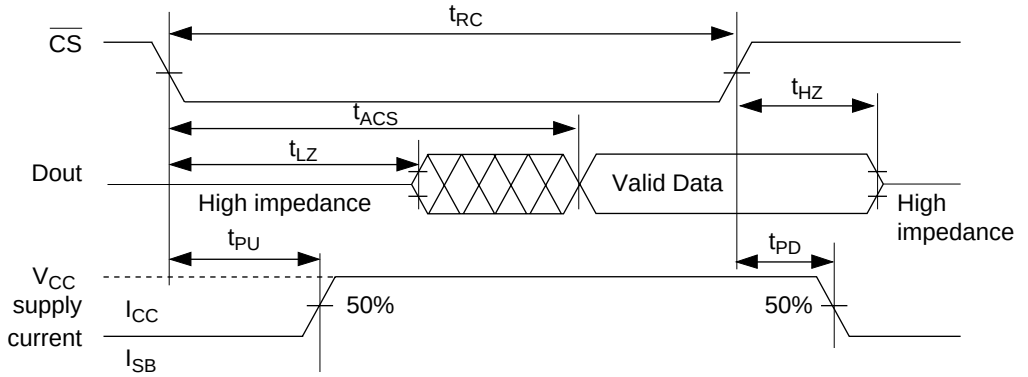
Note: 1. Transition is measured ±200 mV from steady state voltage with load (B).
These parameters are sampled and not 100% tested.

Read Timing Waveform (1)



Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected. $\overline{CS}$ = V_{IL}

Read Timing Waveform (2)



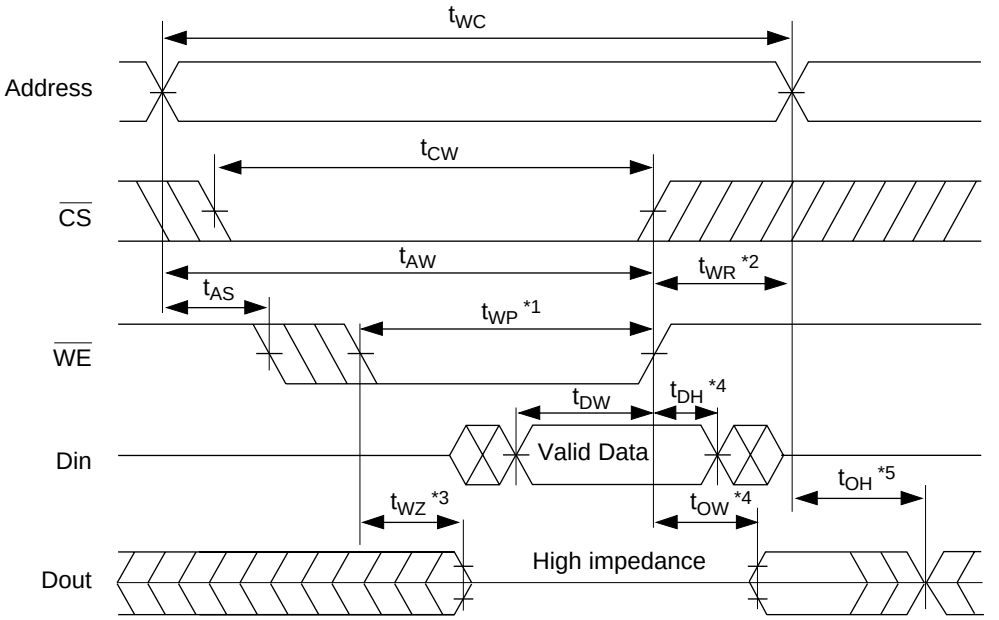
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

		HM6288-25		HM6288-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Date valid to end of write	t_{DW}	12	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}[*1]	0	8	0	10	ns
Output active from end of write	t_{OW}[*1]	5	—	5	—	ns

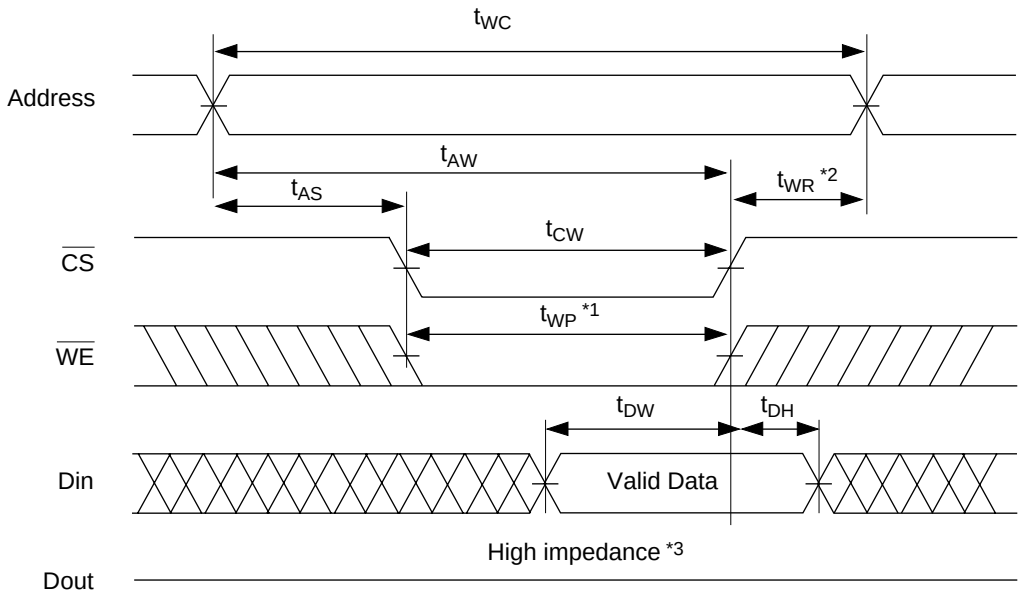
Note: 1. Transition is measured ±200 mV from steady state voltage with load (B).
These parameters are sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after t_{OW}. Then the data input signals of opposite phase to the outpus must not be applied to them.

Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

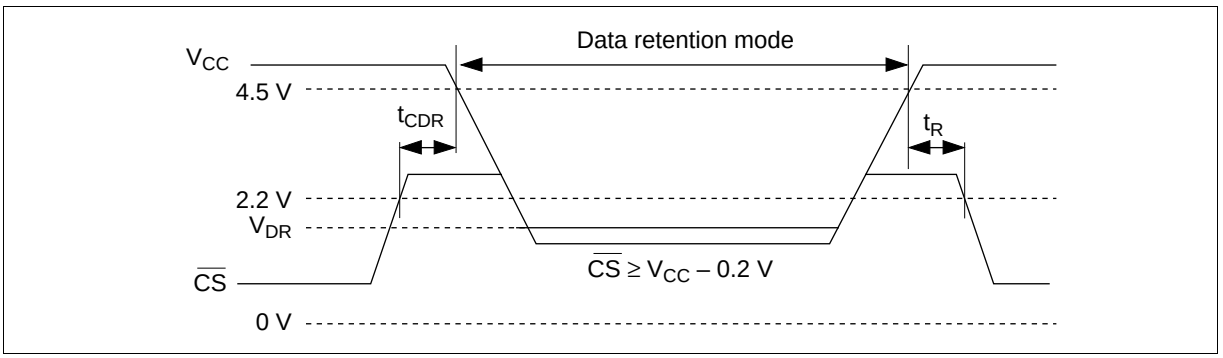
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Data retention characteristics are guaranteed only for L version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	—	50*2	µA	
		—	—	35*3	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC} *1	—	—	ns	

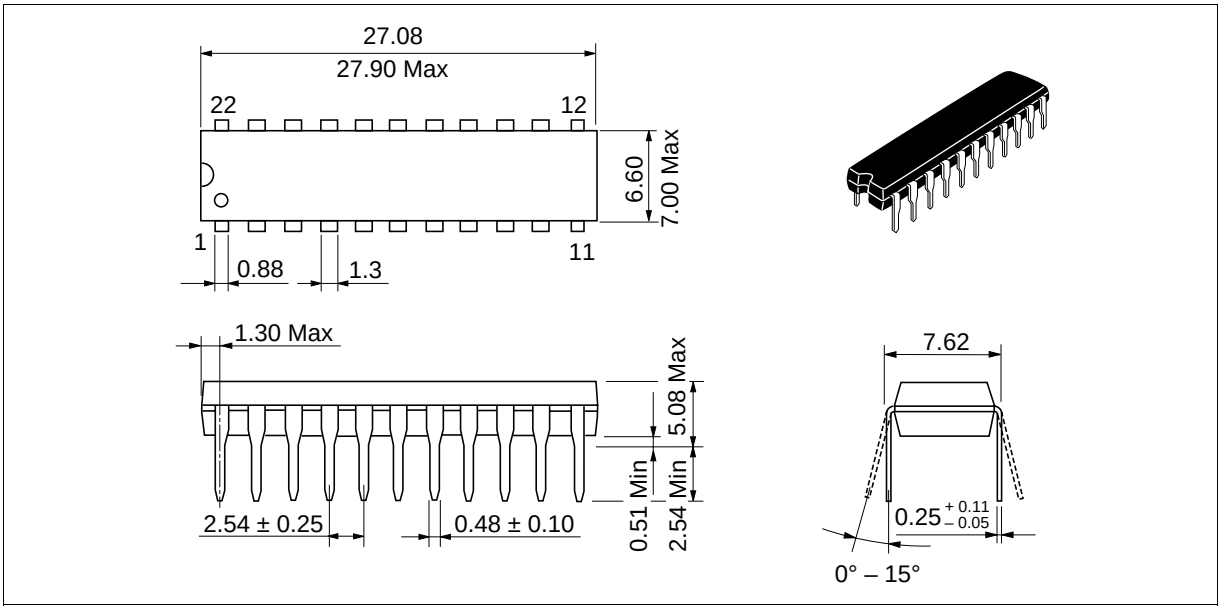
Notes: 1. t_{RC} = read cycle time
2. V_{CC} = 3.0 V
3. V_{CC} = 2.0 V

Low V_{CC} Data Retention Waveform



Package Dimensions

HM6288P/LP Series (DP-22NB) Unit: mm



HM6288JP/LJP Series (CP-24D) Unit: mm