



Low-Noise Synchronous PWM Step-Down DC/DC Converter

■ FEATURES

- 95% Efficiency or up
- 800mA Guaranteed Output Current.
- Adjustable Output Voltage from 0.75V to VIN of a range from +2.5V to 6.5V.
- Very Low Quiescent Current: 35 μ A (Typ.).
- Fixed- 500KHz or Adjustable Frequency Synchronous PWM Operation.
- Synchronizable external Switching Frequency up to 1MHz.
- Accurate Reference: 0.75V (\pm 2%).
- 100% Duty Cycle in Dropout.
- Low Profile 8-Pin MSOP Package.

■ APPLICATIONS

- PDAs.
- Digital Still Cameras.
- Handy-Terminals.
- Cellular Phones.
- CPU I/O Supplies.
- Cordless Phones.
- Notebook Chipset Supplies.
- Battery-Operated Devices (4 NiMH/ NiCd or 1 Li-ion Cells).

■ DESCRIPTION

The AIC1550 is a low-noise pulse-width-modulated (PWM) DC-DC step-down converter. It powers logic circuits in PDAs and small wireless systems such as cellular phones, handy-terminals.

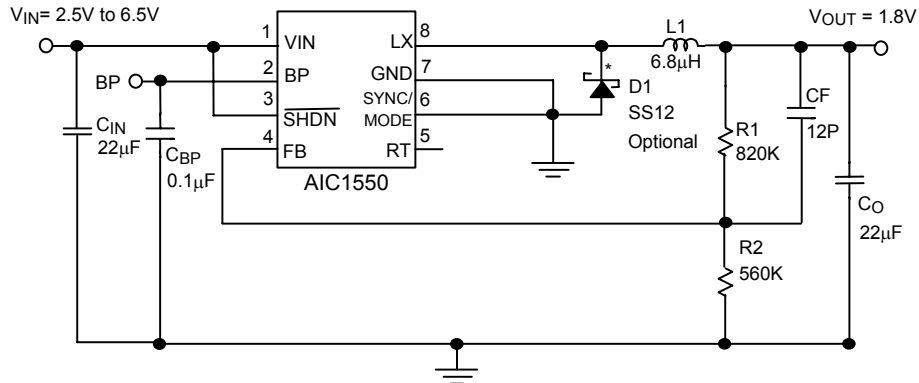
The device features an internal synchronous rectifier for high conversion efficiency. Excellent noise characteristics and fixed-frequency operation provide easy post-filtering. The AIC1550 is ideally suited for Li-ion battery applications. It is also suitable for +3V or +5V fixed input applications. The device can operate in either one of the following four modes.

- (1) **Forced PWM mode** operates at a fixed frequency regardless of the load.
- (2) **Synchronizable PWM mode** allows the synchronization by using an external switching frequency with a minimum harmonics.
- (3) **PWM/PFM Mode** extends battery life by switching to a PFM pulse-skipping mode under light loads.
- (4) **Shutdown mode** sets device to standby, reducing supply current to 0.1 μ A or under.

The AIC1550 can deliver over 800mA output current. The output voltage can be adjusted from 0.75V to VIN ranging from +2.5V to +6.5V. Other features of the AIC1550 include low quiescent current, low dropout voltage, and a 0.75V reference of \pm 2% accuracy. It is available in a space-saving 8-pin MSOP package.



TYPICAL APPLICATION CIRCUIT



C_{IN}: TAIYO YUDEN LMK316F226ZL-T Ceramic capacitor

C_{O1}: TAIYO YUDEN LMK316F226ZL-T Ceramic capacitor

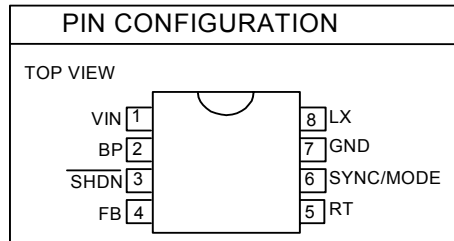
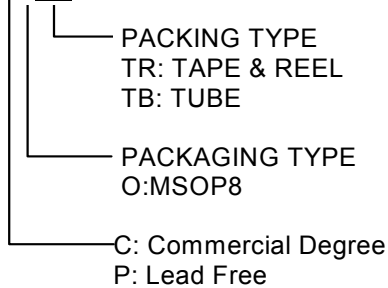
L1: TDK SLF6025-6R8M1R3

D1: GS SS12

* Note: Efficiency can boost 2% to 4% if D1 is connected.

ORDERING INFORMATION

AIC1550XXXX



Example: AIC1550COTR

→ In MSOP Package & Taping & Reel Packing Type

AIC1550POTR

→ In MSOP Lead Free Package & Taping & Reel Packing Type



■ **ABSOLUTE MAXIMUM RATINGS**

VIN, BP, SHDN, SYNC/MODE, RT to GND.....	-0.3 to +7V
BP to VIN.....	-0.3 to 0.3V
LX to GND.....	-0.3 ~ (VIN+0.3V)
FB to GND.....	-0.3 ~ (VBP+0.3V)
Operating Temperature Range.....	-40°C ~ 85°C
Junction Temperature	125°C
Storage Temperature Range.....	- 65°C ~ 150°C
Lead Temperature (Soldering, 10 sec).....	260°C

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

■ **TEST CIRCUIT**

Refer to Typical Application Circuit.



ELECTRICAL CHARACTERISTICS

($V_{IN}=+3.6V$, $T_A=+25^{\circ}C$, $SYNC/MODE = GND$, $\overline{SHDN} = IN$, unless otherwise specified.) (Note1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		2.5		6.5	V
Output Adjustment Range	V_{OUT}		V_{REF}		V_{IN}	V
Feedback Voltage	V_{FB}		0.735	0.75	0.765	V
Line Regulation		Duty Cycle = 100% to 23%		+1		%
Load Regulation		$I_{OUT} = 0$ to 800mA		-1.3		%
FB Input Current	I_{FB}	$V_{FB} = 1.4V$,	-50	0.01	50	nA
P-Channel On-Resistance	$P_{RDS(ON)}$	$I_{LX} = 100mA$	$V_{IN} = 3.6V$	0.32	0.65	Ω
			$V_{IN} = 2.5V$	0.38		
N-Channel On-Resistance	$N_{RDS(ON)}$	$I_{LX} = 100mA$	$V_{IN} = 3.6V$	0.32	0.65	Ω
			$V_{IN} = 2.5V$	0.38		
P-Channel Current-Limit Threshold		(Note 2)	1	1.5	2.1	A
Quiescent Current		$SYNC/MODE = GND$, $V_{FB} = 1.4V$, LX unconnected		35	70	μA
Shutdown Supply Current		$\overline{SHDN} = LX = GND$, includes LX leakage current		0.1	1	μA
LX Leakage Current		$V_{IN} = 5.5V$, $V_{LX} = 0$ or 5.5V	-20	0.1	20	μA
Oscillator Frequency	f_{OSC}		400	500	600	KHz
SYNC Capture Range			500		1000	KHz
Maximum Duty Cycle	$duty_{MAX}$		100			%
Undervoltage Lockout Threshold	UVLO	V_{IN} rising, typical hysteresis is 85mV	1.9	2.0	2.1	V
Logic Input High	V_{IH}	\overline{SHDN} , $SYNC/MODE$, LIM	2			V
Logic Input Low	V_{IL}	\overline{SHDN} , $SYNC/MODE$, LIM			0.4	V
Logic Input Current		\overline{SHDN} , $SYNC/MODE$, LIM	-1	0.1	1	μA
SYNC/MODE Minimum Pulse Width		High or low	500			nS

Note 1: Specifications are production tested at $T_A=25^{\circ}C$. Specifications over the $-40^{\circ}C$ to $85^{\circ}C$ operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: Maximum specification is guaranteed by design, not production tested.



TYPICAL PERFORMANCE CHARACTERISTICS

($T_A=25^\circ\text{C}$, $V_{IN}=3.6\text{V}$, SYNC/MODE=GND, with Schottky diode D1, unless otherwise noted.)

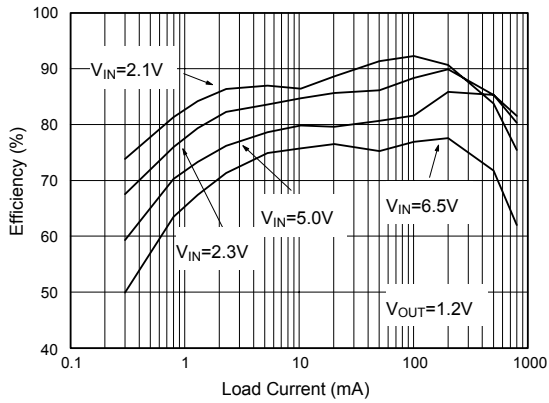


Fig. 1 Load Current vs. Efficiency ($V_{OUT}=1.2\text{V}$)
(Refer to typical application circuit)

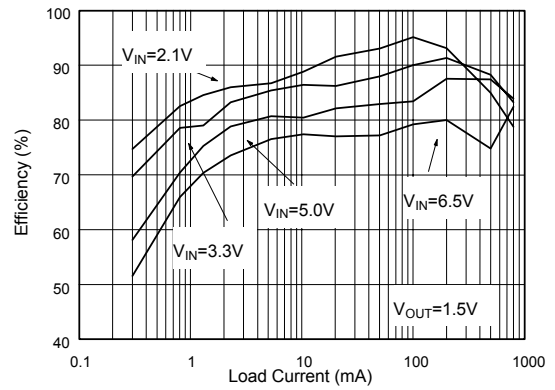


Fig. 2 Load Current vs. Efficiency ($V_{OUT}=1.5\text{V}$)
(Refer to typical application circuit)

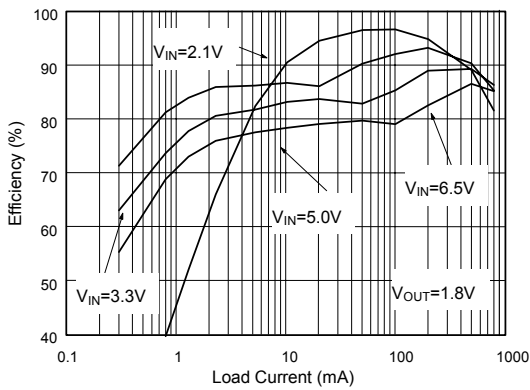


Fig. 3 Load Current vs. Efficiency ($V_{OUT}=1.8\text{V}$)
(Refer to typical application circuit)

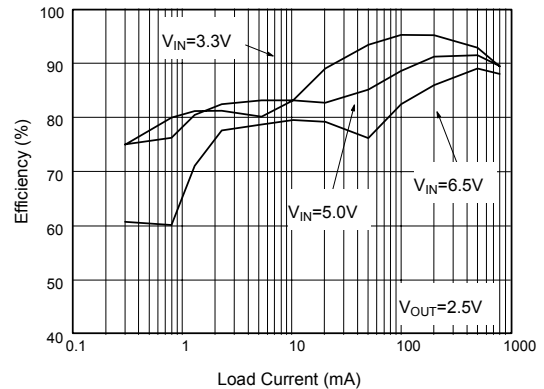


Fig. 4 Load Current vs. Efficiency ($V_{OUT}=2.5\text{V}$)
(Refer to typical application circuit)

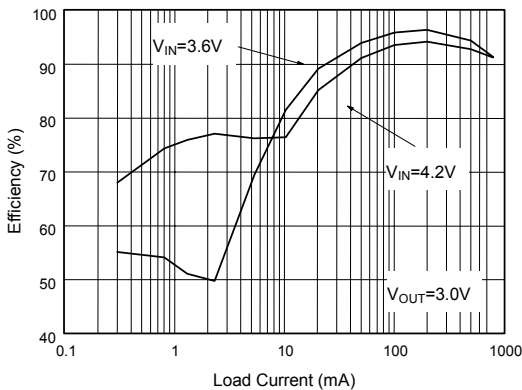


Fig. 5 Load Current vs. Efficiency ($V_{OUT}=3.0\text{V}$)
(Refer to typical application circuit)

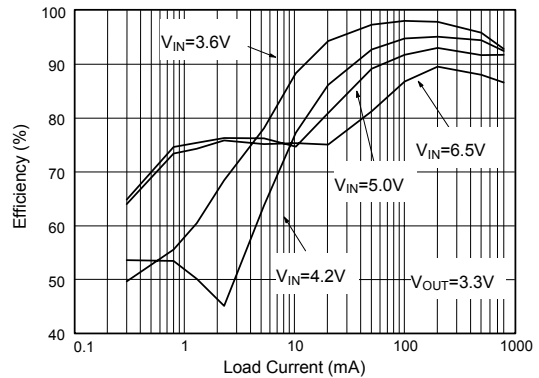


Fig. 6 Load Current vs. Efficiency ($V_{OUT}=3.3\text{V}$)
(Refer to typical application circuit)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

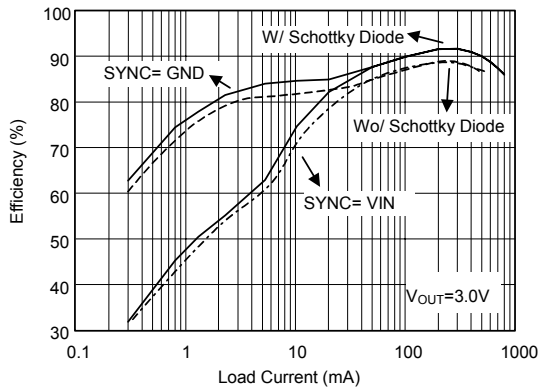


Fig. 7 Load Current vs. Efficiency (W/ or W/O Schottky Diode)

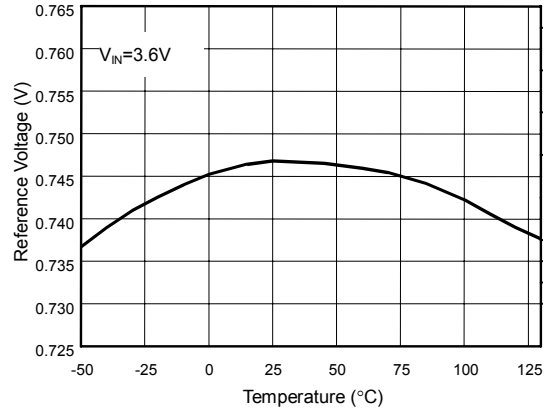


Fig. 8 Reference Voltage vs. Temperature

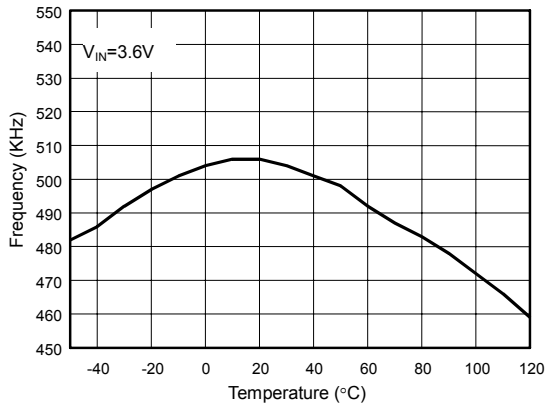


Fig. 9 Oscillator Frequency vs. Temperature

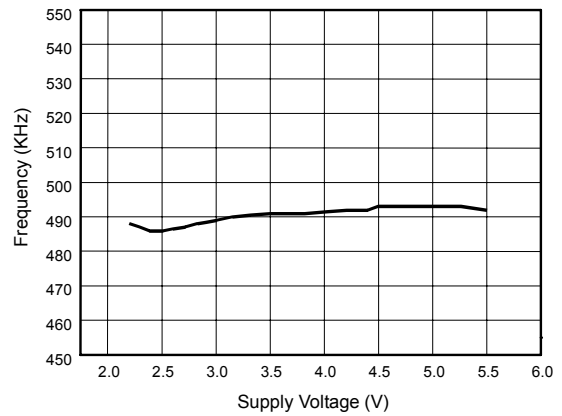


Fig. 10 Frequency vs. Input Voltage

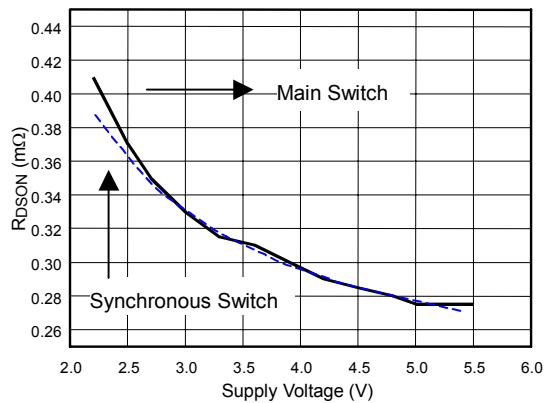


Fig. 11 $R_{DS(ON)}$ vs. Supply Voltage

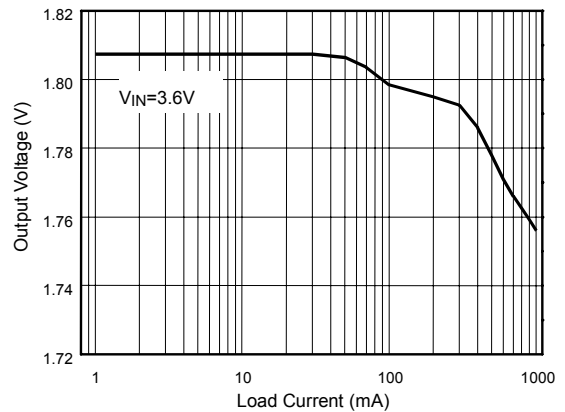


Fig. 12 Output Voltage vs. Load Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

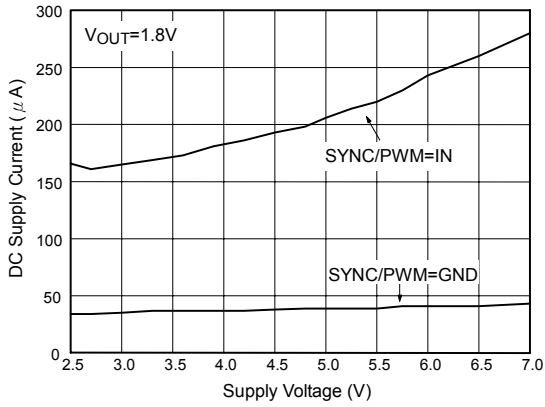


Fig. 13 DC Supply Current vs. Supply Voltage

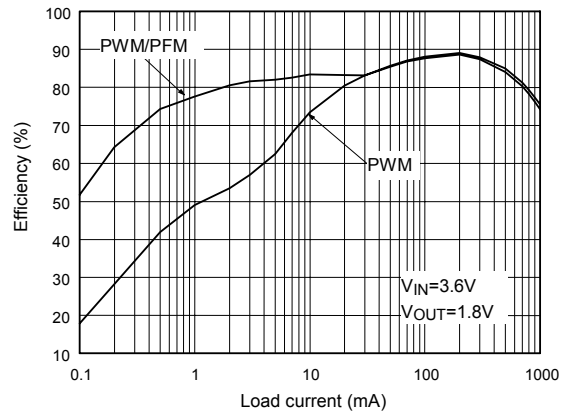


Fig. 14 Efficiency vs. Load current

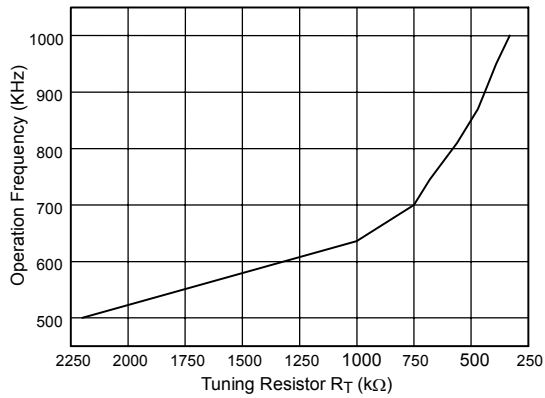


Fig. 15 Operation Frequency vs. Tuning Resistor

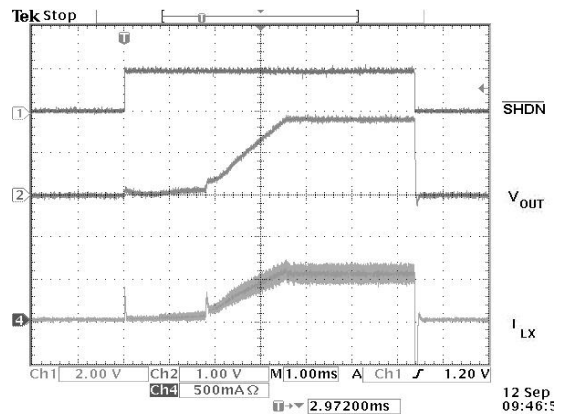


Fig. 16 Start-up from Shutdown, R_{LOAD}=3Ω

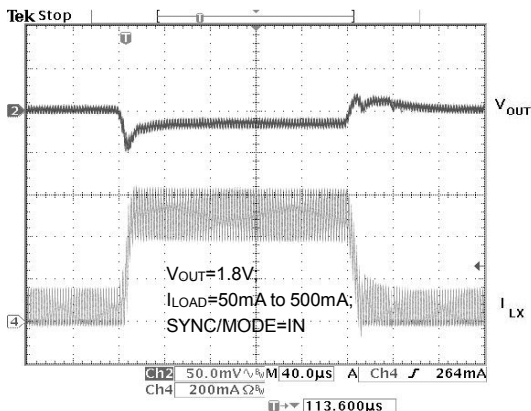


Fig. 17 Load Transient Response

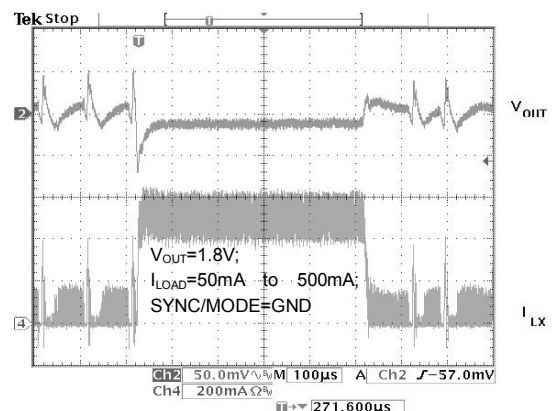


Fig. 18 Load Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

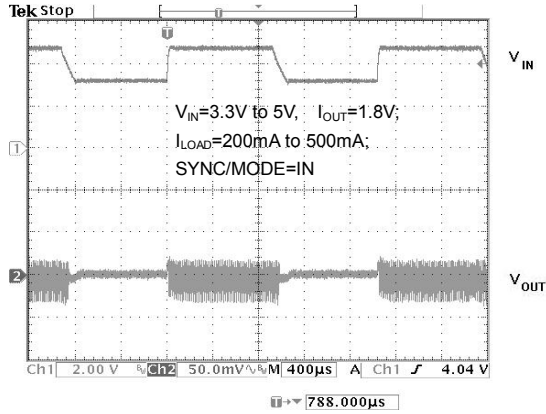


Fig. 19 Line Transient Response

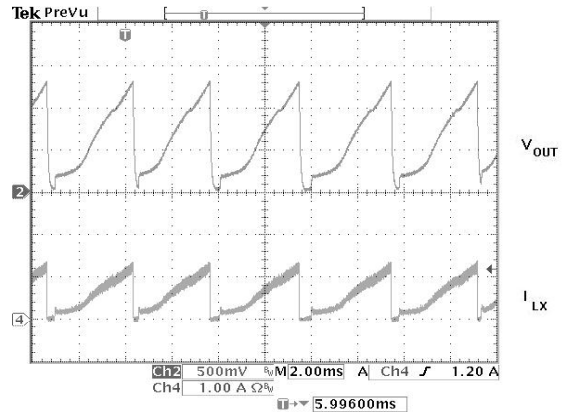


Fig. 20 Short Circuits Protection

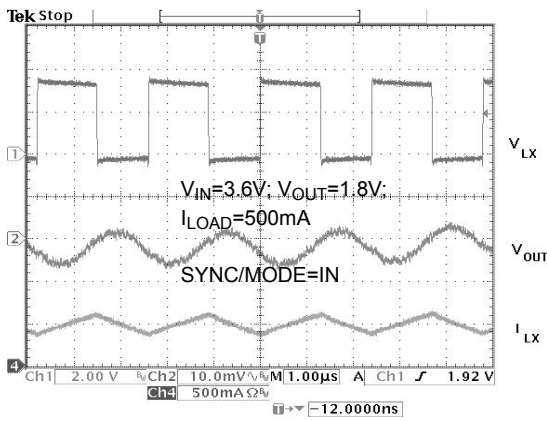


Fig. 21 Switching Waveform

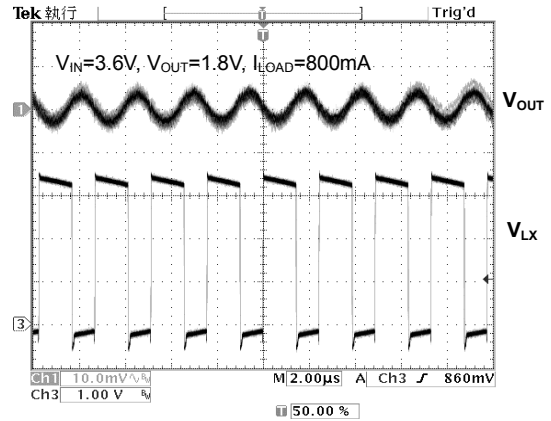
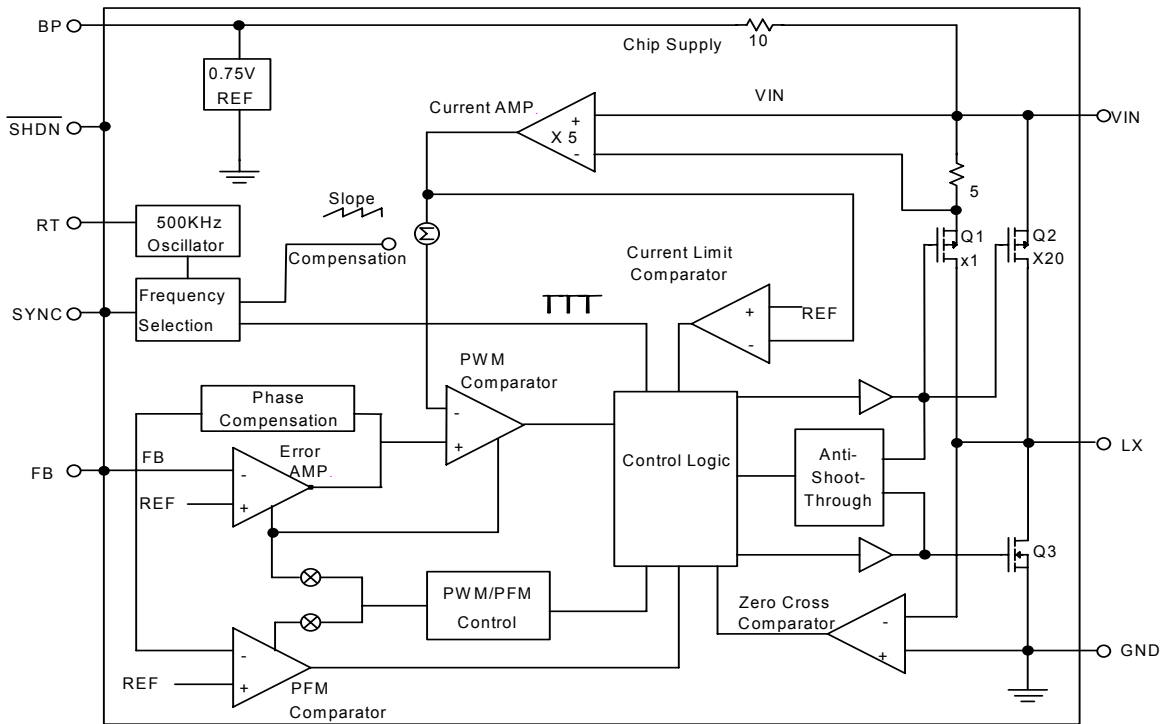


Fig. 22 Output Ripple voltage



■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

- PIN 1: VIN- Supply Voltage Input ranging from +2.5V to +6.5V. Bypass with a 22 μ F capacitor.
- PIN 2: BP- Supply Bypass Pin internally connecting to VIN. Bypass with a 0.1 μ F capacitor.
- PIN 3: $\overline{\text{SHDN}}$ - Active-Low, Shutdown-Control Input reducing supply current to 0.1 μ A in shutdown mode.
- PIN 4: FB- Feedback Input.
- PIN 5: RT- Frequency Adjustable Pin connecting to GND through a resistor to increase frequency. (Refer to Fig. 15)

- PIN 6: SYNC/MODE- Oscillator Sync and Low-Noise, Mode-Control Input.
 SYNC/MODE = VIN (Forced PWM Mode)
 SYNC/MODE = GND (PWM/PFM Mode)
 An external clock signal connecting to this pin allows LX switching synchronization.
- PIN 7: GND- Ground.
- PIN 8: LX- Inductor connecting to the Drains of the Internal Power MOSFETs



■ APPLICATION INFORMATIONS

Introduction

AIC1550 is a low-noise, pulse-width-modulated (PWM), DC-DC step-down converter. It features an internal synchronous rectifier, which eliminates external Schottky diode. AIC1550 is suitable for Li-Ion battery applications, or can be used at 3V or 5V fixed input voltage. It operates in one of following four modes.

- (1) **Forced PWM mode** operates at a fixed frequency regardless of the load.
- (2) **Synchronizable PWM mode** allows the synchronization by using an external switching frequency with a minimum harmonics.
- (3) **PWM/PFM Mode** extends battery life by switching to a PFM pulse-skipping mode under light loads.
- (4) **Shutdown mode** sets device to standby, reducing supply current to 0.1 μ A or under.

Continuous output current of AIC1550 can be upward to 800mA and output voltage can be adjusted from 0.75V to V_{IN} with an input range from 2.5V to 6.5V by a voltage divider. AIC1550 also features high efficiency, low dropout voltage, and a 0.75V reference with $\pm 2\%$ accuracy. It is available in a space-saving 8-pin MSOP package.

Operation

When power on, control logic block detects SYNC/MODE pin connecting to V_{IN} or GND to determine operation function and gives a signal to PWM/PFM control block to determine the proper comparator (ref. Block Diagram). AIC1550 works with an internal synchronous rectifier – Q3, to

increase efficiency. When control logic block turns Q2 on, Q3 will turn off through anti-short-through block. Similarly, when Q3 is on, Q2 will turn off.

AIC1550 provides current limit function by using a 5 Ω resistor. When Q1 turns on, current follows through the 5 Ω resistor. And current amplifier senses the voltage, which crosses the resistor, and amplifies it. When the sensed voltage gets bigger than reference voltage, control logic shuts the device off.

PWM/PFM Function

When connecting SYNC/MODE pin to V_{IN} , the device is forced into PWM (Pulse-Width-Modulated) mode with constant frequency. Advantage of constant frequency is easily reducing noise without complex post-filter. But its disadvantage is low efficiency at light loading. Therefore, AIC1550 provides a function to solve this problem. When connecting SYNC/MODE pin to GND, device is able to get into PWM/PFM (Pulse-Frequency-Modulated) modes. Under a light loading condition, the device turns to PFM mode, which results in a higher efficiency. PWM mode is on when heavy loading applies and the noise is reduced.

Frequency Synchronization

Connecting an external clock signal to SYNC/MODE pin can control switching frequency. The acceptable range is from 500kHz to 1MHz. This mode exhibits low output ripple as well as low audio noise and reduces RF interference while providing reasonable low current efficiency.



100% Duty Cycle Operation

When the input voltage approaches the output voltage, the converter continuously turns Q2 on. In this mode, the output voltage is equal to the input voltage minus the voltage, which is the drop across Q2.

If input voltage is very close to output voltage, the switching mode goes from pure PWM mode to 100% duty cycle operation. During this transient state mentioned above, large output ripple voltage will appear on output terminal.

Components Selection

Inductor

The inductor selection depends on the operating frequency of AIC1550. The internal switching frequency is 500KHz, and the external synchronized frequency ranges from 500KHz to 1MHz. A higher frequency allows the uses of smaller inductor and capacitor values. But, higher frequency results lower efficiency due to the internal switching loss.

The ripple current ΔI_L interrelates with the inductor value. A lower inductor value gets a higher ripple current. Besides, a higher V_{IN} or V_{OUT} can also get the same result. The inductor value can be calculated as the following formula.

$$L = \frac{1}{(f)(\Delta I_L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (1)$$

Users can define the acceptable ΔI_L to gain a suitable inductor value.

Since AIC1550 can be used in ceramic capacitor application, the component selection will be different from the one for the application above. AIC1550 has a built-in slope compensation, which activates when duty cycle is larger than 0.45. The slope Ma , $0.27V/\mu s$, has to be larger than half of $M2$. $M2$ is equal to output voltage divided by $L1$. The formula of inductor is shown as below:

$$L1 > \frac{V_{OUT}}{2 \times Ma} = \frac{V_{OUT}}{2 \times 0.27} \quad (2)$$

Note that output voltage can be defined according to user's requirement to get a suitable inductor value.

Output Capacitor

The selection of output capacitor depends on the suitable ripple voltage. Lower ripple voltage corresponds to lower ESR (Equivalent Series Resistor) of output capacitor. Typically, once the ESR is satisfied with the ripple voltage, the value of capacitor is adequate for filtering. The formula of ripple voltage is as below:

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right) \quad (3)$$

Besides, in buck converter architecture frequency stands at $1/\sqrt{LC}$ when a double pole formed by the inductor and output capacitor occurs. This will reduce phase margin of circuit so that the stability gets weakened. Therefore, a feedforward capacitor that is parallel with $R1$ can be added to reduce output ripple voltage and increase circuit stability. The output capacitor can be calculated as the following formula.

$$\frac{1}{\sqrt{L1 \times C_O}} \cong \frac{1}{R1 \times CF} \quad (4)$$

For more reduction in the ripple voltage, a 12pF ceramic capacitor, which is parallel with output capacitor, is used.

External Schottky Diode

AIC1550 has an internal synchronous rectifier, instead of Schottky diode in buck converter. However, a blank time, which is an interval when both of main switch, Q2, and synchronous rectifier, Q3, are off; occurs at each switching cycle. At the moment, AIC1550 has a decreasing efficiency. Therefore, an external Schottky diode is needed to reinforce the efficiency.



Since the diode conducts during the off time, the peak current and voltage of converter is not allowed to exceed the diode ratings. The ratings of diode can be calculated by the following formulas:

$$V_{D,MAX(OFF)} = V_{IN} \quad (5)$$

$$I_{D,MAX(ON)} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (6)$$

$$\begin{aligned} I_{D,AVG(ON)} &= I_{OUT} - I_{IN} = I_{OUT} - D \times I_{OUT} \\ &= (1-D) \times I_{OUT} \end{aligned} \quad (7)$$

Adjustable Output Voltage

AIC1550 appears a 0.75V reference voltage at FB pin. Output voltage, ranging from 0.75V to V_{IN} , can be set by connecting two external resistors, R1 and R2. V_{OUT} can be calculated as:

$$V_{OUT} = 0.75V \times \left(1 + \frac{R1}{R2}\right) \quad (8)$$

Applying a 12pF capacitor parallel with R1 can prevent stray pickup. They should sit as close to AIC1550 as possible. But load transient response is degraded by this capacitor.

Layout Consideration

To ensure a proper operation of AIC1550, the following points should be given attention to:

1. Input capacitor and V_{in} should be placed as close as possible to each other to reduce the input ripple voltage.
2. The output loop, which is consisted of inductor, Schottky diode and output capacitor, should be kept as small as possible.
3. The routes with large current should be kept short and wide.
4. Logically the large current on the converter, when AIC1550 is on or off, should flow at the same direction.

5. The FB pin should connect to feedback resistors directly. And the route should be away from the noise source, such as inductor of LX line.
6. Grounding all components at the same point may effectively reduce the occurrence of loop. A stability ground plane is very important for gaining higher efficiency. When a ground plane is cut apart, it may cause disturbed signal and noise. If possible, two or three through-holes can ensure the stability of grounding. Fig.24 to 27 show the layout diagrams of AIC1550.

Example

Here are two examples to prove the components selector guide above.

1. Tantalum capacitors application:

Assume AIC1550 is used for mobile phone application, which uses 1-cell Li-ion battery with 2.7V to 4.2V input voltage for power source. The required load current is 800mA, and the output voltage is 1.8V. Substituting $V_{OUT}=1.8V$, $V_{IN}=4.2V$, $\Delta I=250mA$, and $f=500KHz$ to equation (1)

$$L = \frac{1.8V}{500KHz \times 250mA} \left(1 - \frac{1.8V}{4.2V}\right) = 8.23\mu H$$

Therefore, 10 μH is proper for the inductor. And the inductor of series number SLF6025-100M1R0 from TDK with 57.3m Ω series resistor is recommended for the best efficiency.

For output capacitor, the ESR is more important than its capacity. Assuming ripple voltage $\Delta V=100mV$, then the ESR can be calculated as:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{100mV}{250mA} = 0.4\Omega$$

Therefore, a 33 $\mu H/10V$ capacitor, MCM series from NIPPON, is recommend.

Schottky selection is calculated as following.

$$V_{D,MAX(OFF)} = V_{IN} = 4.2V$$



$$\begin{aligned}
 I_{D,MAX(ON)} &= I_{OUT,MAX} + \frac{\Delta I_L}{2} \\
 &= 800\text{mA} + \frac{250\text{mA}}{2} \\
 &= 925\text{mA}
 \end{aligned}$$

$$\begin{aligned}
 I_{D,avg(ON)} &= (1-D) \times I_{OUT} \\
 &= \left(1 - \frac{1.8}{4.2}\right) \times 800\text{mA} \\
 &= 457.14\text{mA}
 \end{aligned}$$

According to the data above, the Schottky diode, SS12, from GS is recommended.

For feedback resistors, choose R2=390kΩ and R1 can be calculated as follows:

$$R1 = \left(\frac{1.8\text{V}}{0.75} - 1\right) \times 390\text{k}\Omega = 546\text{k}\Omega; \text{ use } 560\text{k}\Omega$$

Fig. 22 shows the application circuit of AIC1550, and Fig. 23 to 26 show the layout diagrams of it.

2. Ceramic capacitors application:

Of the same AIC1550 application above, except for ceramic capacitor used, Co, R1, and R2 can be calculated as following formulas. And the same values of load current and output voltage at 800mA and 1.8V respectively are used.

V_{OUT} is substituted by 1.8V in equation (2) as

$$L1 > \frac{V_{OUT}}{0.54} = \frac{1.8}{0.54} = 3.33\mu\text{H}$$

Let L1 = 6.8μH, and choose CF = 12pF, R1 = 820kΩ.

Co calculated by the following formula can improve circuit stability.

$$\frac{1}{\sqrt{L1 \times C_O}} \cong \frac{1}{R1 \times CF}$$

Therefore,

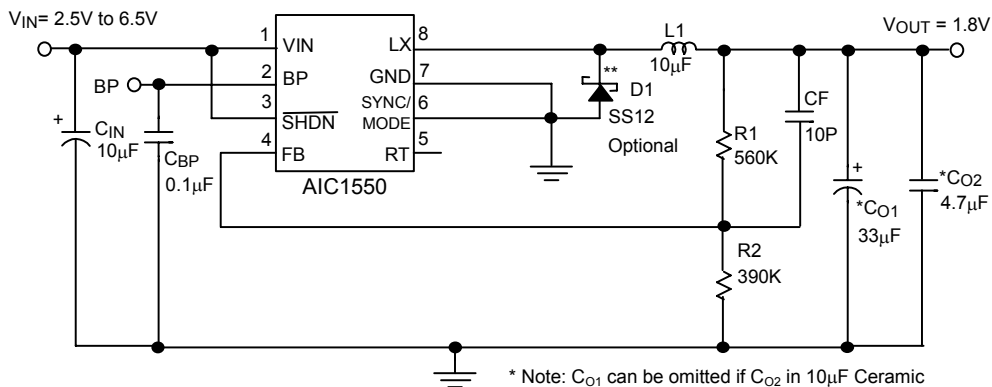
$$C_O = \frac{(R1 \times CF)^2}{L1} = \frac{(820\text{k} \times 12\text{pF})^2}{6.8\mu} = 12\mu\text{F}$$

Say, Co is 22μF. Then, R2 can be decided by equation (8) as

$$\frac{R1}{R2} = \frac{V_{OUT}}{V_{ref}} - 1 = \frac{1.8}{0.75} - 1 = 1.4$$

So, R2 = 560kΩ.

Note: Schottky diode, SS12 from GS, is still required in this application.



C_{IN}: NIPPON 10μF/6V Tantalum capacitor
 C_{O1}: NIPPON 33μF/6V Tantalum capacitor
 L: TDK SLF6025-100M1R0
 D1: GS SS12

* Note: C_{O1} can be omitted if C_{O2} is 10μF Ceramic
 ** Note: Efficiency can boost 2% to 4% if D1 is connected.



Fig. 23 AIC1550 Application Circuit (Tantalum capacitor application)

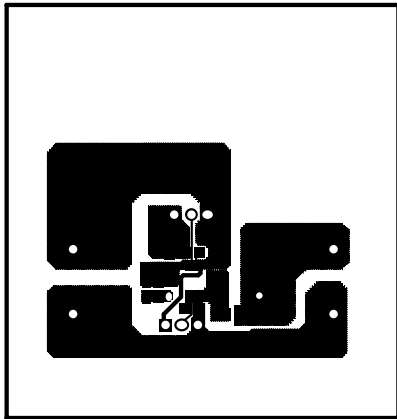


Fig. 24 Top Layer

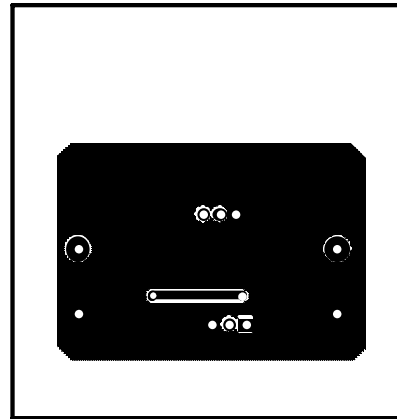


Fig. 25 Bottom Layer

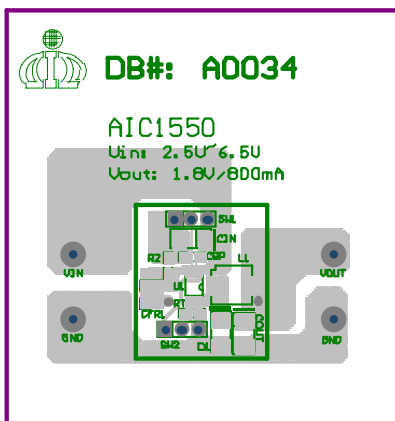


Fig. 26 Top Over Layer

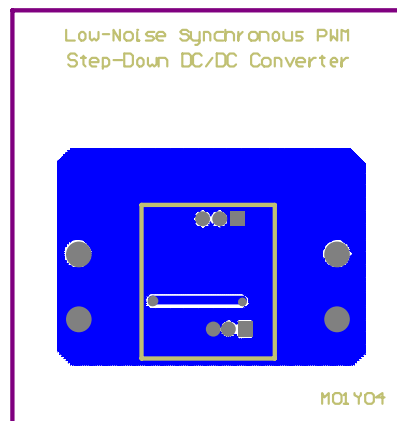
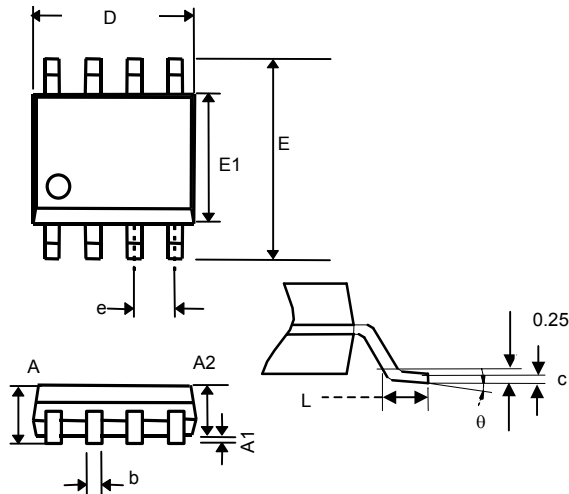


Fig. 27 Bottom Over Layer



■ PHYSICAL DIMENSIONS

● MSOP 8 (CO) (PO) (unit: mm)



SYMBOL	MIN	MAX
A	-	1.10
A1	0.05	0.15
A2	0.75	0.95
b	0.25	0.40
c	0.13	0.23
D	2.90	3.10
E	4.90 BSC	
E1	2.90	3.10
e	0.65 BSC	
L	0.40	0.70
θ	0°	6°

Note:

Information provided by AIC is believed to be accurate and reliable. However, we cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in an AIC product; nor for any infringement of patents or other rights of third parties that may result from its use. We reserve the right to change the circuitry and specifications without notice.

Life Support Policy: AIC does not authorize any AIC product for use in life support devices and/or systems. Life support devices or systems are devices or systems which, (i) are intended for surgical implant into the body or (ii) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.