



No.4871

2SK2171

N-Channel Junction Silicon FET

High-Frequency, Low-Frequency Amp
Analog Switch Applications

Features

- Adoption of FBET process.
- Large $|Y_{fs}|$.
- Small Ciss.
- High P_D allowable power dissipation.

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

			unit
Drain-to-Source Voltage	V_{DSX}	40	V
Gate-to-Drain Voltage	V_{GDS}	-40	V
Gate Current	I_G	10	mA
Drain Current	I_D	100	mA
Allowable Power Dissipation	P_D	400	mW
		Mounted on ceramic board (250mm ² × 0.8mm)	800
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Electrical Characteristics at $T_a = 25^\circ\text{C}$

		min	typ	max	unit
G-D Breakdown Voltage	$V_{(BR)GDS}$ $I_G = -10\mu\text{A}, V_{DS} = 0$	-40			V
Gate-to-Source Leakage Current	I_{GSS} $V_{GS} = -20\text{V}, V_{DS} = 0$			-1.0	nA
Cutoff Voltage	$V_{GS(off)}$ $V_{DS} = 10\text{V}, I_D = 100\mu\text{A}$	-2.0	-3.0	-5.0	V
Drain Current	I_{DSS}^* $V_{DS} = 10\text{V}, V_{GS} = 0$	40*		75*	mA
Forward Transfer Admittance	$ Y_{fs} $ (1) $V_{DS} = 10\text{V}, I_D = 10\text{mA}, f = 1\text{kHz}$	10	15		mS
		$ Y_{fs} $ (2) $V_{DS} = 10\text{V}, V_{GS} = 0, f = 1\text{kHz}$	22	30	
Input Capacitance	Ciss $V_{DS} = 10\text{V}, V_{GS} = 0, f = 1\text{MHz}$		11		pF
Reverse Transfer Capacitance	Crss $V_{DS} = 10\text{V}, V_{GS} = 0, f = 1\text{MHz}$		2.5		pF
Noise Figure	NF $V_{DS} = 10\text{V}, R_g = 1\text{k}\Omega, I_D = 1\text{mA}, f = 1\text{kHz}$		1.5		dB
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$ $V_{DS} = 10\text{mV}, V_{GS} = 0$		30		Ω

*Pulse Test Pulse Width $\leq 2\text{mS}$

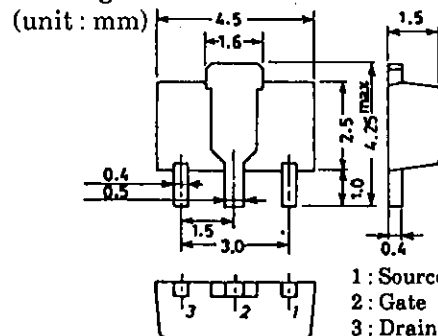
※ : The 2SK2171 is classified by I_{DSS} as follows : (unit : mA)

40	3	52	48	4	63	57	5	75
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Marking : KM

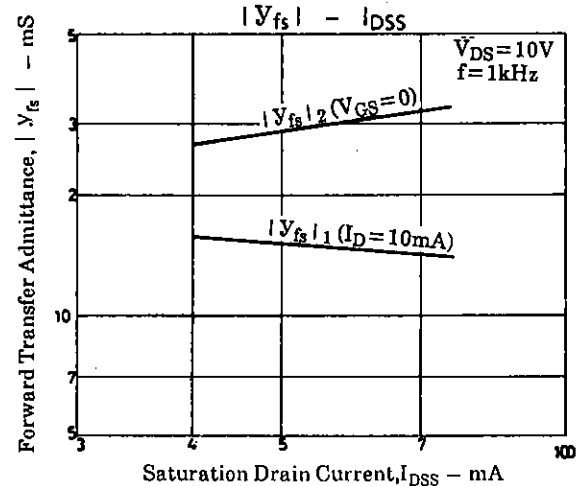
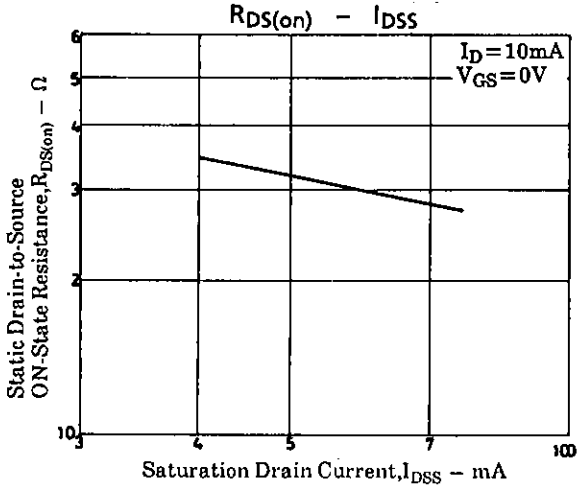
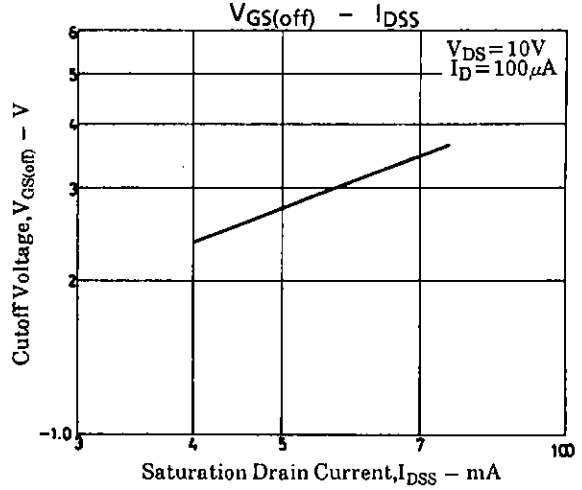
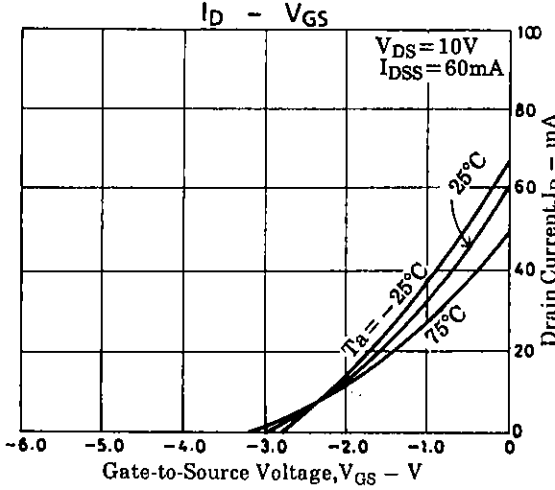
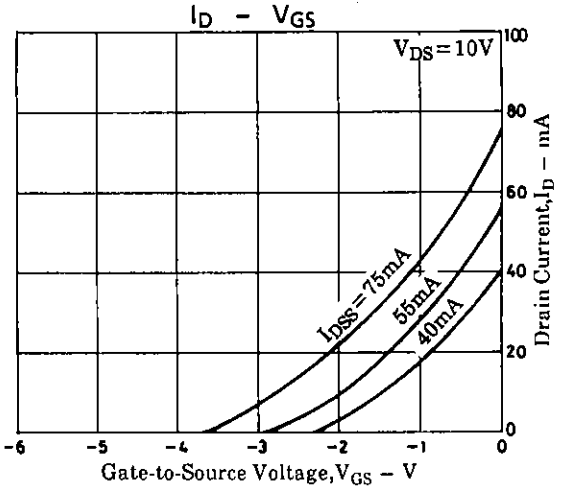
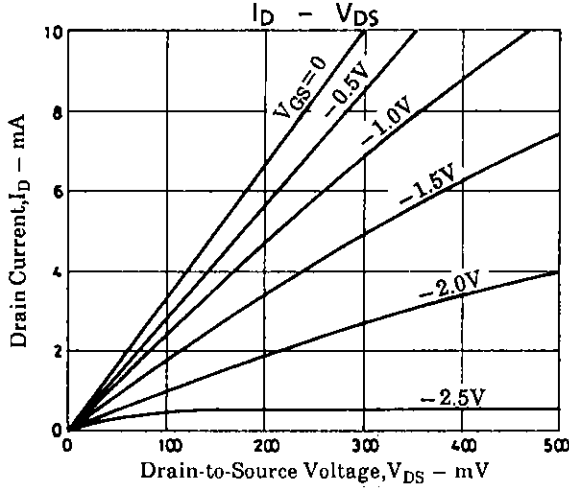
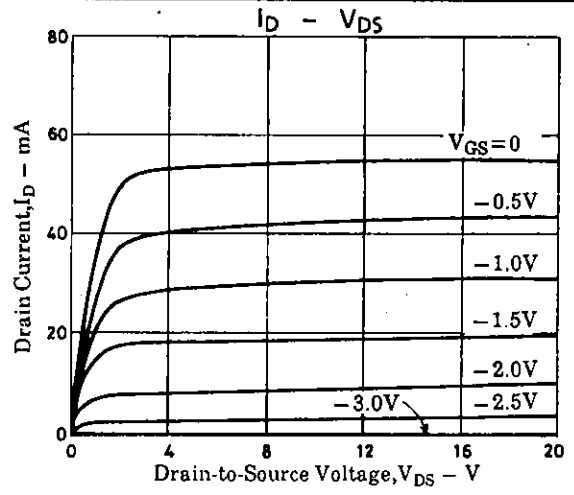
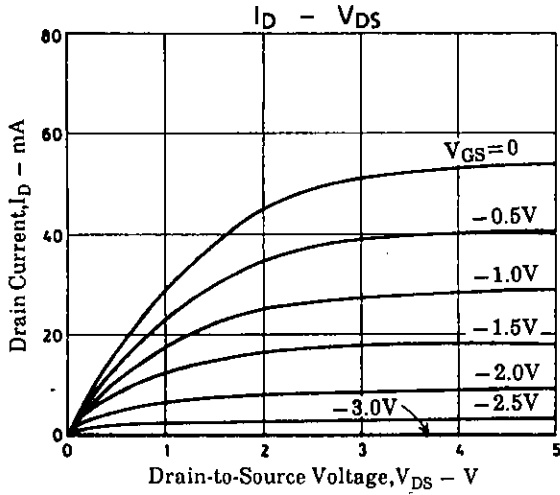
I_{DSS} rank : 3, 4, 5

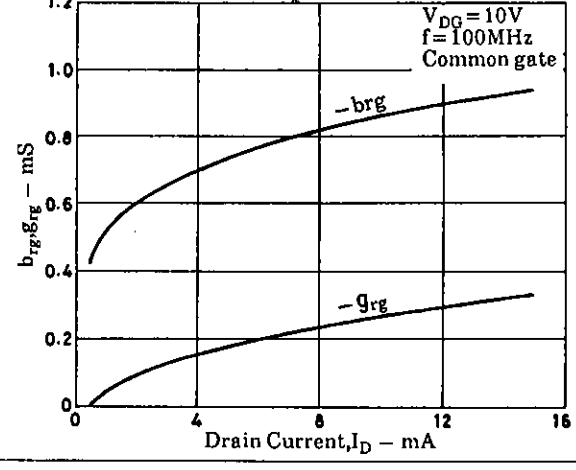
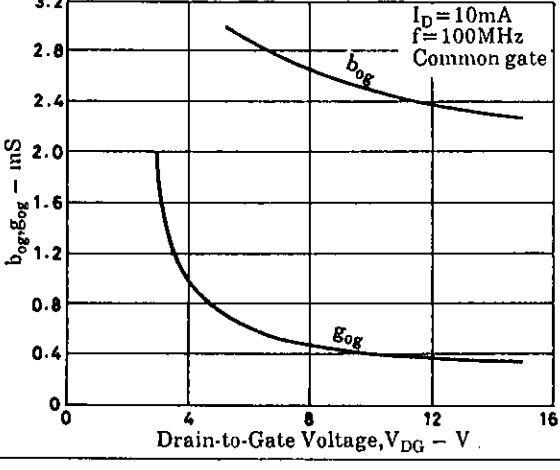
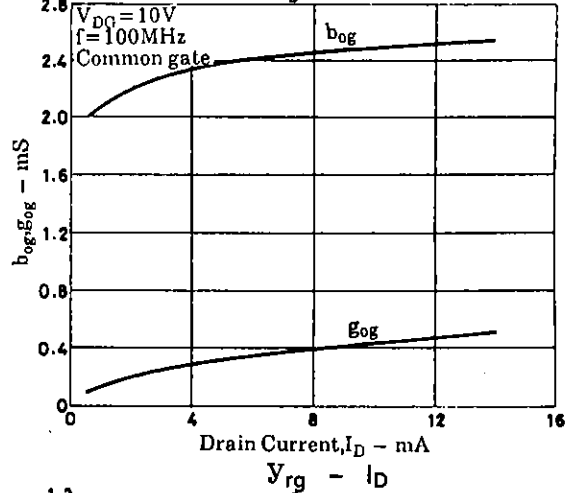
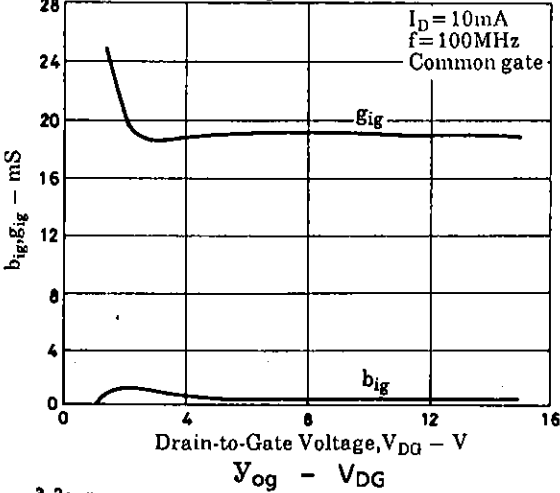
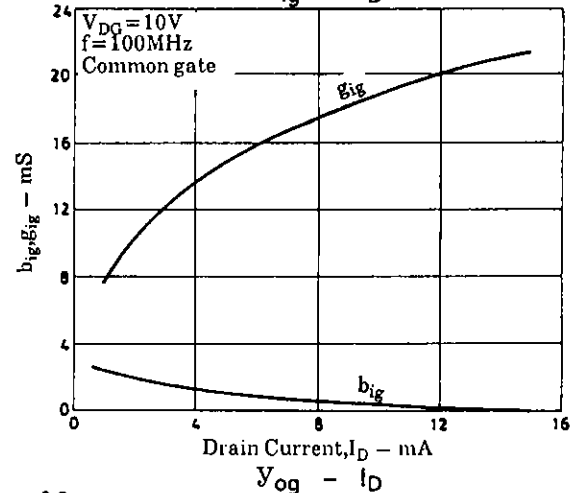
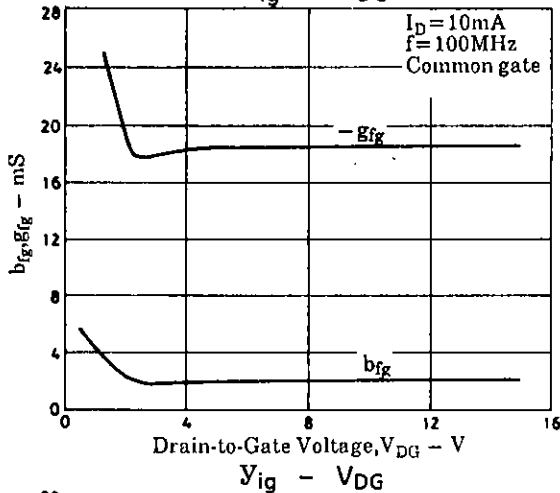
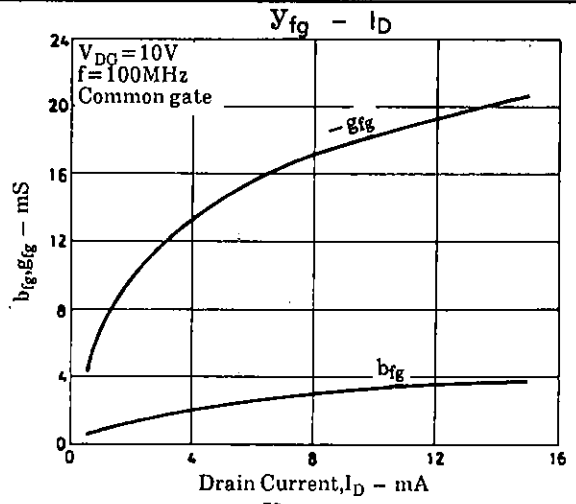
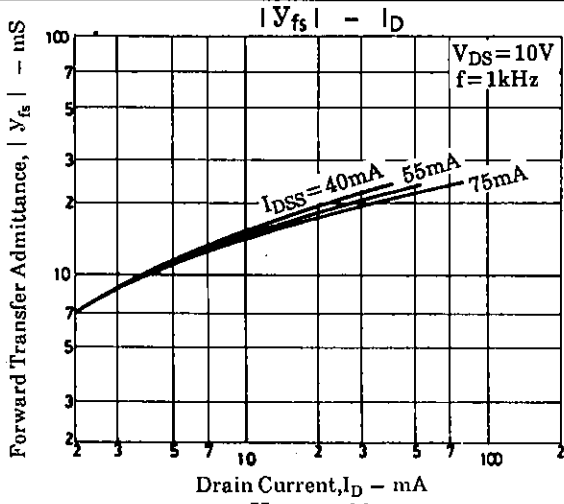
Package Dimensions 2125

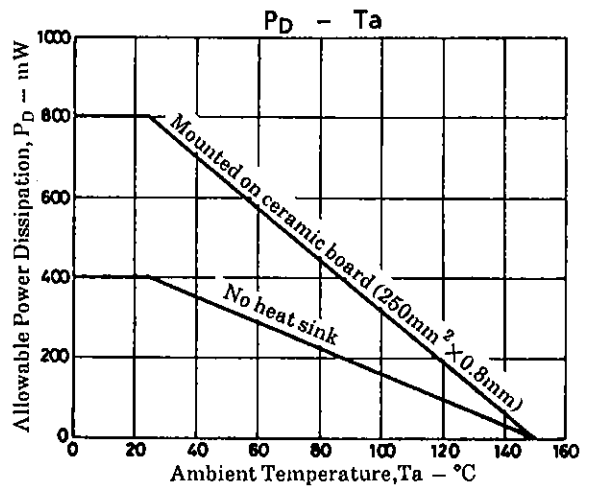
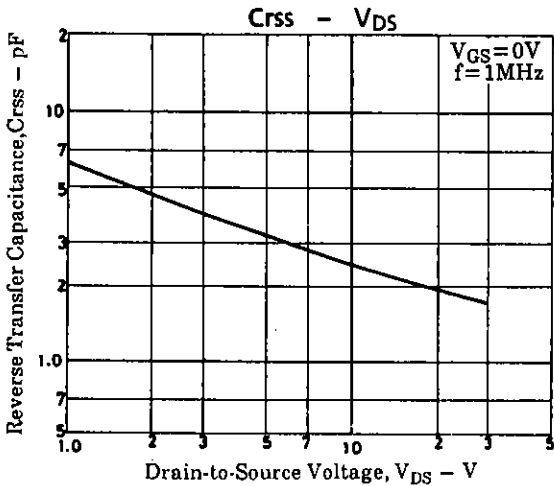
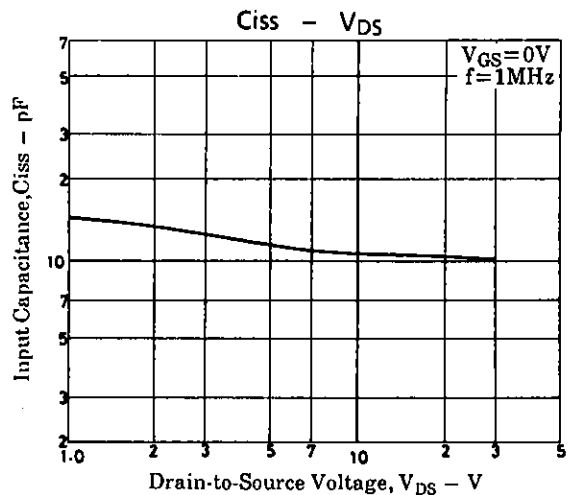
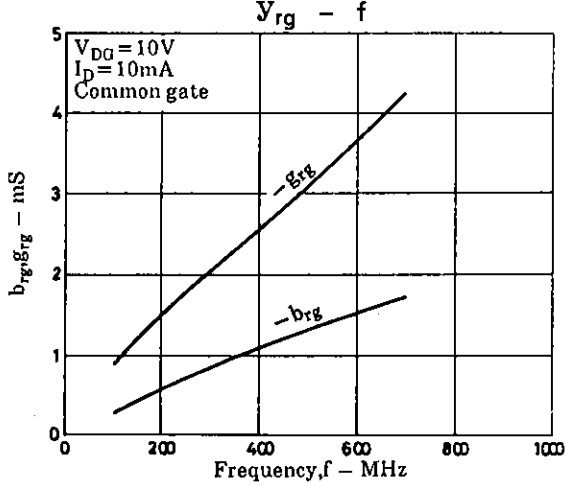
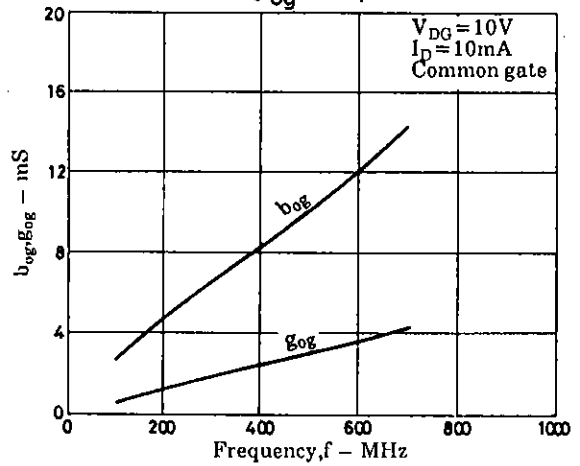
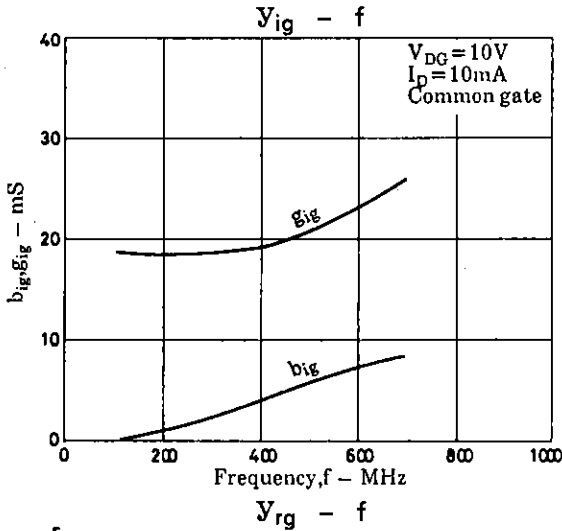
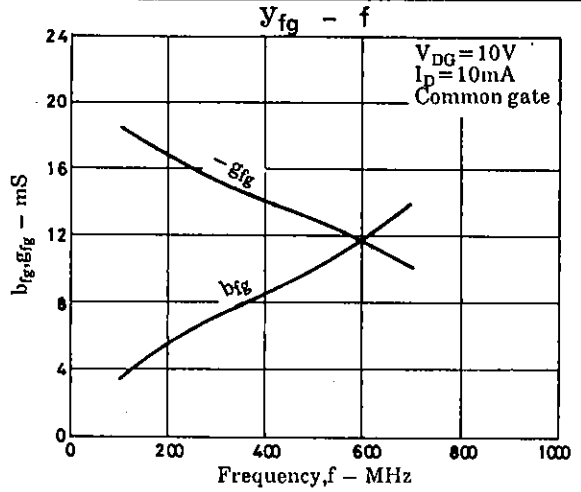
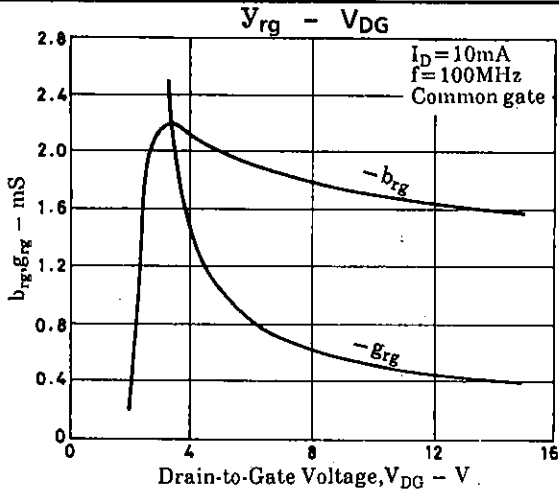


- 1 : Source
- 2 : Gate
- 3 : Drain

SANYO : PCP
(Bottom View)







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