

# TEA5880TS

Integrated FM stereo radio IC for host processor tuning in handheld applications

Rev. 02 — 26 April 2004

Preliminary data sheet

## 1. General description

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The TEA5880TS stereo FM radio IC dramatically reduces the printed-circuit board area (only 100 mm<sup>2</sup>) needed to integrate FM radio functionality into portable devices. This makes it invaluable for any application where space is at a premium.

Relying on a system host processor for radio tuning, the TEA5880TS is ideally suited for powerful devices such as PDAs, notebooks, portable CD and MP3 players.

## 2. Features

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- No alignments necessary
- Complete adjustment-free stereo decoder; no external crystal required
- Fully integrated MPX VCO circuit
- Fully integrated low IF selectivity and demodulation
- The full integration level means no or few external components required
- No external FM discriminator needed due to full integration
- Built-in adjacent channel interference total reduction (no 114 kHz, no 190 kHz)
- The level of the incoming signal at which the radio must lock is software programmable
- Due to new tuning concept, the tuning is independent of the channel spacing
- Very high sensitivity due to integrated low noise RF input amplifier
- RF Automatic Gain Control (AGC) circuit
- Standby mode for power-down, no power switch circuitry required
- 2.7 V minimum supply voltage
- MPX output for RDS
- 3-wire bus
- In combination with the host, fast, low power operation of preset mode, manual search, automatic search and automatic store are possible
- Host can be in Sleep mode after tuning; a minute retuning is recommended to compensate for temperature and voltage fluctuations
- Covers all Japanese, European and US bands.

**PHILIPS**

### 3. Quick reference data

**Table 1: Quick reference data**

$V_{CCA} = V_{CCD}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CCA}$	analog supply voltage		2.7	3.0	5.0	V
$V_{CCD}$	digital supply voltage		2.7	3.0	5.0	V
$I_{CCA}$	analog supply current	operating	-	17	22	mA
		standby	-	1	100	$\mu$ A
$I_{CCD}$	digital supply current	operating	-	250	500	mA
		standby	-	1	100	$\mu$ A
$I_{LED}$	optional stereo LED		-	1	2	mA
$f_{FM(ant)}$	FM input frequency		76	-	108	MHz
$T_{amb}$	ambient temperature	$V_{CCA} = V_{CC(VCO)} = V_{CCD} = 3$ V	-10	-	+75	$^{\circ}$ C
		$V_{CCA} = V_{CC(VCO)} = V_{CCD} = 5$ V	-40	-	+85	$^{\circ}$ C
<b>FM overall system parameters</b>						
$V_{i(RF)}$	RF sensitivity input voltage	$f_{RF} = 76$ MHz to 108 MHz; $\Delta f = 22.5$ kHz; $f_{mod} = 1$ kHz; (S+N)/N = 26 dB; de-emphasis = 75 $\mu$ s; $B_{AF} = 300$ Hz to 15 kHz; left = right	-	1	3	$\mu$ V
$SUP_{pilot}$	pilot suppression	$\Delta f_{pilot} = 6.75$ kHz; $\Delta f = 68.5$ kHz		40		dB
$IP3_{in}$	in-band 3rd order intercept point at LNA input		-	95	-	dB $\mu$ V
$IP3_{out}$	out-band 3rd order intercept point at LNA input		-	95	-	dB $\mu$ V
$S_{-300}$	LOW side 300 kHz selectivity	$\Delta f = -300$ kHz; $f_{RF} = 76$ MHz to 108 MHz	-	40	-	dB
$S_{+300}$	HIGH side 300 kHz selectivity	$\Delta f = 300$ kHz; $f_{RF} = 76$ MHz to 108 MHz	-	50	-	dB
$S_{-200}$	LOW side 200 kHz selectivity	$\Delta f = -200$ kHz; $f_{RF} = 76$ MHz to 108 MHz	-	30	-	dB
$S_{+200}$	HIGH side 200 kHz selectivity	$\Delta f = 200$ kHz; $f_{RF} = 76$ MHz to 108 MHz	-	40	-	dB
IR	image rejection	$f_{RF} = 76$ MHz to 108 MHz	-	26	-	dB
$V_{AUDL}$ ; $V_{AUDR}$	left and right audio output voltage	$V_{RF} = 1$ mV; left = right; $\Delta f = 22.5$ kHz; $f_{mod} = 1$ kHz	-	100	-	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	$V_{RF} = 1$ mV; left = right; $\Delta f = 22.5$ kHz; $f_{mod} = 1$ kHz de-emphasis = 75 $\mu$ s; $B_{AF} = 300$ Hz to 15 kHz	48	56	-	dB
$\alpha_{cs}$	stereo channel separation	$V_{RF} = 1$ mV; right = 1 and left = 0 or right = 0 and left = 1; $f_{mod} = 1$ kHz; $\Delta f_{pilot} = 6.75$ kHz; $\Delta f_{left} = 68.5$ kHz and $\Delta f_{right} = 0$ or $\Delta f_{right} = 68.5$ kHz and $\Delta f_{left} = 0$	15	25	-	dB

Table 1: Quick reference data ...continued

$V_{CCA} = V_{CCD}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$V_{RF} = 1 \text{ mV}$ ; left = right; $\Delta f = 75 \text{ kHz}$ ; $f_{mod} = 1 \text{ kHz}$ ; $B_{AF} = 300 \text{ Hz to } 15 \text{ kHz}$	-	0.7	1.5	%
		$V_{RF} = 1 \text{ mV}$ ; left = right; $\Delta f = 22.5 \text{ kHz}$ ; $f_{mod} = 1 \text{ kHz}$ ; $B_{AF} = 300 \text{ Hz to } 15 \text{ kHz}$	-	0.2	0.7	%
DEEM	integrated de-emphasis		-	50/75	-	$\mu\text{s}$

## 4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TEA5880TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

5. Block diagram

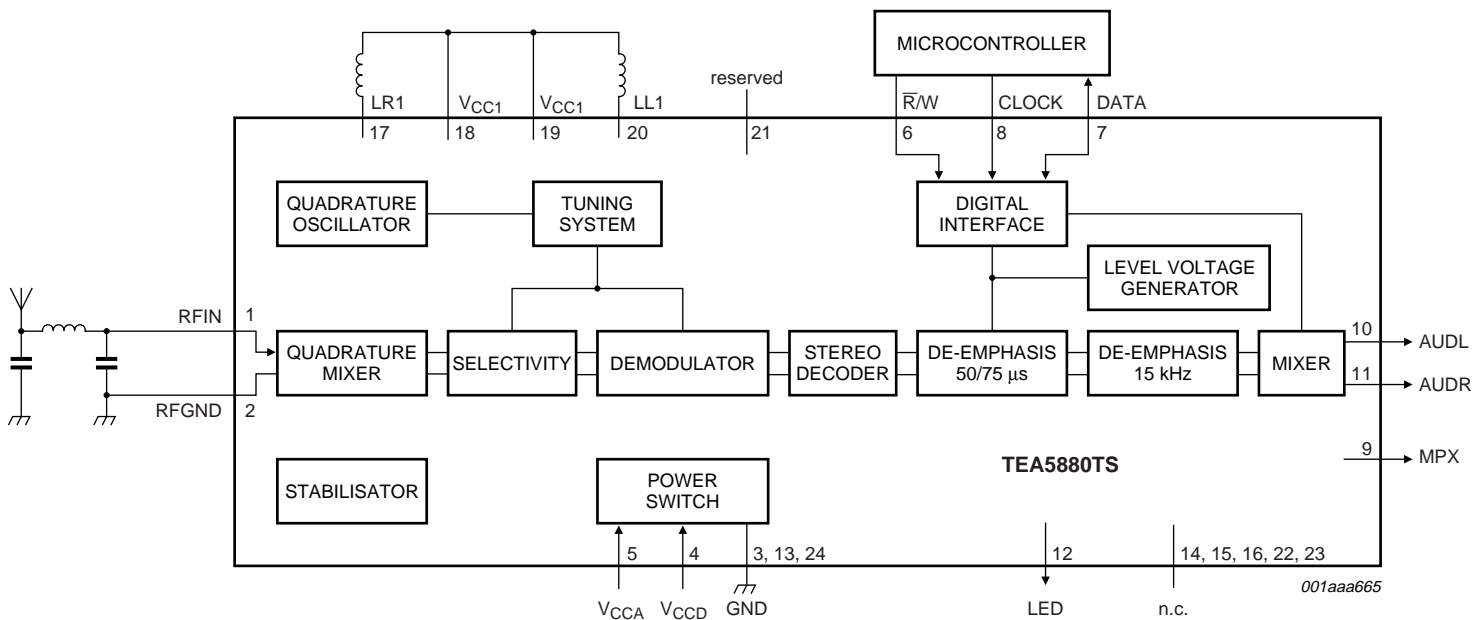


Fig 1. Block diagram.

Depending on the antenna design the filter components at pins 1 and 2 may not be necessary. The only two remaining coils connected to pin 17 to 20 can be replaced by printed-circuit board traces that will fit underneath the TEA5880TS resulting in a design without any external components; see [Section 14](#) for details on the printed-circuit board coils.

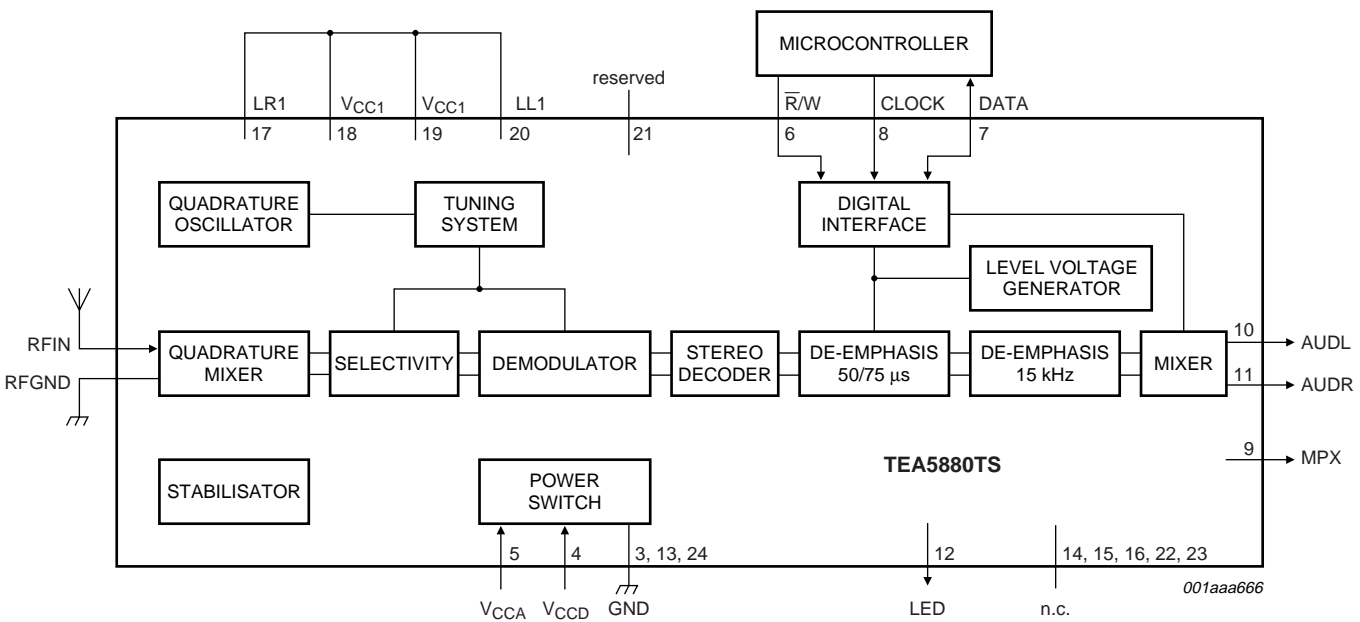


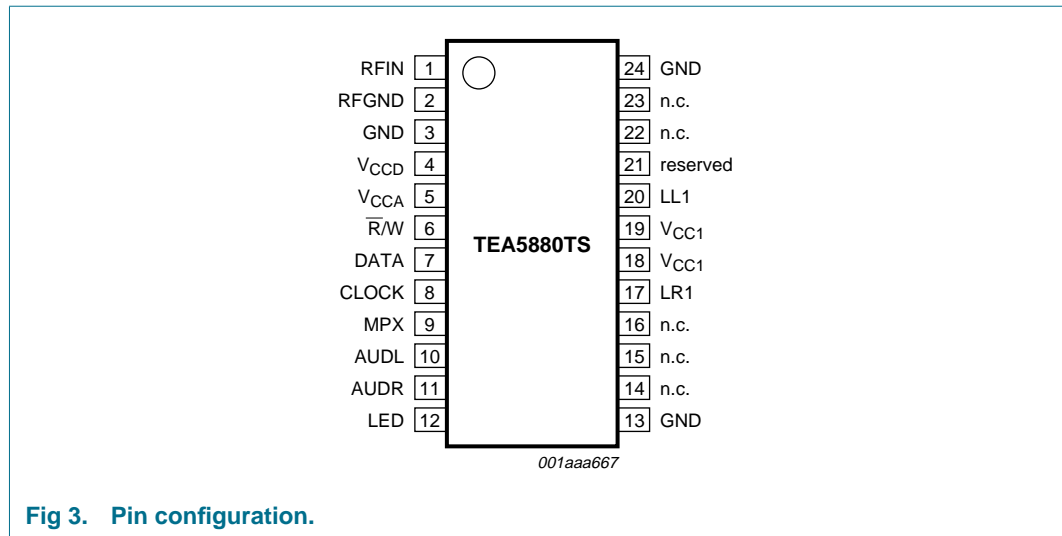
Fig 2. Block diagram (no external components).

## 6. Pinning information

### 6.1 Pin description

Table 3: Pin description

Symbol	Pin	Description
RFIN	1	RF input
RFGND	2	RF ground
GND	3	ground
V <sub>CCD</sub>	4	digital supply voltage
V <sub>CCA</sub>	5	analog supply voltage
$\bar{R}/W$	6	digital read/write command input
DATA	7	bidirectional digital data line
CLOCK	8	digital data clock line input
MPX	9	FM MPX signal output
AUDL	10	audio left channel output
AUDR	11	audio right channel output
LED	12	stereo LED output
GND	13	ground
n.c.	14	not connected
n.c.	15	not connected
n.c.	16	not connected
LR1	17	coil right
V <sub>CC1</sub>	18	internal analog voltage
V <sub>CC1</sub>	19	internal analog voltage
LL1	20	coil left
reserved	21	reserved for testing use
n.c.	22	not connected
n.c.	23	not connected
GND	24	ground



## 7. Functional description

### 7.1 FM quadrature mixer

The FM quadrature mixer converts FM RF (76 MHz to 108 MHz) to an IF of 110 kHz. The FM quadrature mixer provides inherent image rejection.

### 7.2 Quadrature oscillator

The internally tuned LC VCO provides the Local Oscillator (LO) signal for the FM quadrature mixer. The VCO frequency range is 150 MHz to 217 MHz.

### 7.3 Selectivity

Fully integrated I and Q channel IF filter.

### 7.4 Demodulator

The FM quadrature demodulator is an integrated PLL demodulator.

### 7.5 Level voltage generator and analog-to-digital converter

The level voltage is analog-to-digital converted with 3 bits and output via the data line.

### 7.6 IF counter

The IF counter outputs a 16-bit count result via the data line.

### 7.7 Mute

The digital interface controls the audio mute and output level.

### 7.8 Stereo decoder

The PLL stereo decoder is adjustment free. The stereo decoder can be switched to mono via the digital interface.

## 8. Digital interface (3-wire bus)

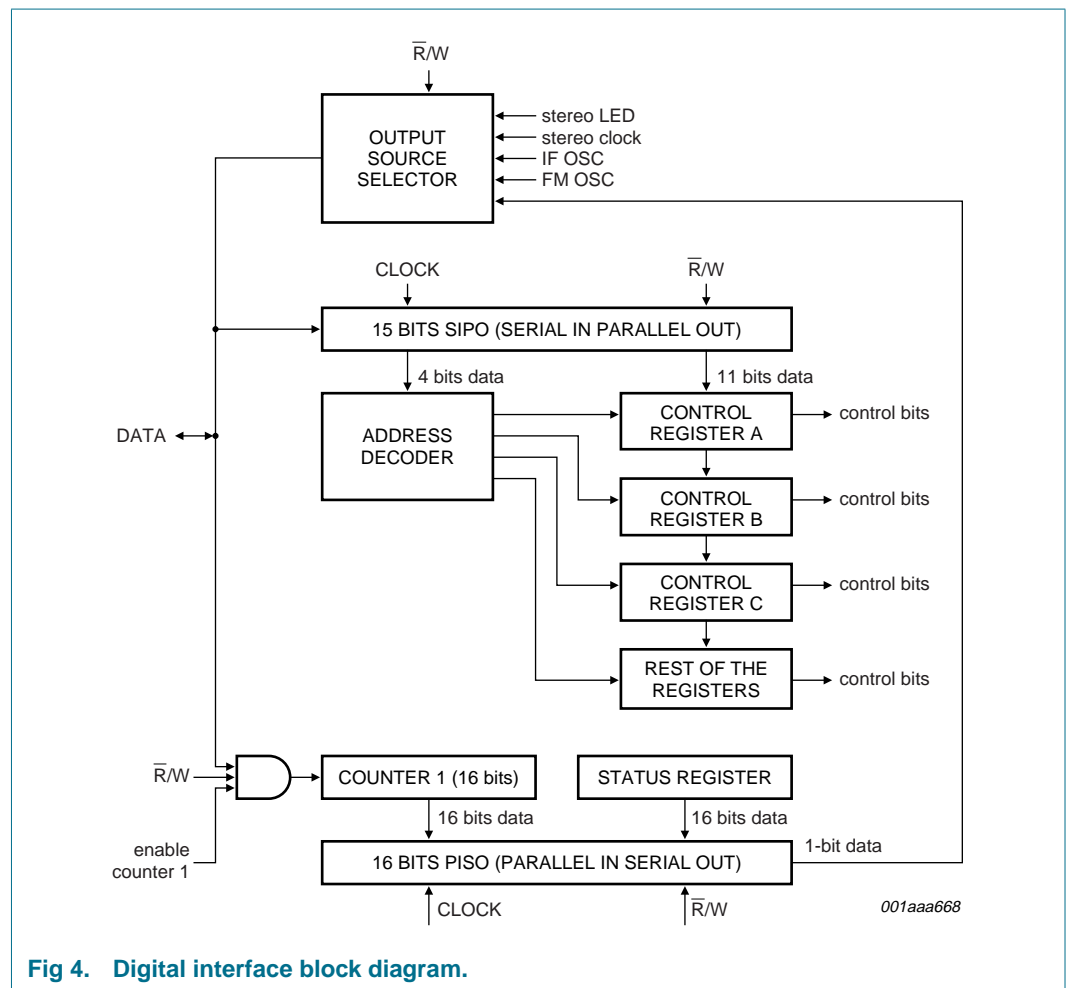
The TEA5880TS has a 3-wire bus with read/write, clock and data line.

The register set of the TEA5880TS can be accessed via the digital interface.

The pins given in [Table 4](#) are defined for the digital interface of the TEA5880TS.

**Table 4: Digital interface pins**

Pin number	Name	Type	Description	Remark
Pin 6	$\bar{R}/W$	input	LOW is read from TEA5880TS; HIGH is write to TEA5880TS	
Pin 8	CLOCK	input	clock	rising edge
Pin 7	DATA	input/output	bidirectional data	



**Fig 4. Digital interface block diagram.**



## 8.1 Register description

**Table 5: TEA5880TS registers description**

Address	Register name	Access	Operation	Data width	Clocks
0000b	VADC	write only	VADC register	11 bits	15
0001b	CTRL_C	write only	control register C	11 bits	15
0010b	CTRL_A	write only	control register A	11 bits	15
0011b	OSC_STEREO	write only	oscillator stereo decoder clock	11 bits	15
0100b	CTRL_B	write only	control register B	11 bits	15
0101b	CAP_FM	write only	capacitor bank FM	11 bits	15
0110b	OSC_IF	write only	oscillator IF	11 bits	15
0111b	OSC_FM	write only	oscillator FM	11 bits	15
-	STATUS	read only	status register	16 bits	15
-	COUNTER	read only	counter register	16 bits	15

**Table 6: VADC - (address 0h) bit description**

Bit	Symbol	Description
14 to 11	-	address bits
10 to 6	VADC2[4:0]	controls the width filter
5	-	not applicable; should be written to logic 0
4 to 0	VADC1[4:0]	controls the center filter

**Table 7: CTRL\_C - (address 1h) bit description <sup>[1]</sup>**

Bit	Symbol	Description
14 to 11	-	address bits
10 and 9	-	reserved for production test; should be written to logic 0
8	-	reserved for swapping counters1 and 2; should be written to logic 0
7 to 4	-	not applicable; should be written to logic 0
3 to 1	-	reserved for time delay selection (counter 2); application should keep bits 3 to 1 at logic 0; see <a href="#">Table 8</a>
0	-	reserved for enable counter 2; should be written to logic 0

[1] The application should write logic 0 to this register at start-up to ensure that the device functions correctly.

**Table 8: Time delay selection**

Value	Decimal	Stop value
000b	0	count 2
001b	1	count 8
010b	2	count 32
011b	3	count 128
100b	4	count 512
101b	5	count 2048
110b	6	count 8192
111b	7	count 32768

Table 9: CTRL\_A - (address 2h) bit description

Bit	Symbol	Description
14 to 11	-	address bits
10 to 7	OUTPUT_SELECT[3:0]	selects an internal circuit as output for measurement purpose; see <a href="#">Table 10</a>
6	STE_PMUTE	<b>mutes the stereo PLL when set to logic 1</b> ; this bit should be set during calibration of the stereo decoder clock and should be cleared during normal operation
5	DEM_PMUTE	<b>mutes the demodulator PLL when set to logic 1</b> ; this bit should be set during calibration of the IF frequency and should be cleared during normal operation
4	STE_INT_OFF#	turns off the stereo integrator loop when set to logic 0
3	EN_MEAS#	enables measurement when set to logic 0
2	AMUTE	mutes the audio when set to logic 1
1	FM	enables the FM circuitry when set to logic 1
0	-	reserved for AM circuitry; should be written to logic 0

Table 10: Description of OUTPUT\_SELECT bits

Symbol	Value	Decimal	Output selected
OS-NONE	0000b	0	no output selected
OS_FM_OSC	0001b	1	FM oscillator
OS_NA2	0010b	2	not defined
OS_CNT2_RDY_NA	0011b	3	reserved for counter 2 ready output
OS_NA4	0100b	4	not defined
OS_STEREO_DEC	0101b	5	stereo decoder clock
OS_NA6	0110b	6	not defined
OS_STEREO_LED	0111b	7	stereo LED
OS_NA8	1000b	8	not defined
OS_IF_OSC	1001b	9	IF oscillator
OS_INTERRUPT_NA	1010b	10	reserved for interrupt output
OS_PISO	1011b	11	PISO output (reading STATUS / COUNTER register)
OS_NA12	1100b	12	not defined
OS_RDS_NA	1101b	13	reserved for RDS output
OS_NA14	1110b	14	not defined
OS_NA15	1111b	15	not defined

Table 11: OSC\_STEREO - (address 3h) bit description <sup>[1]</sup>

Bit	Symbol	Description
14 to 11	-	address bits
10 to 0	SO[10:0]	11-bit digital-to-analog converter for adjusting the stereo decoder clock

[1] The frequency is decreased when increasing the content of this register.

Table 12: CTRL\_B - (address 4h) bit description

Bit	Symbol	Description
14 to 11	-	address bits
10	L_CNT	<b>latch counter:</b> a transition from logic 1 to logic 0 will latch the COUNTER register into the PISO (reading the PISO hereafter will read the COUNTER register)
9	L_STS	<b>latch status:</b> a transition from logic 1 to logic 0 will latch the STATUS register into the PISO (reading the PISO hereafter will read the STATUS register)
8 to 6	-	reserved for output level control; should be written with 4 (100b); see <a href="#">Table 13</a>
5	DEEMP	<b>de-emphasis:</b> logic 1 is 75 $\mu$ s (USA), logic 0 is 50 $\mu$ s (Europe, Japan)
4	PISO_CLR	a transition from logic 1 to logic 0 will clear the PISO; the PISO should be clear before reading the STATUS/COUNTER register
3	CNT_RST	a transition from logic 1 to logic 0 will clear both counter 1 and counter 2
2	CNT1_EN	counter 1 enabled (counting mode) when set to logic 1
1	-	should be written to logic 0
0	MONO	mono mode when set to logic 1, stereo mode when set to logic 0

Table 13: Description of output level control register bits

Value	Decimal	Output level
0000b	0	12 mV
0001b	1	20 mV
0010b	2	35 mV
0011b	3	60 mV
0100b	4	100 mV
0101b	5	170 mV
0110b	6	200 mV

Table 14: CAP\_FM - (address 5h) bit description <sup>[1]</sup>

Bit	Symbol	Description
14 to 11	-	address bits
10	-	reserved for capacitor extra current; this bit should be written to logic 1 by any access to the CAP_FM to ensure that the device functions properly
9 to 8	-	reserved, should be written to logic 0
7 to 0	FC[7:0]	FM capacitor bank switches for adjusting the FM (RF) frequency in big steps. Every bit, when set, will switch on a capacitor with a weight according to its position i.e. bit 0 has weight 1, bit 1 has weight 2, bit 2 has weight 4 etc, bit 6 has weight 64, except for bit 7, which also has the same weight as bit 6; there is thus only $7\frac{1}{2}$ effective bits; this means that the value range 0 to 127 will switch on different capacitors the value range 128 to 191 switches on the same capacitors as range 64 to 127, the value range 192 to 255 will switch on different capacitors (an overlapped range of 64 values caused when FC[7:6] = 01b or 10b)

[1] The frequency is decreased when increasing the content of this register (more capacitors).

**Table 15: OSC\_IF - (address 6h) bit description [1]**

Bit	Symbol	Description
14 to 11	-	address bits
10 to 0	I FO[10:0]	11-bit digital-to-analog converter for adjusting the IF frequency

[1] The frequency is decreased when increasing the content of this register.

**Table 16: OSC\_FM - (address 7h) bit description [1]**

Bit	Symbol	Description
14 to 11	-	address bits
10 to 0	FO[10:0]	11-bit digital-to-analog converter for adjusting the FM frequency in fine steps; this register is used in combination with the CAP_FM register to set a FM frequency

[1] The frequency is increased when increasing the content of this register.

**Table 17: STATUS - bit description [1]**

Bit	Symbol	Description
15 to 9	FS[6:0]	field strength, indicated by the amount of bits set: 0 bits set = < 10 dB $\mu$ V 1 bit set = 10 dB $\mu$ V to 20 dB $\mu$ V 2 bits set = 20 dB $\mu$ V to 30 dB $\mu$ V 3 bits set = 30 dB $\mu$ V to 40 dB $\mu$ V 4 bits set = 40 dB $\mu$ V to 50 dB $\mu$ V 5 bits set = 50 dB $\mu$ V to 60 dB $\mu$ V 6 bits set = 60 dB $\mu$ V to 70 dB $\mu$ V 7 bits set = > 70 dB $\mu$ V
8	-	not applicable; always read as logic 1
7 to 5	R[2:0]	chip revision; the revision for TEA5880TS is 100b
4 to 3	-	not applicable; always read as logic 1
2	-	reserved for production test
1	-	not applicable; always read as logic 1
0	-	reserved for production test

[1] This register does not have an address. To read the status register, latch its content into the PISO (using L\_STS bit in control register B) then read out the PISO.

**Table 18: COUNTER - bit description [1]**

Bit	Symbol	Description
15 to 0	CNT[15:0]	pulses counted during the period that the counter is enabled and the NR/W line the 3 wire bus is low

[1] This register does not have an address. To read the counter register, latch its content into the PISO (using L\_CNT bit in control register B) then read out the PISO.

## 8.2 Accessing the TEA5880TS

Access to the TEA5880TS can be achieved via the 3-wire bus. At the host side, the  $\bar{R}/W$  and CLOCK are output signals, while the DATA signal is bidirectional.

When powered up, the host should initialize the 3-wire bus in the host read mode as follows:

1. Set (at host side) the DATA line into input mode
2.  $\bar{R}/W$  set to LOW
3. CLOCK set to LOW.

Note: Use the following sequence for changing read/write mode:

1. To change from host read mode to host write mode proceed as follows:
  - a. Keep the CLOCK signal LOW
  - b. Set the  $\bar{R}/W$  signal to HIGH (write mode)
  - c. Set the DATA pin (of the application controller) into output mode.
2. To change from host write mode to host read mode proceed as follows:
  - a. Keep the CLOCK signal LOW
  - b. Set the DATA pin (of the application controller) into input mode
  - c. Set  $\bar{R}/W$  to LOW (input mode).

## 8.3 Writing to the TEA5880TS

Writing to the TEA5880TS is achieved with a 15-bit data pattern:

- D[14:11]: 4-bit register address
- D[10:0]: 11-bit register data.

The data pattern is sent serially to the TEA5880TS as follows:

1. Drive  $\bar{R}/W$  pin HIGH to set the TEA5880TS in input mode
2. Drive the DATA pin to correct level
3. Generate positive edge of CLOCK (driving CLOCK into LOW-to-HIGH transition)
4. Delay some time to meet the data hold time requirement
5. Driving CLOCK into HIGH-to-LOW transition
6. Repeat step (2) to (5) 15 times to shift the 15-bit data pattern into the TEA5880TS
7. Drive  $\bar{R}/W$  pin LOW; this signals the TEA5880TS to latch the data into the correct register.

Note: The application should shift the LSB out first.

## 8.4 Reading from the TEA5880TS

Only the status or the counter register can be read from the TEA5880TS.

These are 16-bit registers and can be read serially as follow:

1. Select OS\_PISO (parallel in, serial out) as output (control register A, OUTPUT\_SELECT bits)
2. Clear the PISO (control register B, PISO\_CLR bit, pulse HIGH-to-LOW transition)
3. Latch the counter register (control register B, L\_CNT bit, pulse HIGH-to-LOW transition) or the status register (control register B, L\_STS bit, pulse HIGH-to-LOW transition) into the PISO
4. Drive  $\bar{R}/W$  pin LOW to set the TEA5880TS in output mode
5. Read the first bit at pin DATA
6. Generate positive CLOCK pulse (LOW-to-HIGH transition)
7. Delay for a period of time to meet the data set-up time requirement
8. Read the data bit at pin DATA
9. Drive CLOCK into HIGH-to-LOW transition
10. Repeat step (6) to (9) 15 times to shift the remaining 15 bits of data out of the chip

Note: The TEA5880TS will shift the MSB out first.

## 8.5 Measuring frequency with the TEA5880TS

The three frequencies: IF, stereo decoder clock and FM can be measured by using the counter register and a software timing window. This is achieved as follows:

1. Select the output to be measured (control register A, OUTPUT\_SELECT bits, select OS\_STEREO\_DEC, OS\_IF\_OSC or OS\_FM\_OSC output)
2. Enable measure mode (clear EN\_MEAS# bit of control register A)
3. Reset the counter (control register B, CNT\_RST bit, pulse HIGH-to-LOW transition)
4. Start the counter on the TEA5880TS (control register B, set CNT1\_EN bit); at the moment the  $\bar{R}/W$  signal goes LOW the counter starts
5. Wait time  $t$
6. To stop the counter, first set the  $\bar{R}/W$  signal HIGH, then disable the counter in the TEA5880TS (control register B, clear CNT1\_EN bit)
7. Read the pulse count  $n$  from the counter register of the TEA5880TS
8. Restore the measure mode
9. Restore the output select bits.

Note: The measuring window begins at the moment the  $\bar{R}/W$  signal is driven LOW (point 4) and ends when the  $\bar{R}/W$  signal is driven HIGH (point 6).

The IF and stereo decoder frequency can be calculated using the equation  $f = n/t$ , and the FM frequency can be calculated using the equation  $f = (n/t) \times 256$ .

Note: The precision of 'f' depends on the following:

- The duration of t. 1 pulse wrong at t = 1 ms results in more deviation than at t = 32 ms
- The precision of the measuring window: calculate with t = 32 ms gives other 'f' values than with t = 32 ms. In the application care should be taken to have an accurate measuring window t.

### 8.6 Initialize the TEA5880TS

After power-up, the TEA5880TS needs to be initialized as follows:

- Control register A: STE\_PMUTE = 1; DEM\_PMUTE = 1; AMUTE = 1; FM = 1; other bits = 0
- Control register B: CNT\_RST = 1; PISO\_CLR = 1; MONO = 1; DEEMP = 1 (for Europe); Bit [8:6] = 100b; other bits = 0
- Control register C: All bits = 0
- VADC register: VADC1 = 26 (decimal), this value should not be changed hereafter; VADC2 = 18 (decimal), this value should not be changed hereafter
- Calibrate the IF frequency at 110 kHz
- Calibrate the stereo decoder clock at 37.5 kHz (to reduce the initialization time, calibration of the stereo decoder clock can be postponed until the stereo mode is selected).

## 9. Timing diagrams

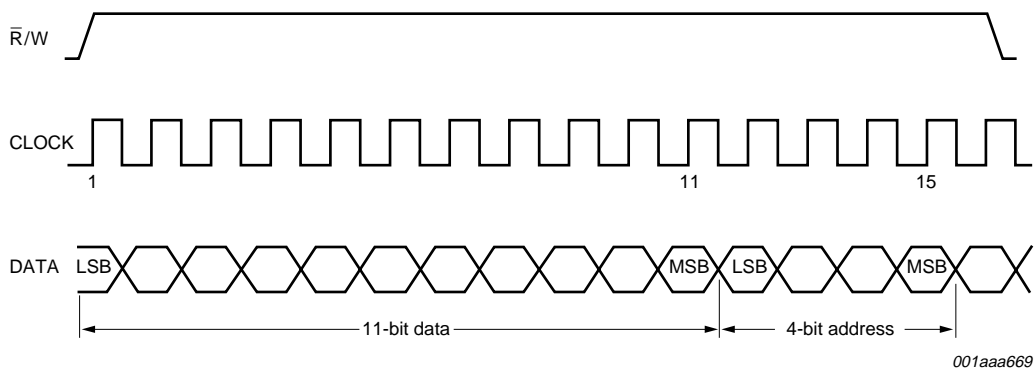
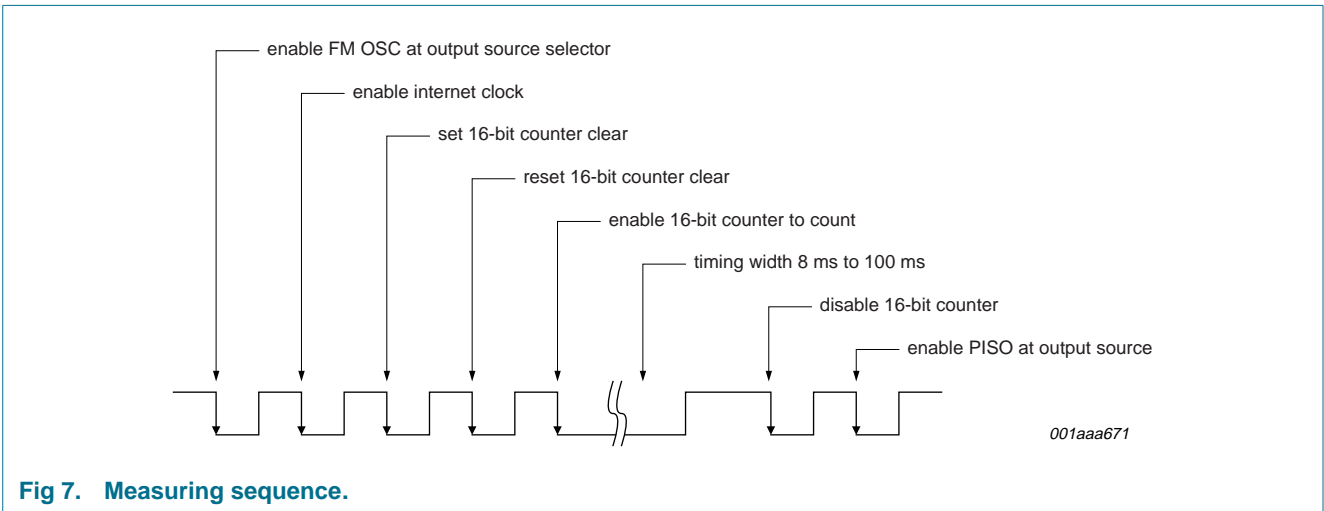
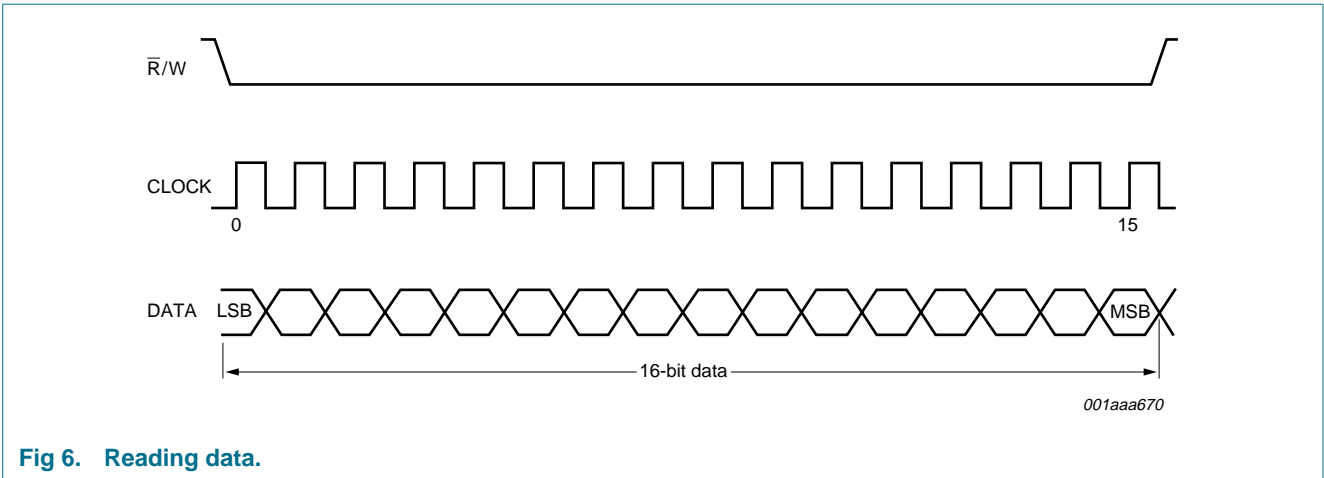


Fig 5. Writing data.





## 10. Limiting values

**Table 19: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCD}$	digital supply voltage		-0.3	+5	V
$V_{CCA}$	analog supply voltage		-0.3	+8	V
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	ambient temperature	$V_{CCA} = V_{CC(VCO)} = V_{CCD} = 3\text{ V}$	-10	+75	°C
		$V_{CCA} = V_{CC(VCO)} = V_{CCD} = 5\text{ V}$	-40	+85	°C
$V_{esd}$	electrostatic discharge voltage for all pins	[1]	-200	+200	V
		[2]	-2000	+2000	V

[1] Machine model (R = 10  $\Omega$ , C = 200 pF, 75  $\mu$ H).

[2] Human body model (R = 1.5 k $\Omega$ , C = 100 pF).

## 11. Thermal characteristics

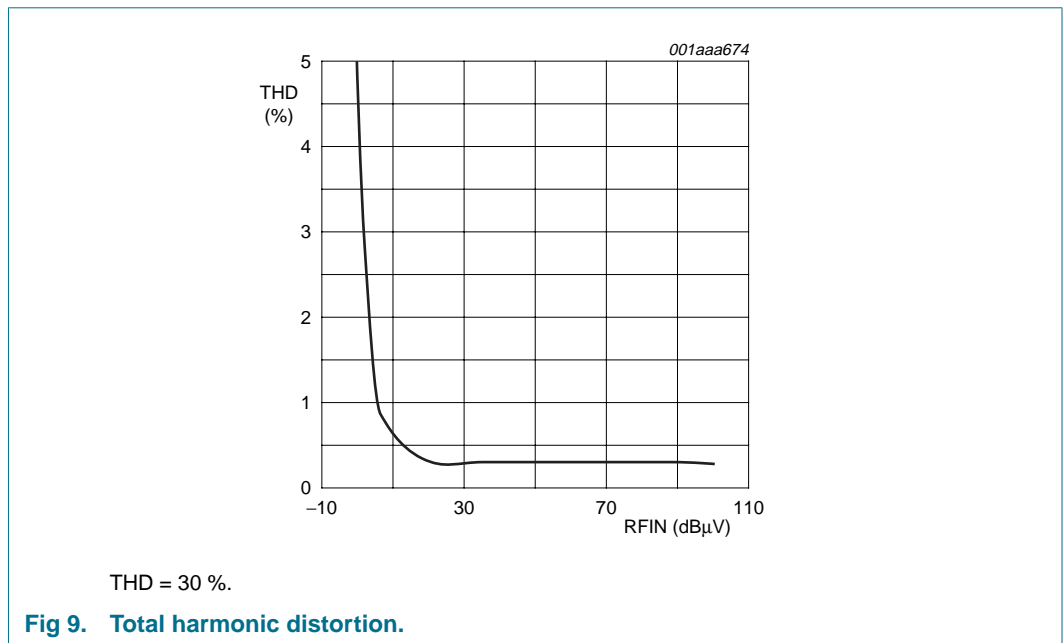
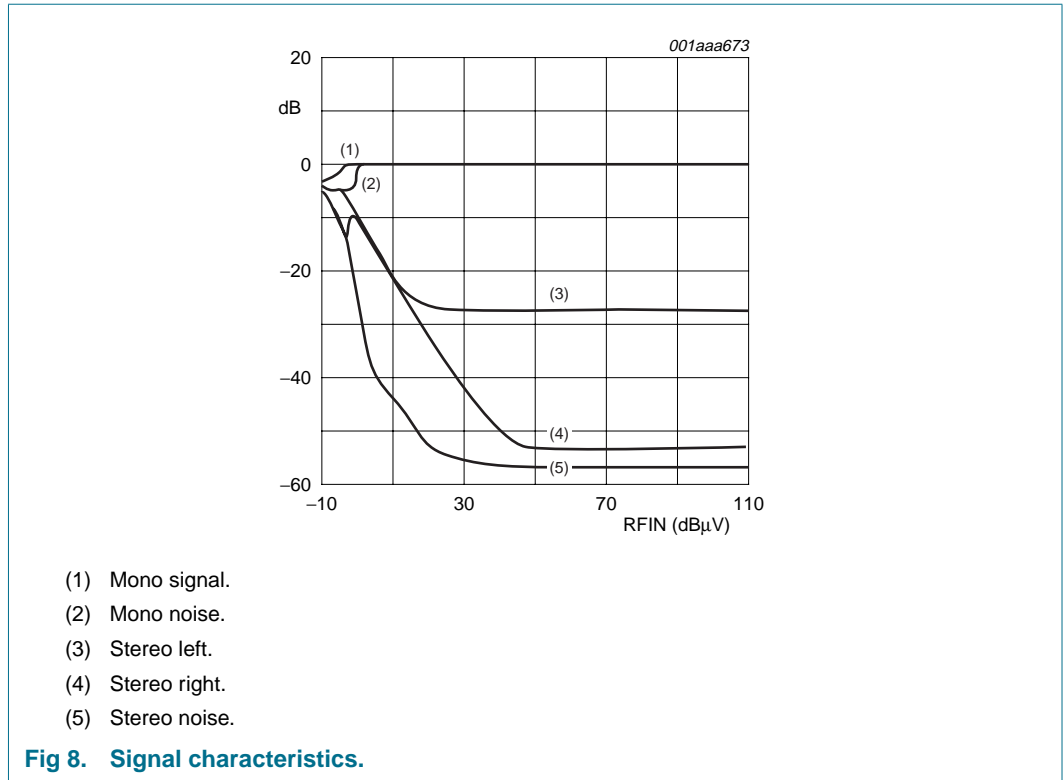
**Table 20: Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	<td>	K/W

## 12. Characteristics

**Table 21: Digital input AC values**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Digital inputs</b>						
$V_{IH}$	HIGH-level input voltage	$I_{OH} = 500\text{ }\mu\text{A}$	1.4	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.6	V
<b>Digital outputs</b>						
$I_{sink(L)}$	LOW-level sink current		500	-	-	$\mu\text{A}$
$V_{OL}$	LOW-level output voltage	$I_{OL} = 500\text{ }\mu\text{A}$	-	-	0.6	V
<b>Timing</b>						
$f_{clk}$	clock input		-	-	1	MHz
$t_{CLK(H)}$	clock HIGH time		495	-	-	ns
$t_{CLK(L)}$	clock LOW time		495	-	-	ns



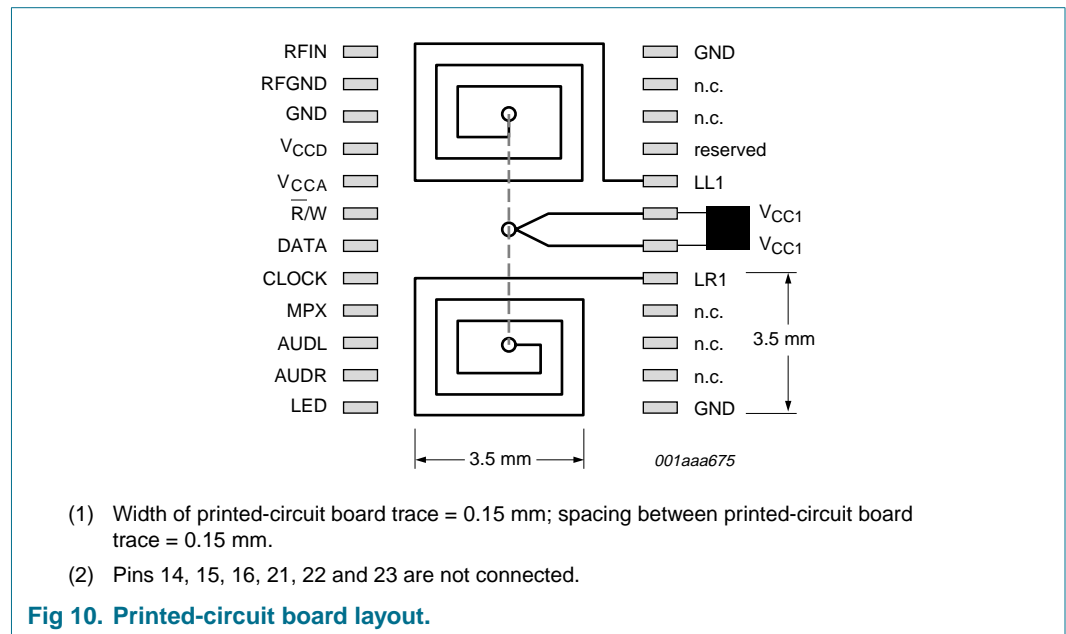
### 13. Components list

No external components necessary.

### 14. Printed-circuit board layout for SSOP24 package

The printed-circuit board traces from LL1 to  $V_{CC1}$  and from  $V_{CC1}$  to LR1 as shown in [Figure 10](#), are to create two inductors, each of approximately 38 nH. These inductors, together with internal capacitors, form part of the LC oscillator to determine the FM tuning band. If the value of the inductors becomes much greater than 38 nH, the whole FM tuning band (normally from 76 MHz to 108 MHz) will be shifted lower. If the value of the inductors becomes much smaller than 38 nH, the whole FM tuning band (normally from 76 MHz to 108 MHz) will be shifted higher.

If the layout of the two inductance traces is not preferred, two SMD inductors can be used to replace the two printed-circuit board inductance traces as an alternative. The layout of the two SMD inductors should be as close to the pins as possible.



15. Application information

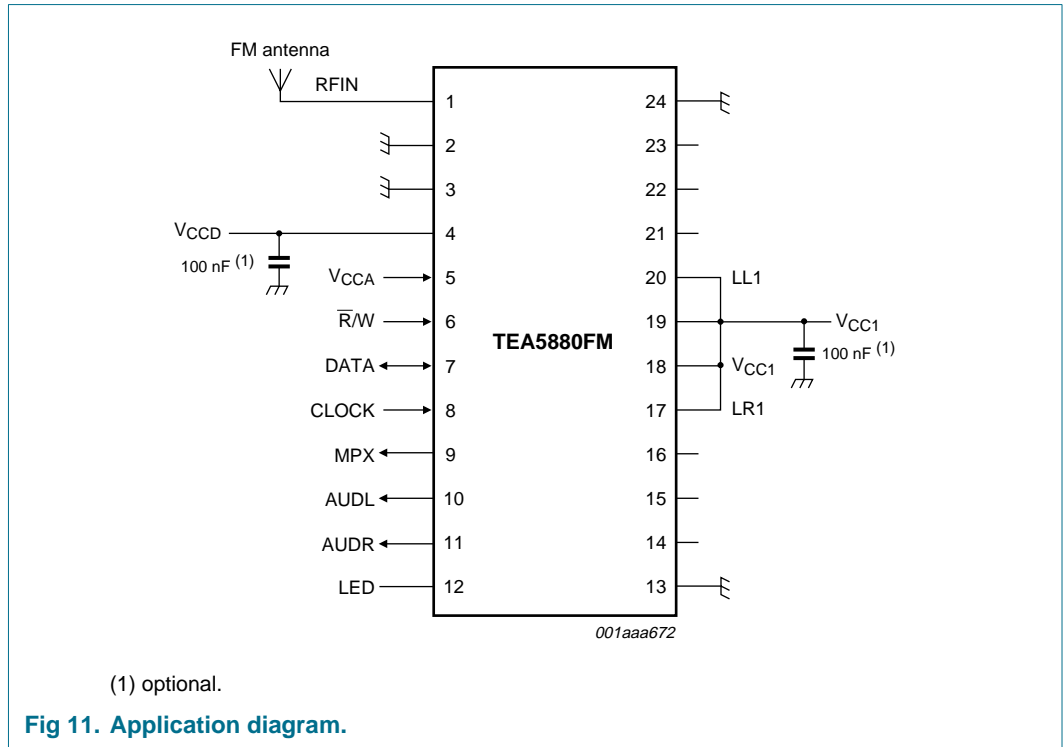


Fig 11. Application diagram.

16. Package outline

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

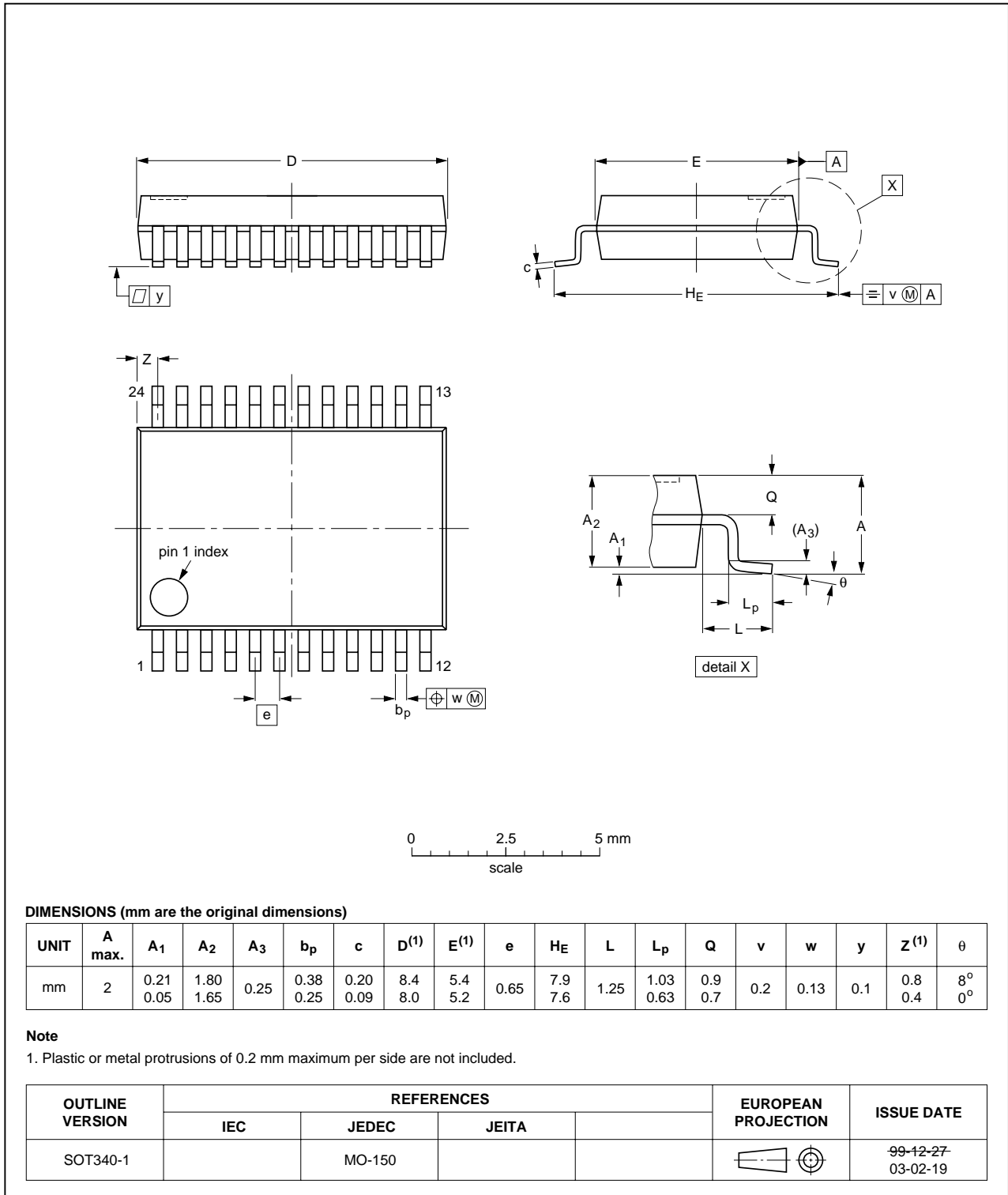


Fig 12. Package outline.

## 17. Soldering

### 17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 17.5 Package related soldering information

**Table 22: Suitability of surface mount IC packages for wave and reflow soldering methods**

Package <sup>[1]</sup>	Soldering method	
	Wave	Reflow <sup>[2]</sup>
BGA, HTSSON..T <sup>[3]</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>[3]</sup> , TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>[4]</sup>	suitable
PLCC <sup>[5]</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>[5]</sup> <sup>[6]</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>[7]</sup>	suitable
CWQCCN..L <sup>[8]</sup> , PMFP <sup>[9]</sup> , WQCCN..L <sup>[8]</sup>	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.



## 18. Revision history

Table 23: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
TEA5880_2	20040426	Preliminary data sheet	-	9397 750 13022	-

## 19. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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