

Mono BTL audio amplifier with DC volume control

TDA7052B

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7052B and TDA7052BT are 1 W and 0.5 W mono Bridge-Tied Load (BTL) output amplifiers with DC volume control.

They have been designed for use in TV and monitors, but are also suitable for use in battery-fed portable recorders and radios.

A Missing Current Limiter (MCL) is built in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (300 mA typ.). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_O	output power	$V_P = 6\text{ V}$				
	TDA7052B	$R_L = 8\ \Omega$	0.9	1.0	–	W
	TDA7052BT	$R_L = 16\ \Omega$	0.5	0.55	–	W
$G_{V(max)}$	maximum total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control		68	73.5	–	dB
$I_{q(tot)}$	total quiescent current	$V_P = 6\text{ V}; R_L = \infty$	–	9.2	13	mA
THD	total harmonic distortion					
	TDA7052B	$P_O = 0.5\text{ W}$	–	0.3	1	%
	TDA7052BT	$P_O = 0.25\text{ W}$	–	0.3	1	%

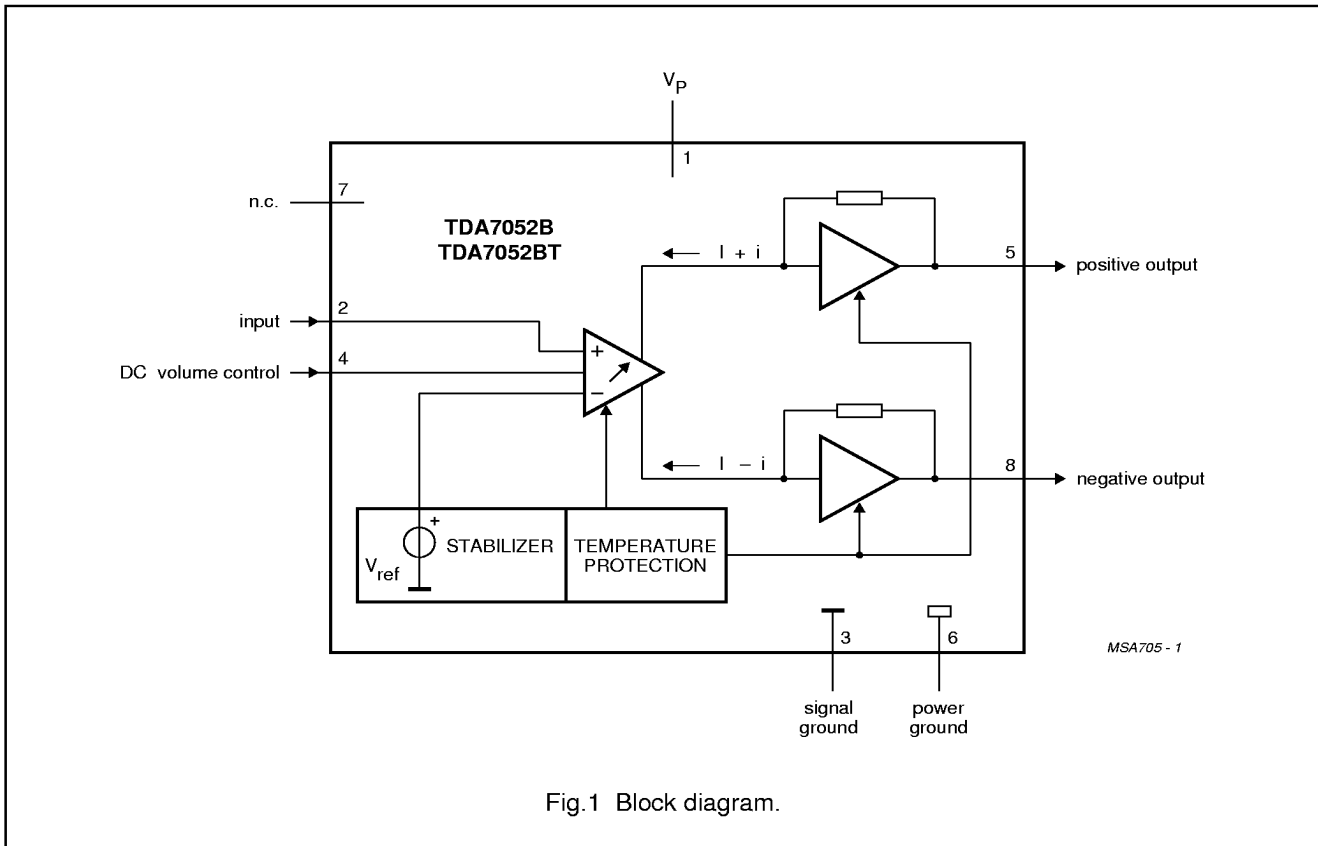
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7052B	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA7052BT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

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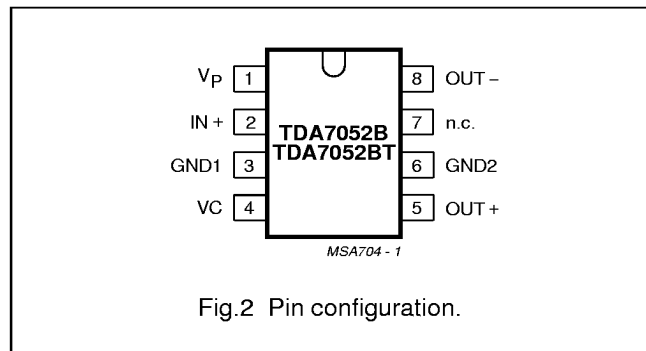
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BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
V _P	1	supply voltage
IN+	2	input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c.	7	not connected
OUT-	8	negative output



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FUNCTIONAL DESCRIPTION

The TDA7052B and TDA7052BT are mono BTL output amplifiers with DC volume control which have been designed for use in TV and monitors but are also suitable for use in battery-fed portable recorders and radios.

In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low. In the TDA7052B and TDA7052BT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required. With this configuration, a low offset voltage is maintained and the minimum supply voltage remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions. For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stage has a logarithmic control characteristic. Therefore, the total gain can be controlled from 40.5 dB to -33 dB. If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power. Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

Power dissipation

Assume for the TDA7052B that $V_P = 6\text{ V}$; $R_L = 8\ \Omega$.

The maximum sine wave dissipation is 0.9 W.

The $R_{th\ j-a}$ of the package is 100 K/W.

Therefore $T_{amb(max)} = 150 - 100 \times 0.9 = 60\text{ °C}$.

Assume for the TDA7052BT that $V_P = 6\text{ V}$; $R_L = 16\ \Omega$.

The maximum sine wave dissipation is 0.46 W.

The $R_{th\ j-a}$ of the package is 155 K/W.

Therefore $T_{amb(max)} = 150 - 155 \times 0.46 = 78\text{ °C}$.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
$V_{2,4}$	input voltage pins 2 and 4		–	5	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	1.25	W
	TDA7052B		–	0.8	W
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	h

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	TDA7052B	100	K/W
	TDA7052BT	155	K/W

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CHARACTERISTICS

$V_P = 6\text{ V}$; $V_{DC} = 1.4\text{ V}$; $f = 1\text{ kHz}$; $R_L = 8\ \Omega$; $T_{amb} = 25\text{ }^\circ\text{C}$; unless otherwise specified (see Fig.13).

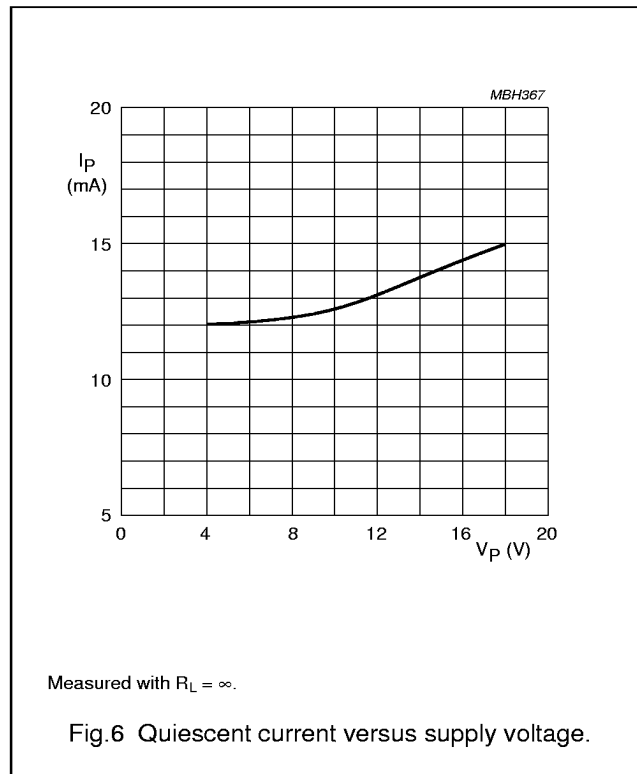
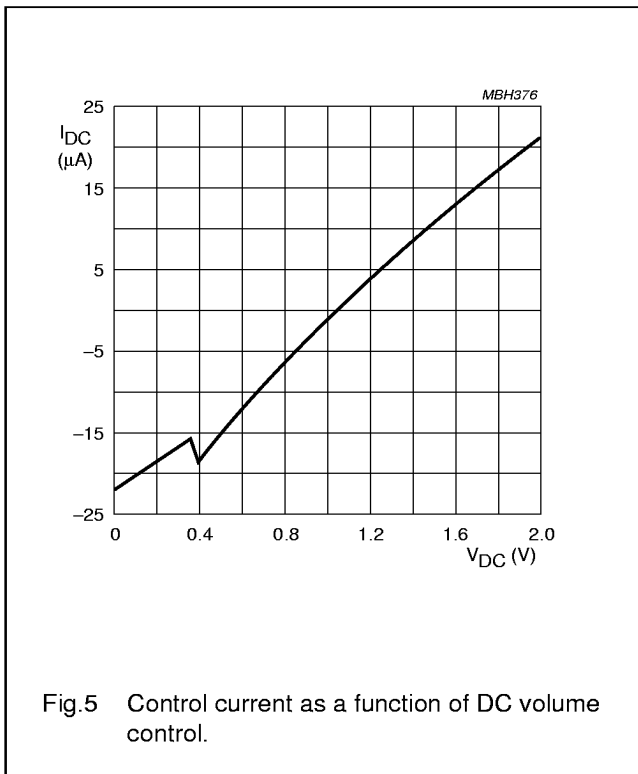
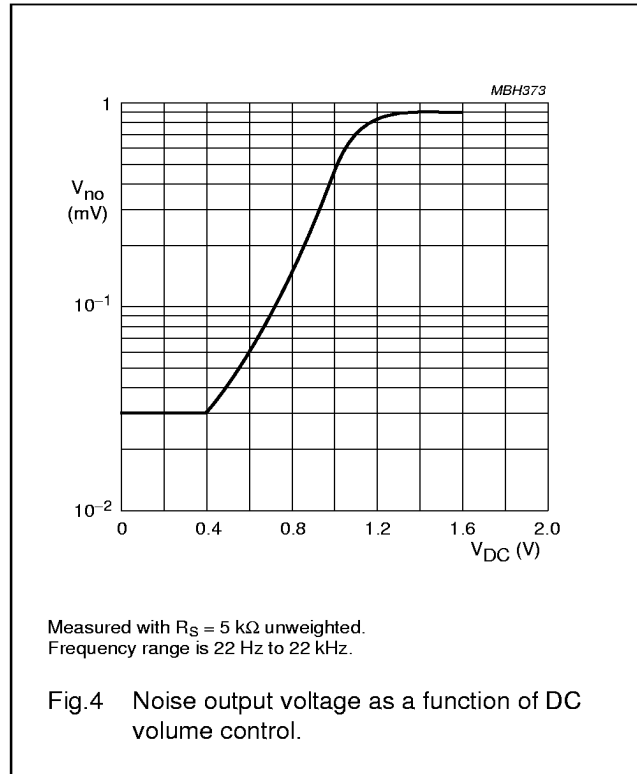
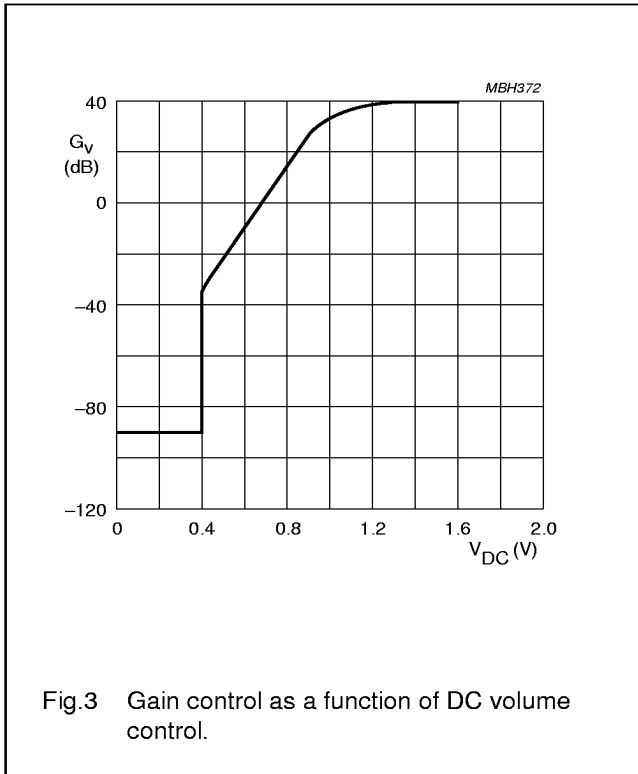
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4.5	–	18	V
$I_{q(\text{tot})}$	total quiescent current	note 1; $R_L = \infty$	–	9.2	13	mA
Maximum gain ($V_4 = 1.4\text{ V}$)						
P_O	output power TDA7052B TDA7052BT	THD = 10%	0.9 0.5	1.0 0.55	– –	W W
THD	total harmonic distortion TDA7052B TDA7052BT	$P_O = 0.5\text{ W}$ $P_O = 0.25\text{ W}$	– –	0.3 0.3	1 1	% %
$G_{v(\text{max})}$	maximum total voltage gain		39.5	40.5	41.5	dB
V_I	input signal handling (RMS value)	$G_{v(\text{max})} = 0\text{ dB}$; THD < 1%	1.0	–	–	V
V_{no}	noise output voltage (RMS value)	note 2; $f = 500\text{ kHz}$	–	210	–	μV
B	bandwidth	at –1 dB	–	0.02 to 300	–	kHz
SVRR	supply voltage ripple rejection	note 3	48	60	–	dB
$ \Delta V_O $	DC output offset voltage	$ V_8 - V_5 $	–	0	200	mV
Z_I	input impedance (pin 3)		15	20	25	k Ω
Mute position						
V_O	output voltage in mute position	note 4; $V_4 \leq 0.4\text{ V}$; $V_I = 1.0\text{ V}$	–	–	30	μV
DC volume control; note 5						
ϕ	gain control		68	73.5	–	dB
I_4	control current	$V_4 = 0\text{ V}$	–20	–25	–30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L .
2. The noise output voltage (RMS value) at $f = 500\text{ kHz}$ is measured with $R_S = 0\ \Omega$ and $B = 5\text{ kHz}$.
3. The ripple rejection is measured with $R_S = 0\ \Omega$ and $f = 100\text{ Hz}$ to 10 kHz . The ripple voltage V_R of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with $R_S = 5\text{ k}\Omega$ unweighted.
5. The DC volume control can be configured in several ways. Two possible circuits are shown in Figs 14 and 15. The circuits at the volume control pin will influence the switch-on and switch-off behaviour and the maximum voltage gain.

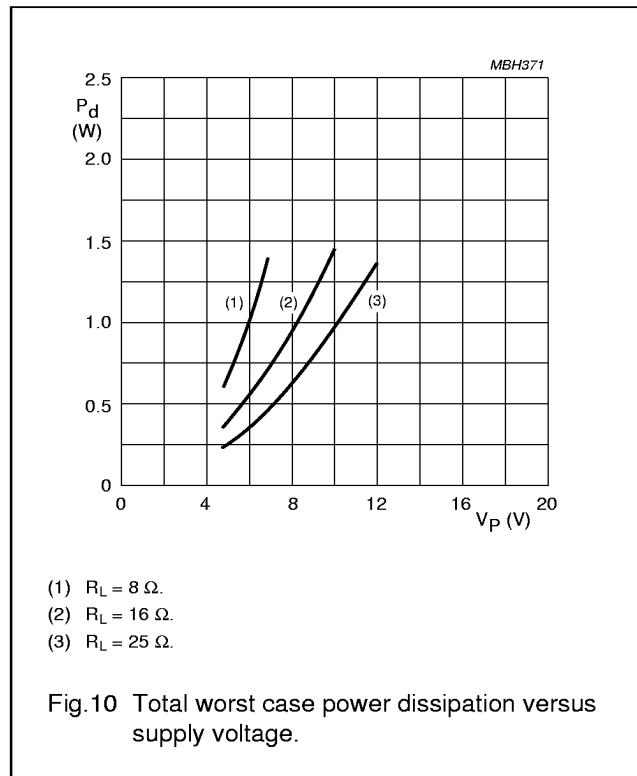
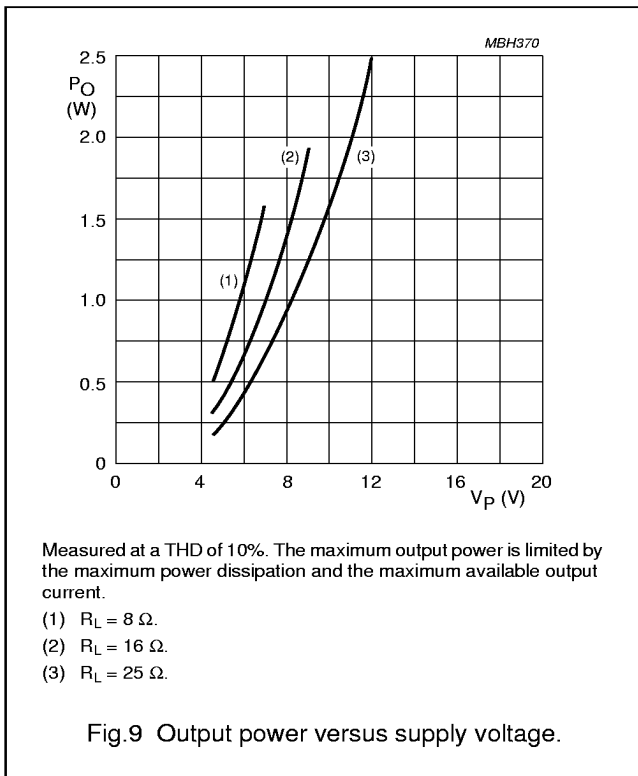
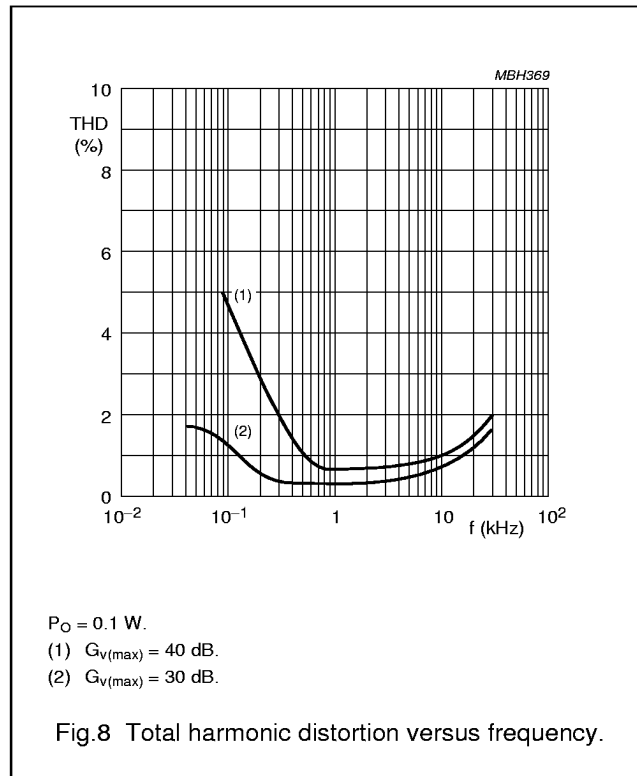
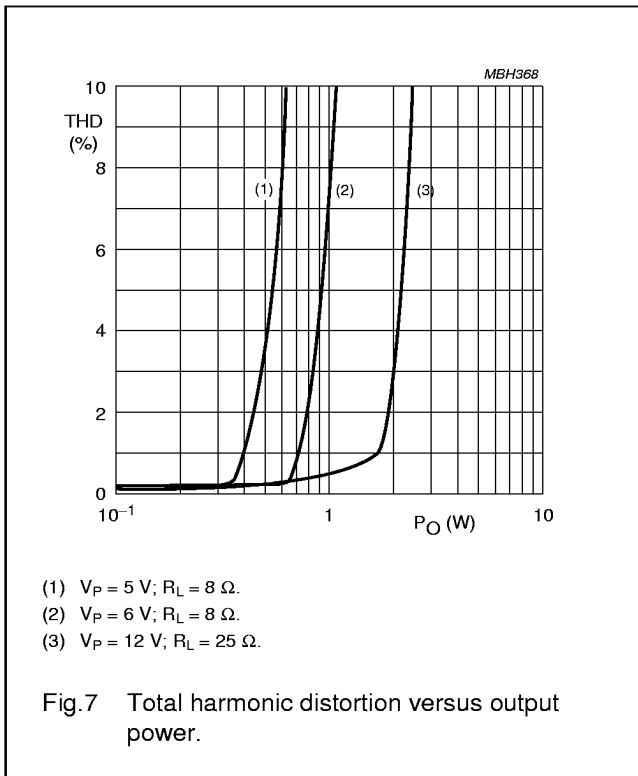
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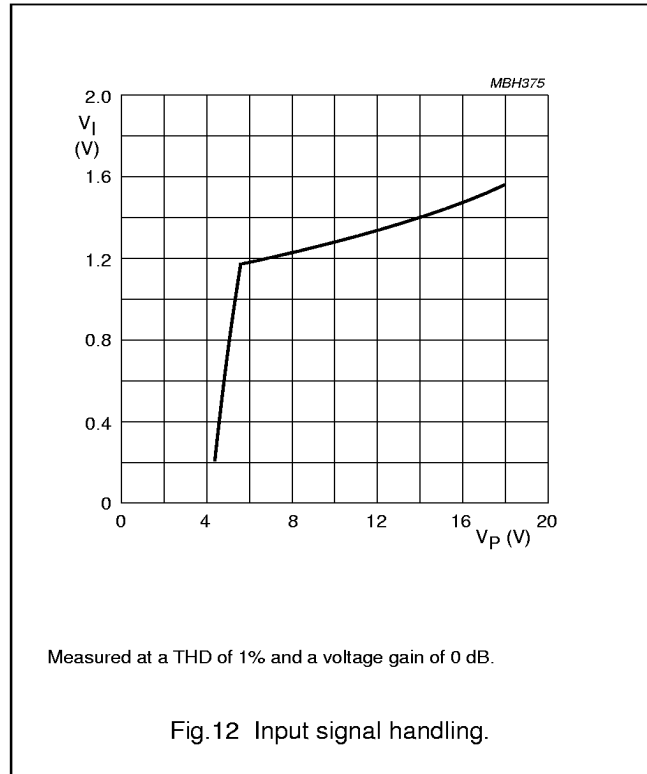
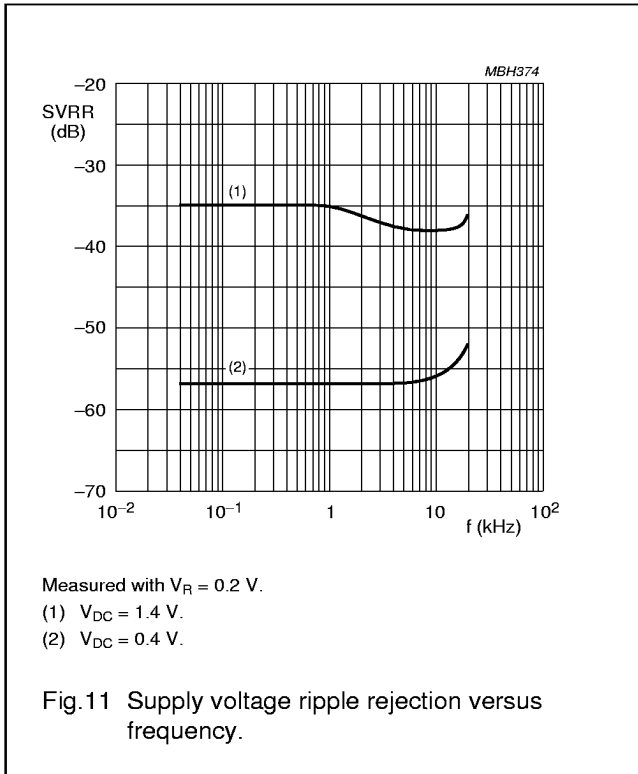
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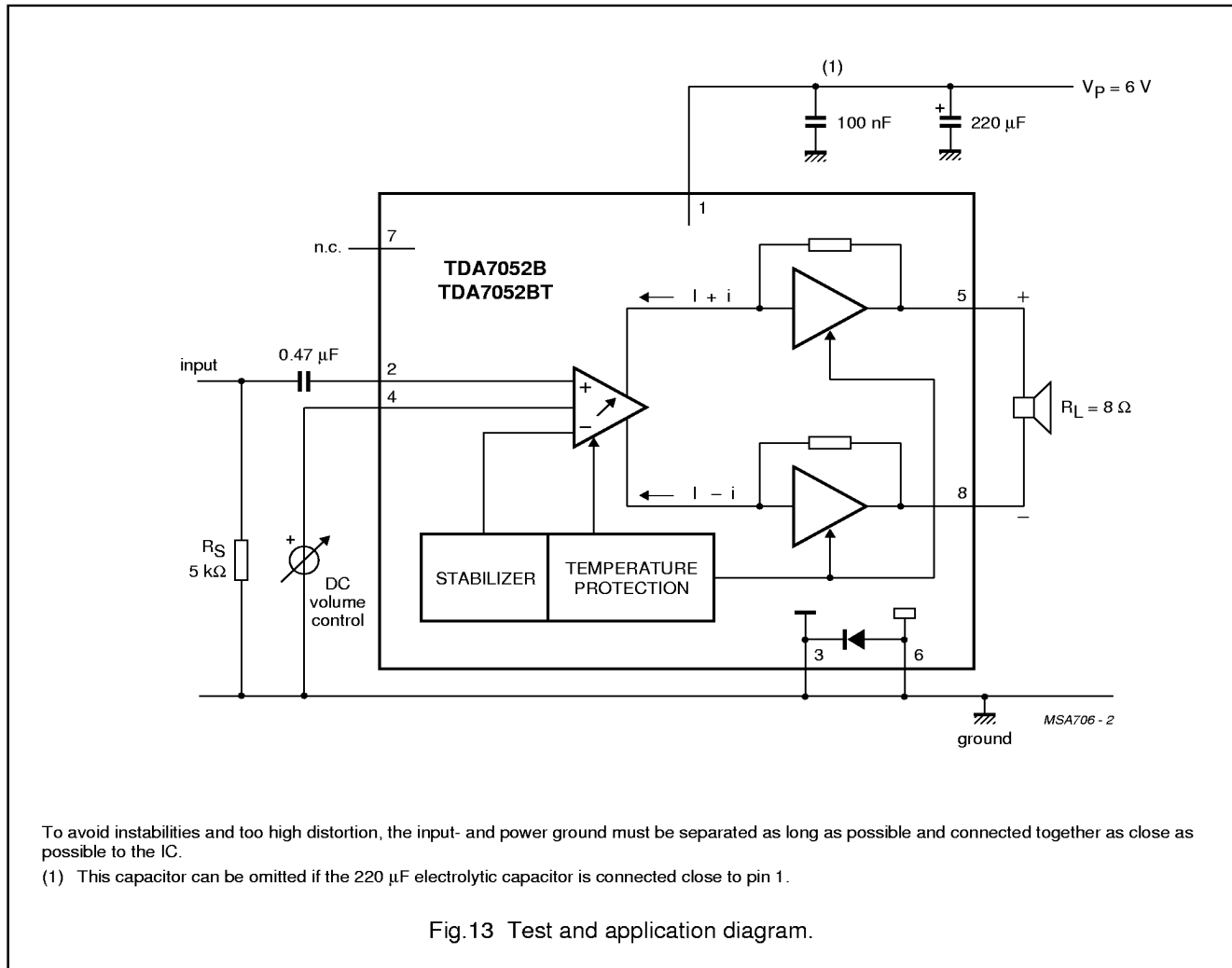
QUALITY SPECIFICATION

In accordance with "SNW-FQ-611E", if this type is used as an audio amplifier.

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TEST AND APPLICATION INFORMATION



For single-end application the output peak current may not exceed 100 mA; at higher output currents the short circuit protection (MCL) will be activated.

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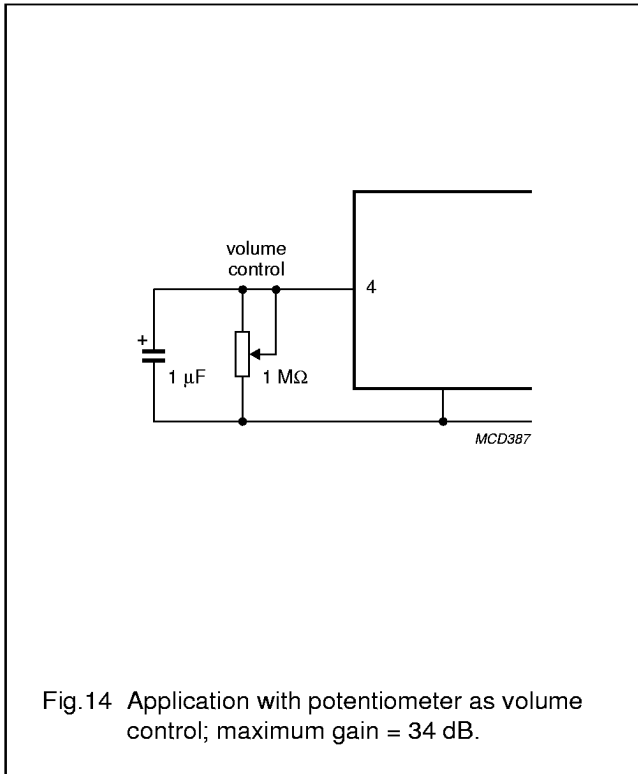


Fig. 14 Application with potentiometer as volume control; maximum gain = 34 dB.

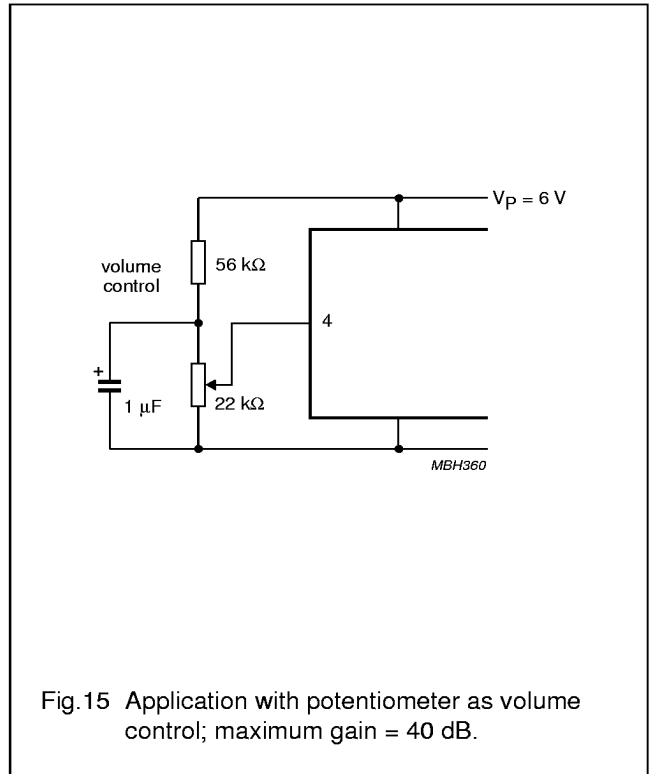


Fig. 15 Application with potentiometer as volume control; maximum gain = 40 dB.

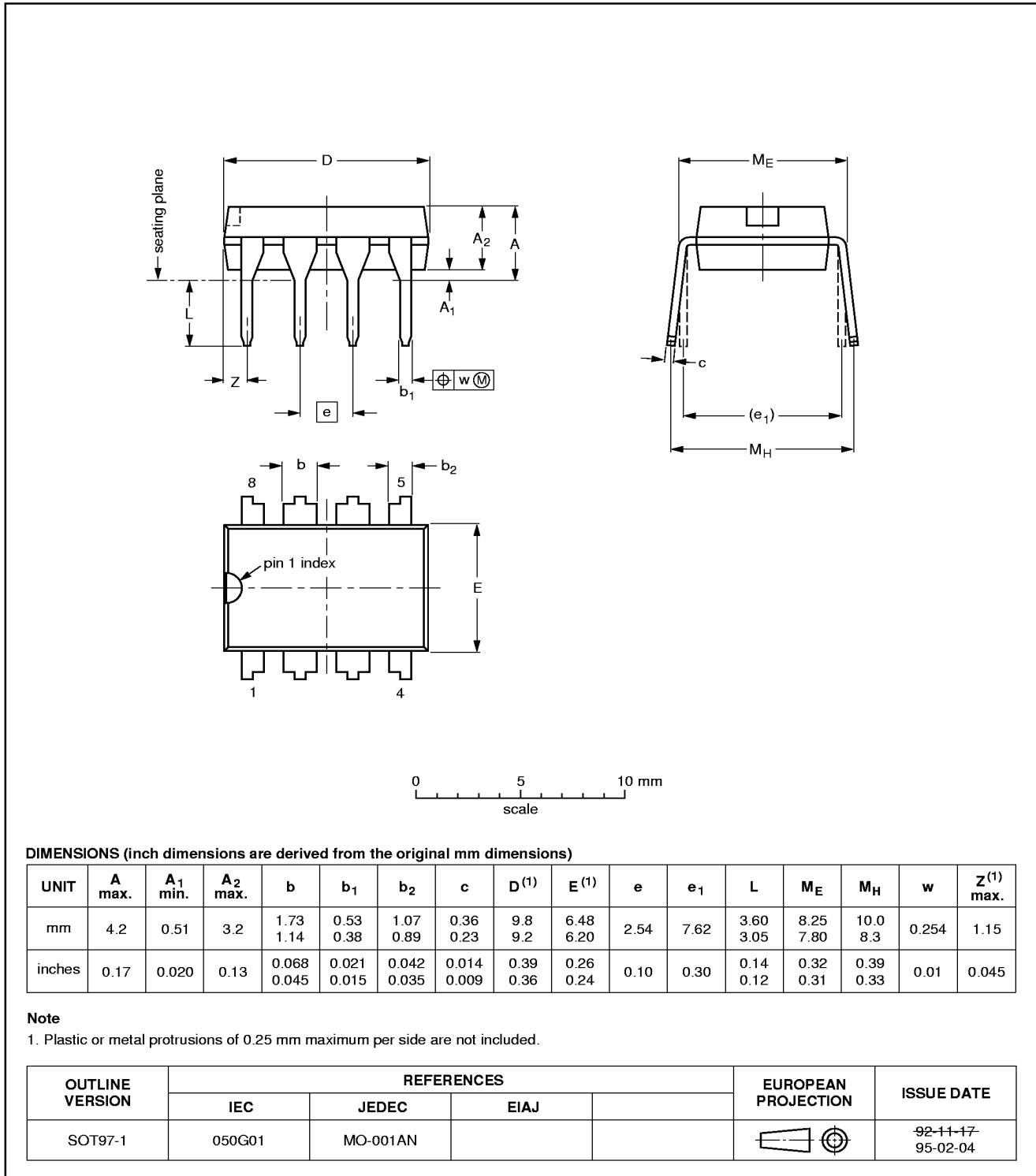
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PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1

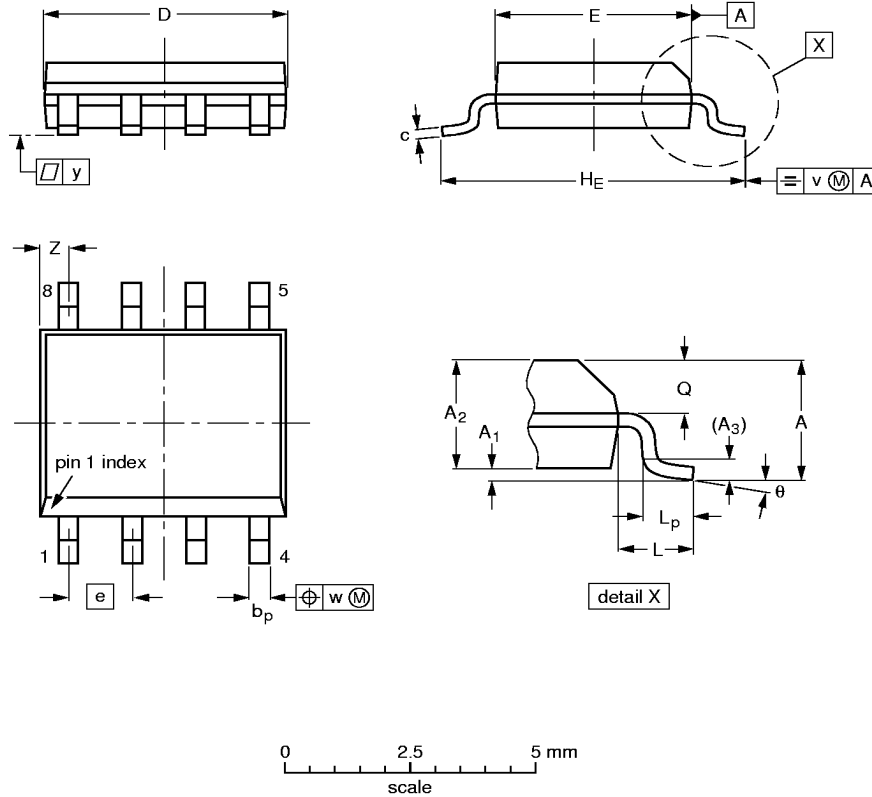


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S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				95-02-04 97-05-22

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.