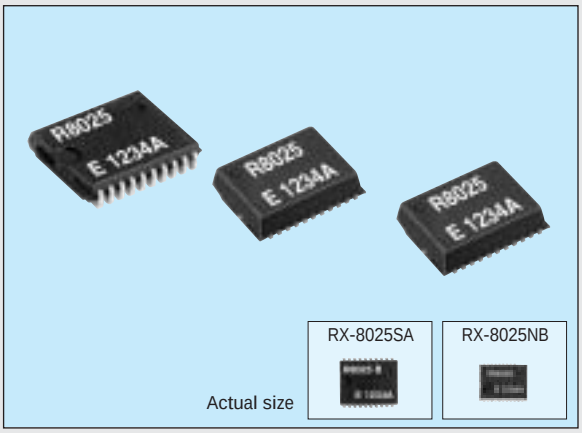
I² C-BUS INTERFACE REAL TIME CLOCK MODULE

RX-8025SA/NB

Product number (please refer to page 2)

Q4180255xxxxx00
Q4180259xxxxx00

- Built-in frequency adjusted 32.768 kHz crystal unit.
- Compliant with I²C high-speed bus specifications. (400 kHz)
- Dual Alarm and Timer IRQ function are Available.
- 32.768 kHz clock frequency output. (FOE, FOUT)
- Low backup current : 0.48 µA/3 V (Typ.)
- Wide operating voltage range : 1.7 V to 5.5 V
- Wide timekeeper voltage range : 1.15 V to 5.5 V



The details are mentioned in the application manual.

http://www.epsondevice.com

Specifications (characteristics)

Absolute Max. rating

GND=0V

Item	Symbol	Condition	Min.	Max.	Unit
Supply voltage	V_{DD}	VDD to GND	-0.3	+6.5	V
Input voltage	V_I	SCL,SDA,FOE pins	GND-0.3	+6.5	
Output voltage	V_{O1}	SDA, $\overline{INT}$, $\overline{INTB}$ pins	GND-0.3	+6.5	
	V_{O2}	FOUT pin	GND-0.5	V_{DD}+0.3	
Storage temperature Range	T_{STG}	Stored as bare product after unpacking	-55	+125	˚C

Operating range

GND=0V

Item	Symbol	Condition	Min.	Max.	Unit
Power voltage	V_{DD}	—	1.7	5.5	V
Clock voltage	V_{CLK}	—	1.15		
Operating temperature	T_{OPR}	No condensation	-40	+85	˚C

Frequency characteristics

GND=0V

Item	Symbol	Condition	Range	Unit
Frequency tolerance	Δf/f	Ta=+25 ˚C, VDD=3.0 V	AA : 5 ±5 ∗1	x 10^{-6}
Oscillation start-up time	t_{STA}	Ta=+25 ˚C, VDD=3.0 V	3 Max.	s
Frequency temperature characteristics	Top	Ta=-10˚C to +70˚C, V_{DD}=3.0 V ; Reference at +25˚C	+10 -120	x 10^{-6}
Frequency voltage characteristics	f/V	Ta=+25 ˚C, V_{DD}=2.0 V to 5.5 V	±1 Max.	x 10^{-6}
Aging	fa	Ta=+25 ˚C, VDD=3.0 V, first year	±5 Max.	x 10^{-6}/year

∗1 Equivalent to 15 seconds of monthly deviation (excluding offset.)

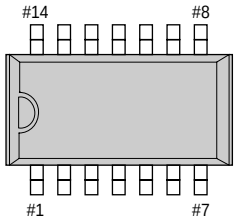
DC characteristics

(GND=0 V, VDD = 1.8 V to 5.5 V, Ta = -40 ˚C to +85 ˚C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Standby current	I_{DD2}	fSCL=0 Hz, FOE = GND, $\overline{INTA}$, $\overline{INTB}$ = V_{DD}, FOUT ; output off ("L" level)	V_{DD} = 3 V		0.48	1.20	µA
"H" input voltage	V_{IH}	SCL, SDA, FOE pins		0.8 V_{DD}		5.5	V
"L" input voltage	V_{IL}			GND -0.3		0.2 V_{DD}	
"H" output current	I_{OH}	FOUT pins, V_{OH} = V_{DD}-0.5 V				-0.5	mA
"L" output current	I_{OL1}	FOUT pins, V_{OL} = 0.4 V		0.5			
	I_{OL2}	$\overline{INTA}$, $\overline{INTB}$ pins, V_{OL} = 0.4 V		1.0			
	I_{OL3}	SDA pin, V_{OL} = 0.4 V		4.0			
Input leakage current	I_{IL}	SCL pins, V_I = 5.5 V or GND VDD = 5.5 V		-1		1	µA

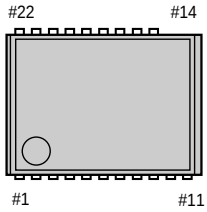
Terminal connection

RX-8025SA



No.	Pin terminal	No.	Pin terminal
1	N.C	14	N.C
2	SCL	13	SDA
3	FOUT	12	$\overline{INTB}$
4	N.C	11	GND
5	TEST	10	$\overline{INTA}$
6	V_{DD}	9	N.C
7	FOE	8	N.C

RX-8025NB

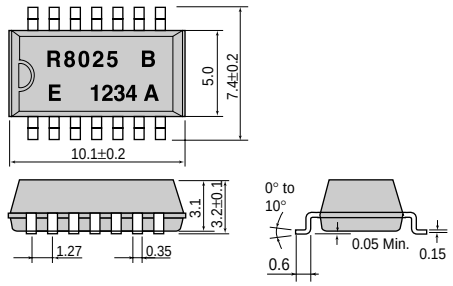


No.	Pin terminal	No.	Pin terminal
1	FOE	22	N.C
2	V_{DD}	21	N.C
3	N.C	20	N.C
4	TEST	19	N.C
5	FOUT	18	N.C
6	SCL	17	N.C
7	SDA	16	N.C
8	$\overline{INTB}$	15	N.C
9	GND	14	N.C
10	$\overline{INTA}$	13	—
11	N.C	12	—

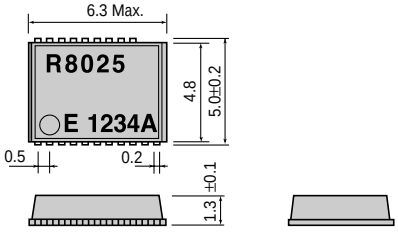
External dimensions

(Unit: mm)

RX-8025SA (SOP 14-pin)



RX-8025NB (SON 22-pin)



Register table

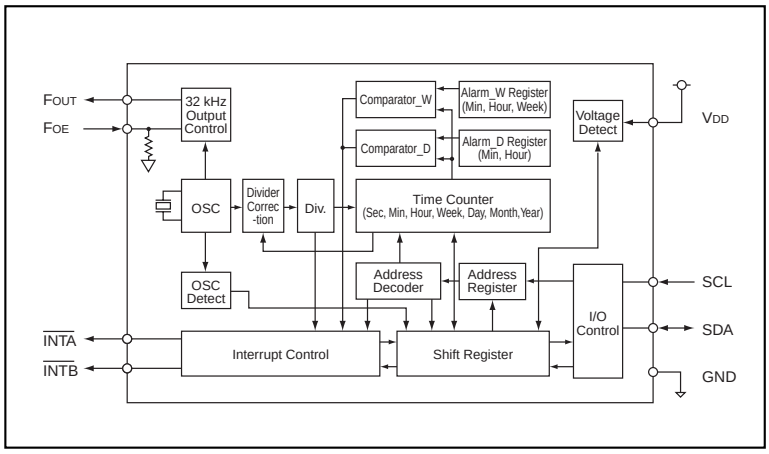
Address	Register symbol	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Seconds	o	S40	S20	S10	S8	S4	S2	S1
1	Minutes	o	M40	M20	M10	M8	M4	M2	M1
2	Hours	o	o	H20 P, $\overline{A}$	H10	H8	H4	H2	H1
3	Weekdays	o	o	o	o	o	W4	W2	W1
4	Days	o	o	D20	D10	D8	D4	D2	D1
5	Months	o	o	o	MO10	MO8	MO4	MO2	MO1
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
7	Digital Offset	o	F6	F5	F4	F3	F2	F1	F0
8	Alarm_W ; Minutes	o	WM40	WM20	WM10	WM8	WM4	WM2	WM1
9	Alarm_W ; Hour	o	o	WH20 WP, $\overline{A}$	WH10	WH8	WH4	WH2	WH1
A	Alarm_W ; Weekday	o	WW6	WW5	WW4	WW3	WW2	WW1	WW0
B	Alarm_D ; Minutes	o	DM40	DM20	DM10	DM8	DM4	DM2	DM1
C	Alarm_D ; Hour	o	o	DH20 DP, $\overline{A}$	DH10	DH8	DH4	DH2	DH1
D	Reserved	Reserved							
E	Control 1	WALE	DALE	$\overline{12}$, 24	•	TEST	CT2	CT1	CT0
F	Control 2	VDSL	VDET	$\overline{XST}$	PON *1	•	CTFG	WAFG	DAFG

0 : Always set this bit to “0”.

AC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	–		400	kHz
Tolerance spike time on bus	t_{SP}			50	ns
Start condition set-up time	$t_{SU;STA}$	0.6			µs
Start condition Hold time	$t_{HD;STA}$				
SCL “L” time	t_{LOW}	1.3			
SCL “H” time	t_{HIGH}	0.6			
SCL and SDA rise time	tr	–		0.3	
SCL and SDA fall time	tf				
Data set-up time	$t_{SU;DAT}$	200			ns
Data hold time	$t_{HD;DAT}$	0			
Stop condition set-up time	$t_{SU;STO}$	0.6			µs
Bus free time	t_{BUF}	1.3			

Block diagram



Timing chart