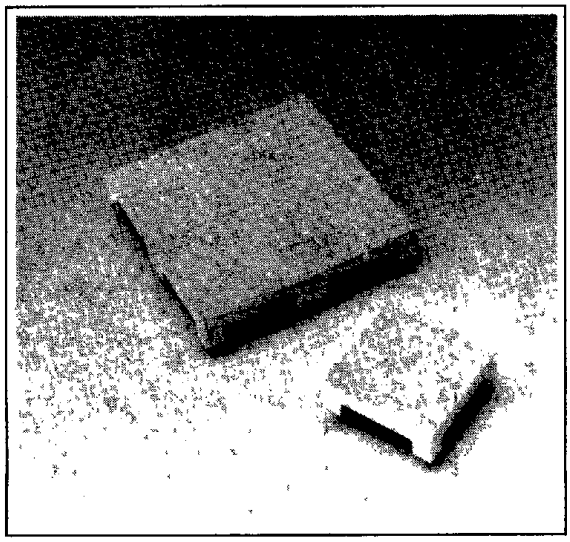
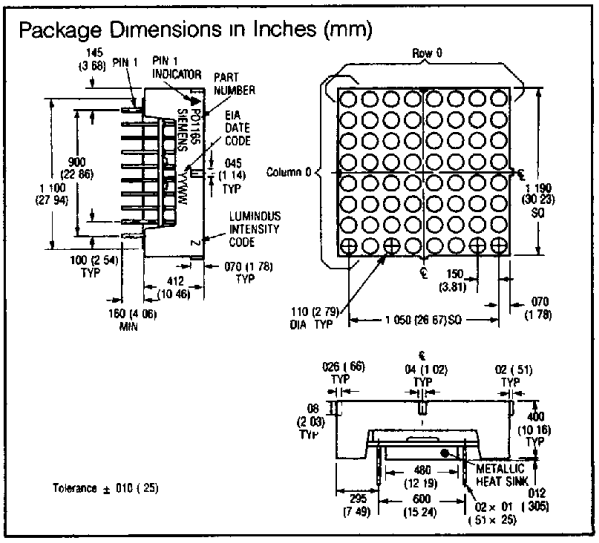
SIEMENS

T-41-37

HIGH EFFICIENCY RED PD1165
VERY BRIGHT GREEN PD1167

1.16″ Square 8 × 8 Dot Matrix Programmable Display™ Module With On Board Drivers, Built-In RAM and Software Controllable Features





FEATURES

- **Active Display Size 1.16″ Square**
- **0.11″ Diam. Dots on 0.15″ Centers**
- **Very Bright Green or High Efficiency Red**
- **Intensity Matched and Binned**
- **Readable from 35 Feet**
- **Viewing Angle ±75°**
- **Interlocking X-Y Stackable Packages for Larger Displays**
- **On board CMOS Circuits with Complete Drive Circuits and Logic Interfaces**
- **Each Dot Addressable Over TTL Compatible, 8 Bit BUS**
- **Alternate Language & Graphics Programming Capability**
- **Cascadable-Synchronizable Logic for Expanded Display Systems**
- **Software Controlled Attributes:**
  9 Levels of Intensity Settings
  Memory Clear
  Blanking or Blinking
  Built-In Lamp Test
- **100% Burned in Prior to Final Test**
- **20 Pin DIP Package: 0.6″ Wide Rows, 0.1″ Pin Spacing**
- **Wave Solderable**
- **−20°C to +70°C Operating Range**

DESCRIPTION

The high efficiency red PD 1165 and very bright green PD 1167 are modular 8×8 dot matrix Programmable Displays. They are constructed with highly efficient III/V material LEDs, packaged in a reflector package for maximum dot illumination. Further optimizing light output are built-in CMOS drive circuits. These circuits strobe the LEDs at peak currents that give the best time averaged luminous intensity for the power required. The user has complete control of the display through further built-in CMOS circuitry. The display appearance can be set by programming an 8 bit RAM.

Features such as blinking, synchronizing, blanking, one of nine intensity levels or lamp tests are easily programmed through a control word. Additional external connections are available for clock inputs, clock outputs and total intensity control through an external resistor.

All products are 100% burned-in and tested, then subjected to out-going AQL's of 25% for brightness matching, visual alignment and dimensions, .065% for electrical and functional.

The display is constructed of epoxy filled polycarbonate with two interconnected pcbs A heat sink is attached to cool the device with its 20 pin dip lead construction. The package is wave solderable and has been fully qualified for operation and storage over a temperature range from −20°C to +70°C.

Maximum Ratings

V_{CC}, DC Supply Voltage . . . . . −0.5 to +6.0 Vdc
V_{IN}, Input Voltage Levels Relative to GND (all inputs) . . . . . −0.5 to (V_{CC} +0 5) Vdc
Operating Temperature . . . . . −20°C to +70°C
Storage Temperature . . . . . −20°C to +70°C
Relative Humidity (non condensing) @65°C 90%
Power Dissipation @V_{CC} = 5 0 V, T_A = −20°C . . . . . 1.6 W
Junction Temperature @70°C (Θ_{JA} = 25°C/W) . . . . . 95°C
Maximum Solder Temperature .063″ (1 59 mm) below the Seating Plane, t<5 sec . . . 260°C

Recommended Operating Conditions −20°C to +70°C

Parameter	Min.	Nom.	Max.	Units
V_{CC}, Supply Voltage	4.5	5.0	5.5	V
V_{IH}, Input Voltage High	2.7			V
V_{IL}, Input Voltage Low			0.8	V
Clock Fan Out(1)		8	15	Disp

Note 1 The number of displays that can be synchronized by one "master" display clock depends on how "clean" the line is The maximum can only be achieved in very "clean" electrical environments A buffer is required for larger systems or noisy environments

Optical Characteristics @25°C

Spectral Peak Wavelength . (HER) 630 nm typ. .(Green) 565 nm typ.
Viewing Angle, both axis (off normal axis) . . . . . ±75°
Active Display Size . . . . . 1.16″ square
Dot Size . . . . . 0.11″ diam.
Pitch (center to center dot spacing) . . . . . 0.15″
Time Averaged Luminous Intensity (100% bright) . . . . . 0 5 mcd/dot min 1 7 mcd/dot typ
Dot to Dot Intensity Matching Ratio . . . . 1.8:1.0 max
Display Average Intensity Matching Ratio (per bin) . . . . . 1.5:1 0 max.
Bin to Bin Matching Ratio (adjacent bin) . . . . 1.9:1 0 max.

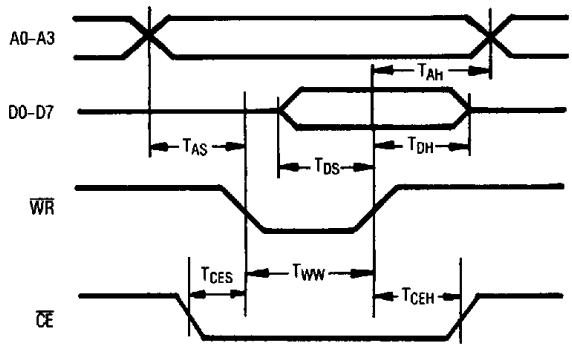
DC CHARACTERISTICS

Parameter	−20°C			+25°C			+70°C			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{CC} Blank		3.0	4.0		2.0	3.0		1 0	2.0	mA	$\overline{WR}$ = V_{CC} = 5.0 V, V_{IN} = 0 8 V
I_{CC} Lamp Test		115	130		105	115		95	105	mA	V_{CC} = 5.0 V
I_{CC} 64 dots on at full intensity(1, 2)		235	265		205	230		185	200	mA	V_{CC} = 5 0 V
I_{IL}		12	24		10	20		8	16	μA	V_{CC} = 5 0 V
V_{IH}	2.7			2 7			2.7			V	4.5 V ≤ V_{CC} ≤ 5.5 V
V_{IL}			0.8			0 8			0.8	V	4.5 V ≤ V_{CC} ≤ 5.5 V

Notes 1. Average LED drive current is 3 mA Peak current at ⅛ duty cycle is typically 25 mA
2 RDIM can be used to reduce I_{CC} and subsequently lower the nominal display intensity level See figure (2) for typical brightness reductions with the use of R_{EXT}

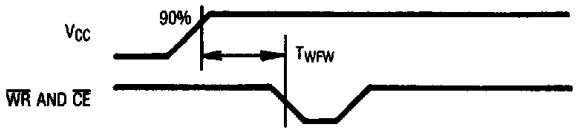
PD 1165

WRITE CYCLE

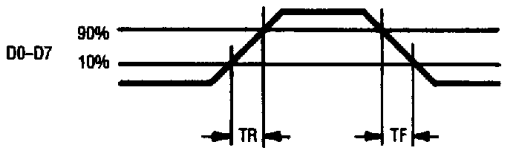


RESET TIMING

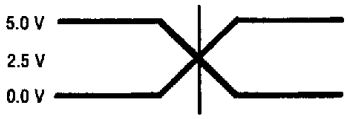
POWER ON TO FIRST WRITE TIMING



DATA BUS TRANSITIONS AT CL = 150 pF



TIMING MEASUREMENT LEVELS



AC CHARACTERISTICS Over Operating Temperature Range at V_{CC} = 4.5 V

Parameter	Symbol	−20°C (t_{MIN})	+25°C (t_{MIN})	+70°C (t_{MIN})	Units
Chip Enable Set Up Time	T_{CES}	0	5	5	ns
Address Set Up Time	T_{AS}	10	10	10	ns
Write Pulse Width	T_{WW}	20	30	30	ns(2)
Data Set Up Time	T_{DS}	40	55	55	ns(2)
Chip Enable Hold Time	T_{CEH}	0	0	0	ns
Address Hold Time	T_{AH}	5	5	5	ns
Data Hold Time	T_{DH}	20	20	20	ns
Reset Pulse Width	T_{REW}	50	50	50	µs(1)
Minimum Time Between Power Up and the First Write Operation	T_{WFW}	2	2	2	ms
Total Write Time ($T_{AS}+T_{WW}+T_{DH}$)	T_{WR}	35	45	45	ns

Notes 1 50 µs or 2 clock cycles minimum The internal clock frequency is between 50 and 80 kHz. If an external clock is supplied, it should be held between 50 and 60 kHz
2 T_{WW} must be less than T_{DS}

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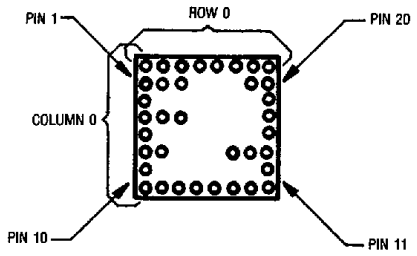
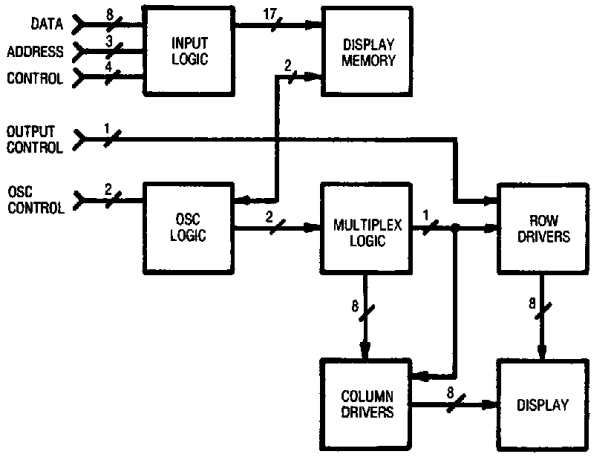
TOP VIEW



PD 1165, PD 1167 PINOUT			
1	$\overline{RST}$	20	GND
2	CLK OUT	19	D7
3	$\overline{WR}$	18	D6
4	$\overline{CE}$	17	D5
5	A0	16	D4
6	A1	15	D3
7	A2	14	D2
8	A3	13	D1
9	CLK IN	12	D0
10	R DIM	11	V_{CC}

PD 1165 (PD 1167) BLOCK DIAGRAM



PIN DEFINITIONS

Pin		
1.	$\overline{RST}$	Resets the System Active low.
2.	CLK_{OUT}	Clock output for daisy chaining
3.	$\overline{WR}$	Writes data into the display. Active low.
4.	$\overline{CE}$	Chip Enable. Active low.
5.	A0	Address Input (LSB)
6.	A1	Address Input
7	A2	Address Input (MSB)
8.	A3	Address Input for control words.
9.	CLK_{IN}	Clock Input for daisy chaining
10	R_{DIM}	Controls Brightness through R_{EXT}
11.	V_{CC}	Plus 5 volts power pin
12.	D0	Data Bus Bit 0 (LSB)
13.	D1	Data Bus Bit 1
14.	D2	Data Bus Bit 2
15.	D3	Data Bus Bit 3
16.	D4	Data Bus Bit 4
17.	D5	Data Bus Bit 5
18.	D6	Data Bus Bit 6
19	D7	Data Bus Bit 7 (MSB)
20.	GND	Ground

FUNCTIONAL DESCRIPTION

The PD 1165 (PD 1167) block diagram includes the major blocks and internal registers.

Display Memory consists of a 8×8 bit RAM block for the display columns and rows. Each one of the eight bit correspond to a LED and each eight bit cluster corresponds to a column It also contains a 1×8 bit block to serve as Control Word Register.

The **Input Logic** consists of Data Buffers, Control Logic and Address Decode Logic.

The **Oscillator (OSC) Logic** generates clock for internal and external use Reset function is a part of this block.

The **Multiplex Logic** generates multiplex scheme for column and row drivers, intensity control and blinking.

The **Row Drivers** drive 8 rows of eight LEDs each. The row drive currents could be trimmed using an external resistor (R_{DIM}) to set the nominal display brightness.

The **Column Drivers** drive 8 columns of eight LEDs each.

The **Display** consists of 64 LEDs connected in clusters of 8 to form columns and rows.

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USING THE PD 1165 (PD 1167)

POWER ON AND RESET

Each PD 1165 (PD 1167) series part is equivalent to a miniaturized hybrid display system. Careful consideration of power supply capabilities and applications should always be exercised. It is important that $GND \leq V_{IN} < (V_{CC} + 0.5\ V)$ always be maintained during use.

POWER SUPPLY REQUIREMENTS

A 5 volt power supply with no more than 10% tolerance should be used. Each display, depending on programming can switch very large loads. To keep transients on V_{CC} above ($V_{IN} - 0.5$ V), a 0.01 μF mica capacitor and a 22 μF tantalum capacitor should be located as close as conveniently possible to the V_{CC} and GND pins.(1)

To avoid malfunction during Power Up and Power Down, follow the sequences listed below.

POWER UP SEQUENCE

1. Float (tri-state) all display inputs.
2. Apply V_{CC} and GND to the display.
3. Activate inputs as required enabling the display (Observe T_{WRW} restrictions.)

POWER DOWN SEQUENCE

1. Float (tri-state) all active input signals to the display.
2. Turn off power to the display.

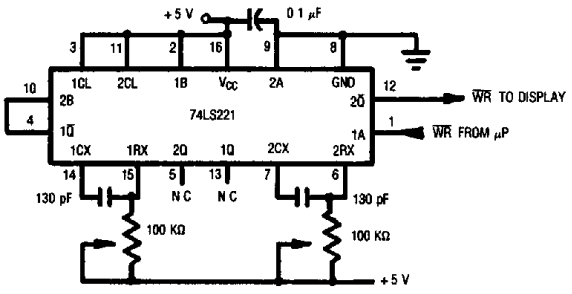
Once the display is powered up or following a hard reset using (RST), the display will initialize in a blinking lamp test control state. All LEDs will be on at 50% intensity blinking at about 2 Hz. Software control words can then be input initializing the displays configuring them for intensity and blinking attributes as well as clock control and timing synchronization.

SIGNAL CONDITIONING/INPUT BUFFERING

If cable lengths of 18 inches or more are used between the microprocessor and displays, the inputs should be buffered with tri-state non-inverting buffers. The buffers should be mounted as close to the displays as practical. Suggested buffers are the 74HCT244 or 74HC541.

The PD 1165 (PD 1167) accepts programming on the falling edge of the write pulse ($\overline{WR}$). Interfacing the displays to microprocessors that write on the rising edge (such as the 8035) will require the pulse from the microprocessor to be delayed. A dual one-shot circuit such as the one illustrated in figure (1) below is recommended.

FIGURE 1. WRITE DELAY CIRCUIT FOR μP's THAT WRITE ON RISING EDGE OF $\overline{WR}$



PROGRAMMING THE PD 1165 (PD 1167)

As described earlier, each display has 1 byte of RAM for a control word and 8 bytes for the display state of each LED.(2)

ADDRESSING LEDs AND CONTROL WORDS

Addressing the LEDs is managed through the A0-A2 address lines and D0-D7 data lines. Each data line corresponds to an LED row location with the address lines identifying a binary representation for the LED columns. The control word RAM address is identified by A3. $\overline{WR}$ and $\overline{CE}$ must also be low to input valid data.

Address State				Location
A3	A2	A1	A0	
0	0	0	0	First Column
0	0	0	1	Second Column
0	0	1	0	Third Column
0	0	1	1	Fourth Column
0	1	0	0	Fifth Column
0	1	0	1	Sixth Column
0	1	1	0	Seventh Column
0	1	1	1	Eighth Column
1	0	0	0	Control Word

When the appropriate column is addressed, a specific LED can be "written" on or off by identifying the appropriate row. Some examples are.

D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	0	0	0	0	0	1	1st Row On
0	0	1	0	0	0	0	0	6th Row On
0	0	0	1	0	0	0	1	1st & 5th Rows On

High Signals turn on LEDs, low turn off LEDs. Patterns remain until re-written or cleared.

CONTROL WORD OPERATION

When address bit A3 is taken high, the control word RAM is accessed. The same control word appears at all eight LED address locations of the display. These words determine display functions such as clearing, blanking, blinking, brightness to nine levels, selecting internal or external clock sources, resetting timing for synchronizing blinking and implementing a lamp test. These instructions are implemented in the following manner.

Brightness (D0-D2, RDIM): Display intensity must be set at one of the following levels. Increments of 12.5% are possible.

D7	D6	D5	D4	D3	D2	D1	D0	Intensity Level
X	X	X	X	X	0	0	0	12.5%
X	X	X	X	X	0	0	1	25.0%
X	X	X	X	X	0	1	0	37.5%
X	X	X	X	X	0	1	1	50.0%
X	X	X	X	X	1	0	0	62.5%
X	X	X	X	X	1	0	1	75.0%
X	X	X	X	X	1	1	0	87.5%
X	X	X	X	X	1	1	1	100.0%

Note 1 The device heatsink is tied to V_{CC}. It should be electrically insulated from all data and ground lines

Note 2 0=Low 1=High, X=Don't Care, $=appropriate intensity code.

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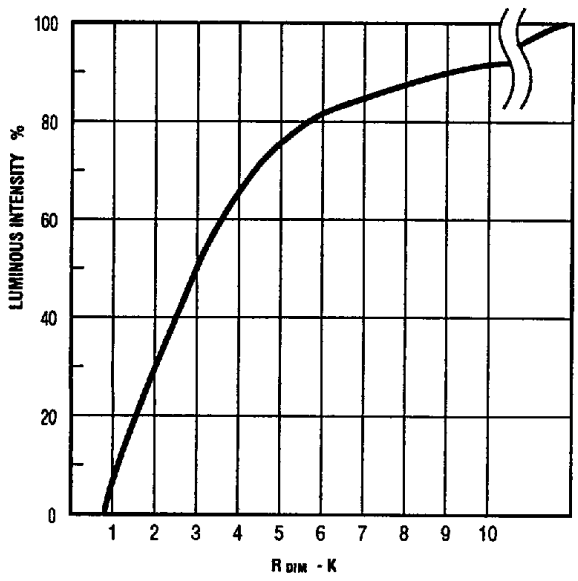
These intensity levels are proportional to the total display brightness. Each device is intensity categorized, however, this maximum brightness category can be lowered through an external resistor See figure (2) for the characteristic relationship of intensity to R_{EXT}. A 4K resistor would be equivalent to one intensity category shift.

Figure 2. Luminous Intensity vs. R_{DIM}



Display Blank (D3): The D3 bit will visually clear the display, blank it, without affecting the display RAM LED pattern.(1)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	X	X	X	1	$	$	$	Blank

Note 1 Although it is not recommended, the display can be dimmed by strobing the blank instruction on and off If this is done, frequencies of 1 KHz or more should be utilized to avoid flickering

Clock Select (D4): The appropriate clock selection should be included in the control word. For multiple display systems, external synchronized clocks should be used when blinking is required for uniform display appearance. One display can act as a master clock for up to 15 other displays provided the D4 bit is properly set.

D7	D6	D5	D4	D3	D2	D1	D0	Operation
X	X	X	0	X	$	$	$	Internal Clock
X	X	X	1	X	$	$	$	External Clock

Blink Control D5

D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	X	1	X	0	$	$	$	Blink Display at 2 Hz

Lamp Test D6, D2, D1, D0
The lamp test is only functional with the intensity level set to 50%. This does not affect display RAM.

D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	1	X	X	0	0	1	1	Turn all LEDs on at 50% brightness

Memory Clear D7, D6

D7	D6	D5	D4	D3	D2	D1	D0	Operation
1	0	X	X	X	$	$	$	Clear Display RAM, turn off LEDs

Reset Timing D7, D6
Timing reset is necessary for synchronizing display blinking for multiple display systems. It has no effect on display RAM.

D7	D6	D5	D4	D3	D2	D1	D0	Operation
1	1	X	X	X	$	$	$	Internal Timing Reset

DESIGN CONSIDERATIONS

MULTIPLE DISPLAY SYSTEMS

The PD 1165 (PD 1167) parts may be cascaded for flat panel displays of any size. If blinking is to be used, up to 15 displays can be synchronized to one "master" display clock as described earlier. Additional displays will require a buffer to drive the clock load.

The connection scheme is straight forward as illustrated in figure (3) below.

1 Buss together: Data lines, Address lines, Write Enable lines, Reset lines, V_{CC} (with proper capacitors for power supply conditioning) and GND lines.
2. Terminate the Data, Address and Write lines of the "master" display to the microprocessor interface
3. Terminate the CE lines of the "slave" displays to the appropriate microprocessor address decoders.
4 Connect the clock out (pin 2) of the "master" display to the buffer for/or clock in (pin 9), of the "slave" displays.

This flat panel sub assembly can then be interfaced easily with microprocessors, such as the 8035, as illustrated in figure (4) below.

For systems with synchronized blinking, an initializing control softword reset should precede the instructions for clearing, brightness, clock selection, etc.

INTENSITY MATCHING

For best matching, displays from one bin should be used. It is often acceptable, under normal viewing conditions, to use displays from two neighboring bins. The RDIM connection allows users to set intensity levels to match displays of all intensity levels.

ESD PROTECTION

The silicon gate CMOS IC of the PD 1165 (PD 1167) is sensitive to ESD damage Users of these devices are encouraged to take all the standard precautions, normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. Where these conditions are not or cannot be met, keep the leads of the device shorted together or the parts in anti-static packaging.

SOLDERING CONSIDERATIONS

The PD 1165 (PD 1167) can be hand soldered with SN63 solder using a grounded iron set to 260°C

Wave soldering is also possible following these conditions. Preheat that does not exceed 93°C on the solder side of the PC board or a package surface temperature of 70°C. Water soluble organic acid flux or resin-based RMA flux can be used.

Wave temperature of 245°C ±5°C with a dwell between 1 5 sec. to 3.0 sec. Exposure to the wave should not exceed temperatures above 260°C, for 5 seconds at 0.063" below the seating plane. The packages should not be immersed in the wave.

POST SOLDER CLEANING PROCEDURES

The least offensive cleaning solution is hot D I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Care should be exercised in choosing these as some may chemically attack the polycarbonate package. Maximum exposure should not exceed two minutes at elevated temperatures. Acceptable solvents are TF (trichlorotrifluoroethane), TP35, TMS+, TE, and Isopropyl Alcohol.

Unacceptable solvents contain TCM, TMC, TA, TES, Acetone, and III Trichloroethane Since many commercial mixtures exist, you should contact your preferred solvent vendor for chemical composition information. Some major solvent manufacturers are: Allied Chemical Corporation, Specialty Chemical Division, Morristown, NJ; Baron-Blakeslee, Chicago, IL; Dow Chemical, Midland, MI; E.I. DuPont de Nemours & Co., Wilmington, DE.

For further information refer to Appnotes 18 and 19 in the current Siemens Optoelectronic Data Book.

An alternative to soldering and cleaning the display modules is to use sockets. Naturally, 20 pin DIP sockets .600" wide with .100" centers work well for single displays. Multiple display assemblies are best handled by longer SIP sockets or DIP sockets when available for uniform package alignment. Socket manufacturers are Aries Electronics, Inc., Frenchtown, NJ; Garry Manufacturing, New Brunswick, NJ; Robinson-Nugent, New Albany, IN; and Samtec Electronic Hardware, New Albany, IN.

For further information refer to Appnote 22 in the current Siemens Optoelectronic Data Book

FIGURE 3. GENERAL INTERFACE CIRCUIT

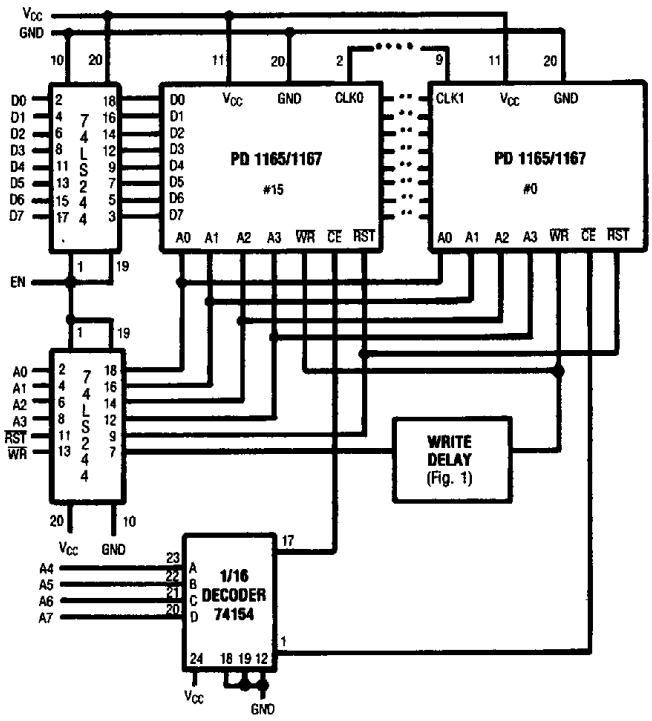


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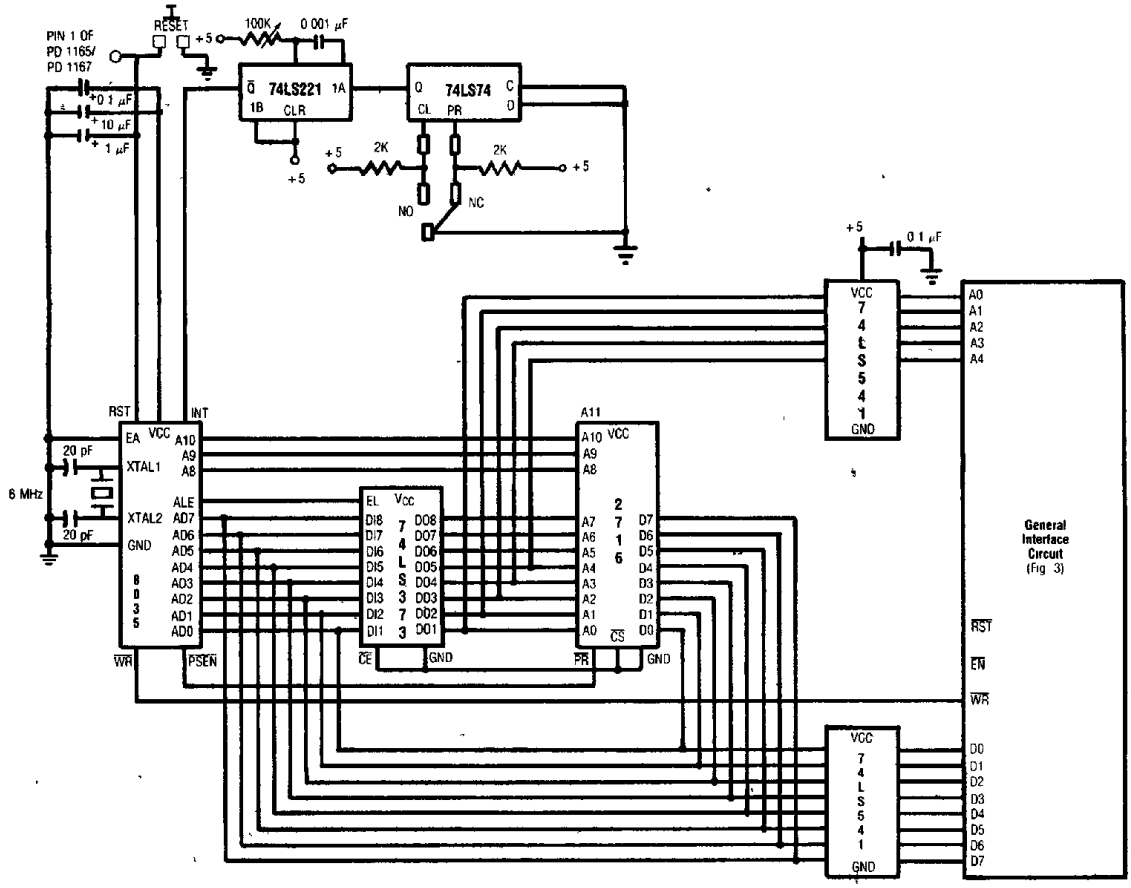
FIGURE 4. MICROPROCESSOR INTERFACE CIRCUIT



OPTICAL CONSIDERATIONS

The 1.19" high character of the PD 1165 (PD 1167) allows readability up to 35 feet. Proper filter selection will allow the user to build a display that can be utilized over this distance.

Filters enhance the contrast ratio between a lit LED and the character background. The only limitation is cost The cost/benefit ratio for filters can be maximized by first considering the ambient lighting environment

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are inexpensive and effective in optimizing contrast ratios. The PD 1165 is a high efficiency red display and should be matched with a long wavelength pass filter in the 570 nm to 590 nm range. The PD 1167 should be matched with a yellow-green band-pass filter that peaks at 565 nm. For display systems of multiple colors (using other Siemens displays), neutral density grey filters offer the best compromise.

Additional contrast enhancement can be gained through shading the displays. Plastic band-pass filters with built-in louvers offer the "next step up" in contrast improvement Also, plastic filters can be further improved with anti-reflective coatings to reduce glare. The trade-off is "fuzzy" characters. Mounting the filters close to the display reduces this effect. Care should be taken not to overheat the plastic filters by allowing for proper air flow.

Optimal filter enhancements for any condition can be gained through the use of circular polarized, anti-reflective, band-pass filters. The circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1%.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homelite, Wilmington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY; Hoya Optics, Inc., Fremont, CA.

One final note on mounting filters. Recessing display and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several Bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E.-Atlas, Van Nuys, CA

Refer to Siemens Appnote 23 for further information.

REPLACEMENT

Should a display nested within a panel be damaged, replacement can be made by trimming the tabs off the neighboring displays adjacent to the damaged displays Row # 0 and Column # 0 (typically above and to the left). Once the interlocking tabs are trimmed (using a razor blade-type cut), the damaged device may be removed and replaced