DATA SHEET

PCF8562
Universal LCD driver for low multiplex rates

Preliminary Specification

November 22, 2004

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, $^1/_2$ and $^1/_3$
- Internal LCD bias generation with voltage-follower buffers
- 32 segment drives: up to sixteen 8-segment numeric characters; up to eight 15-segment alphanumeric characters; or any graphics of up to 128 elements
- 32 × 4-bit RAM for display data storage
- Auto-incremental display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 to 5.5 V
- Wide logic LCD supply range: from 2.5 V for low-threshold LCDs and up to 6.5 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- TTL/CMOS compatible
- Compatible with 4, 8 or 16-bit microprocessors or microcontrollers
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8562 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 32 segments. The PCF8562 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8562TT	TSSOP48	plastic, 48 leads; body	SOT362-1

4 BLOCK DIAGRAM

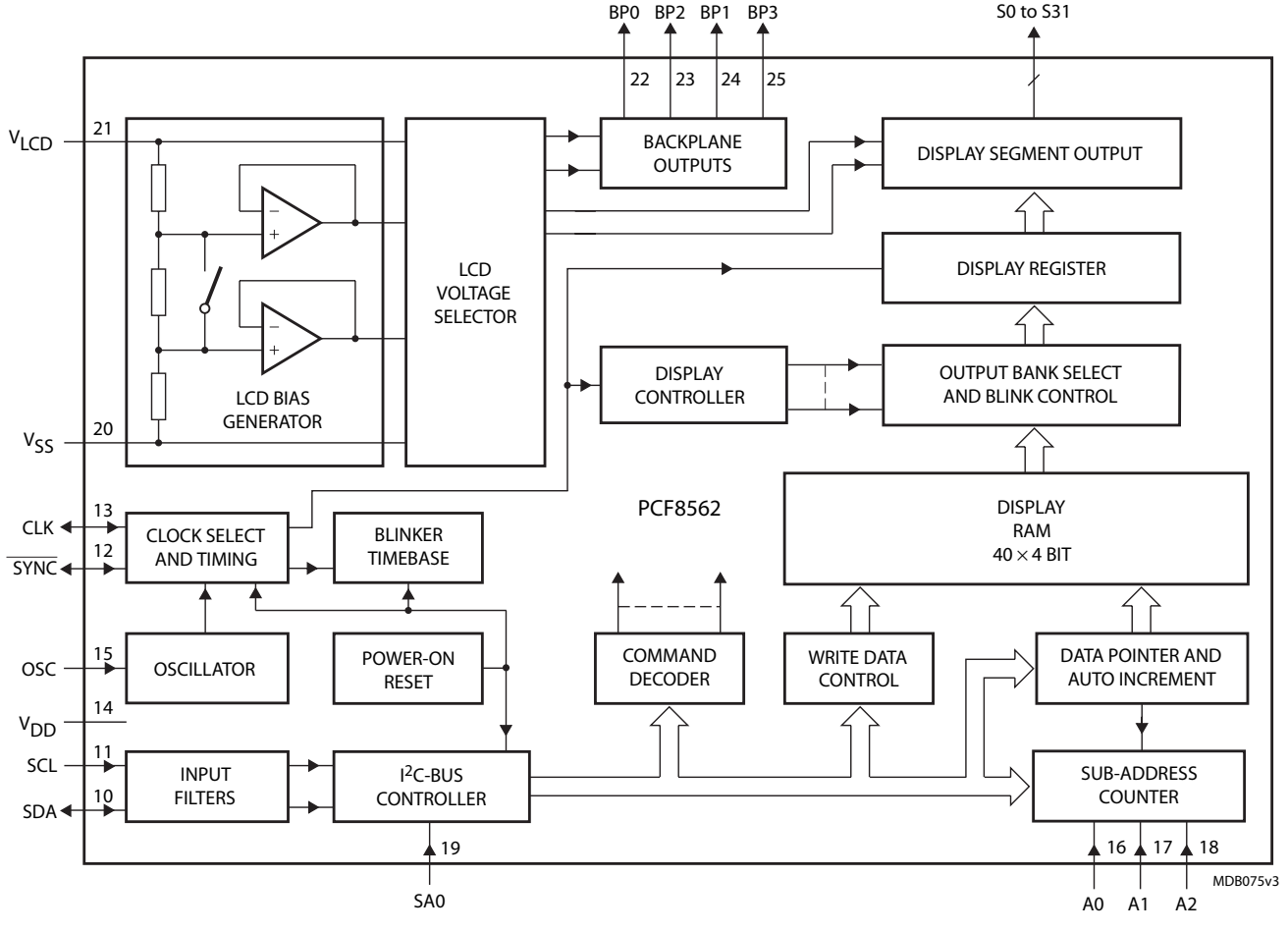


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
	PCF8562TT	
SDA	10	I^2C-bus serial data Input / Output
SCL	11	I^2C-bus serial clock input
CLK	13	external clock input / output
V_{DD}	14	supply voltage
$\overline{SYNC}$	12	cascade synchronisation input / output
OSC	15	internal oscillator enable input
A0 to A2	16 to 18	sub address inputs
SAO	19	I^2C-bus slave address input: bit 0
V_{SS}	20	logic ground
V_{LCD}	21	LCD supply voltage
BP0 to BP3	22 to 25	LCD backplane outputs
S0 to S22	26 to 48	LCD segments output
S23 to S31	1 to 9	

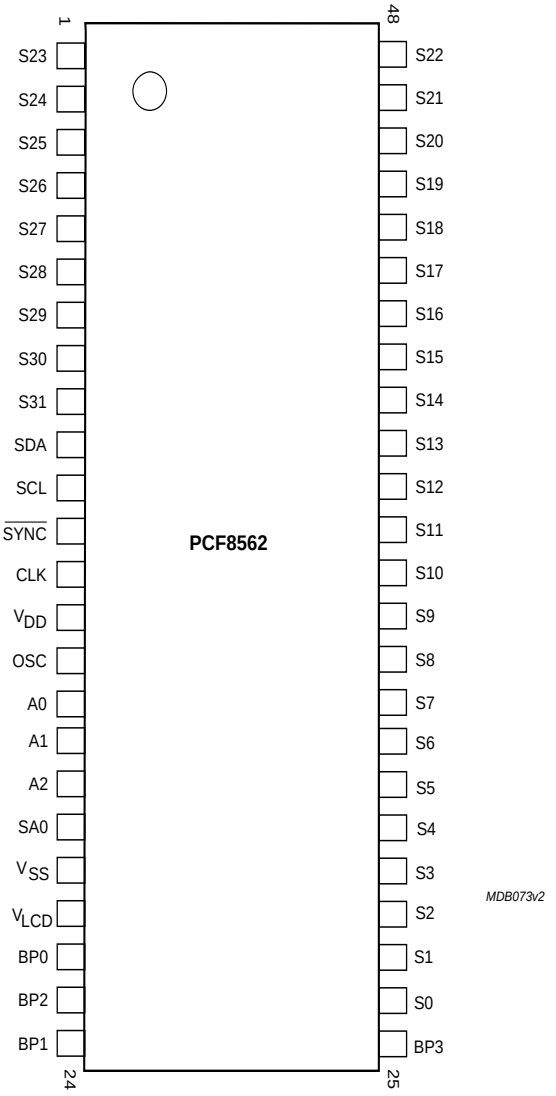


Fig.2 Pin Configuration (TSSOP48)

6 FUNCTIONAL DESCRIPTION

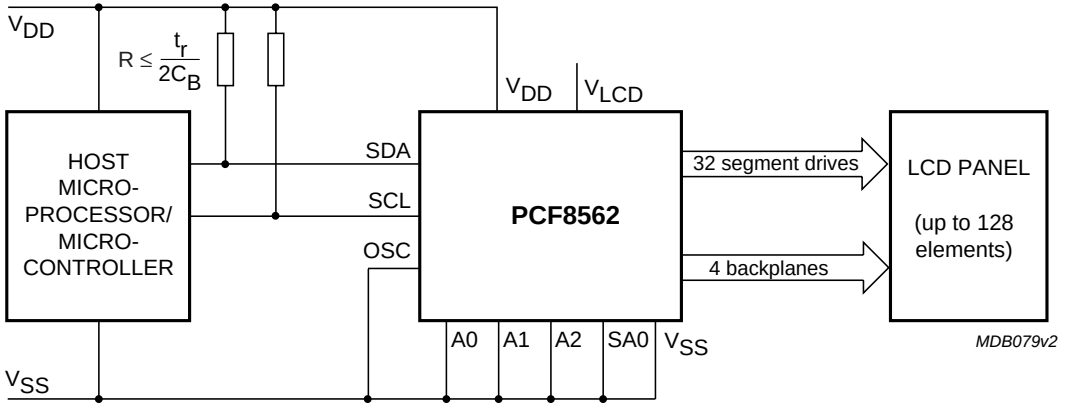
The PCF8562 is a versatile peripheral device designed to interface any microprocessor/microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 32 segments.

The display configurations possible with the PCF8562 depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 1; all of these configurations can be implemented in the typical system shown in Fig.4.

The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8562. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	128	16	16	8	16	128 dots (4 × 32)
3	86	12	12	6	12	96 dots (3 × 32)
2	64	8	8	4	8	64 dots (2 × 32)
1	32	4	4	2	4	32 dots (1 × 32)



The resistance of the power supply lines must be kept to a minimum.

Fig.4 Typical system configuration.

6.1 Power-on reset

At power-on the PCF8562 resets to the following starting conditions:

- All backplane outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- Drive mode '1 : 4 multiplex with ⅓bias' is selected
- Blinking is switched off
- Input and output bank selectors are reset (as defined in Table 4)
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared
- Display is disabled.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three resistors connected in series between V_{LCD} and V_{SS}. The middle resistor can be bypassed to provide a ½bias voltage level for the 1 : 2 multiplex configuration. The LCD voltage can be temperature compensated externally via the supply to pin V_{LCD}.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting Discrimination ratios (D), are given in Table 2.

A practical value for V_{LCD} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1 : 3 and 1 : 4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

6.3.1 LCD BIAS FORMULAE

Bias is calculated by the formula $\frac{1}{1+a}$

where for ½ bias, a = 1; for ⅓ bias, a = 2.

The LCD on voltage (V_{on}) is calculated by the formula $V_{op}\sqrt{\frac{\frac{1}{N}+\left[(N-1)\cdot\left(\frac{1}{1+a}\right)\right]^2}{N}}$

The LCD off voltage (V_{off}) is calculated by the formula $V_{op}\sqrt{\frac{a^2-(2a+N)}{N\cdot(1+a)^2}}$

where V_{op} is the resultant voltage at the LCD segment; N is the LCD drive mode: 1 = static, 2 = 1 : 2, 3 = 1 : 3, 4 = 1 : 4.

Discrimination is the ratio of V_{on} to V_{off}, and is determined by the formula $\frac{V_{on}}{V_{off}} = \sqrt{\frac{(a+1)^2 + (N-1)}{(a-1)^2 + (N-1)}}$

Using the above formula, the discrimination for an LCD drive mode of 1 : 3 with ½bias is $\sqrt{3}$ = 1.732, and the discrimination for an LCD drive mode of 1 : 4 with ½bias is $\frac{\sqrt{21}}{3}$ = 1.528.

The advantage of these LCD drive modes is a reduction of the LCD full-scale voltage V_{LCD} as follows:

- 1 : 3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(rms)} = 2.449\ V_{off(rms)}$
- 1 : 4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309\ V_{off(rms)}$

These compare with $V_{LCD} = 3\ V_{off(rms)}$ when ⅓ bias is used.

Table 2 Discrimination ratios

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{lcd}}$	$\frac{V_{on(rms)}}{V_{lcd}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2 multiplex	2	3	½	0.354	0.791	2.236
1 : 2 multiplex	2	4	⅓	0.333	0.745	2.236
1 : 3 multiplex	3	4	⅓	0.333	0.638	1.915
1 : 4 multiplex	4	4	⅓	0.333	0.577	1.732

6.4 LCD drive mode waveforms

6.4.1 STATIC DRIVE MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (S_n) waveforms for this mode are shown in Fig.5.

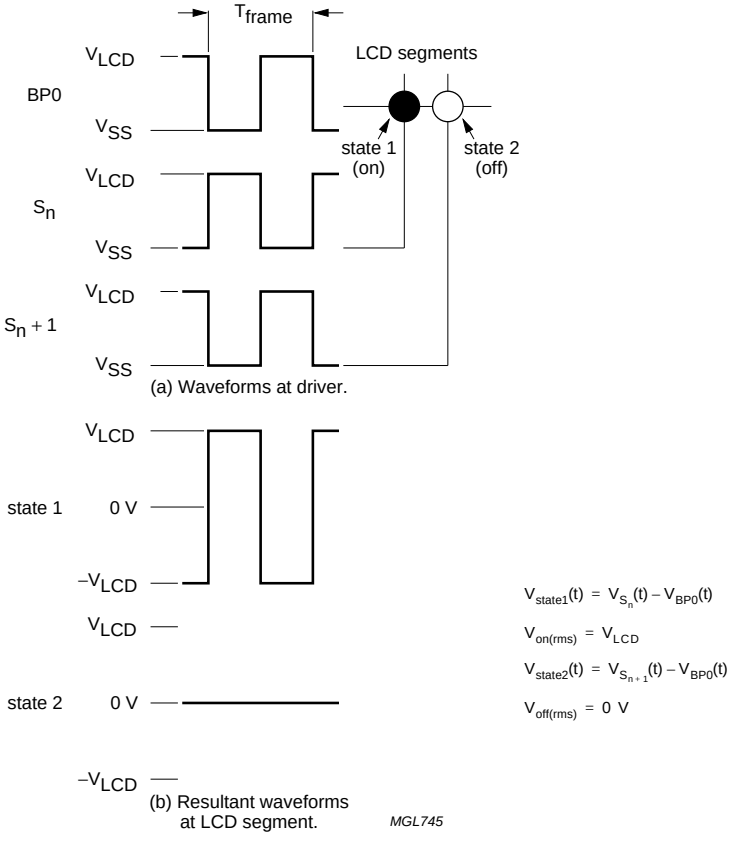
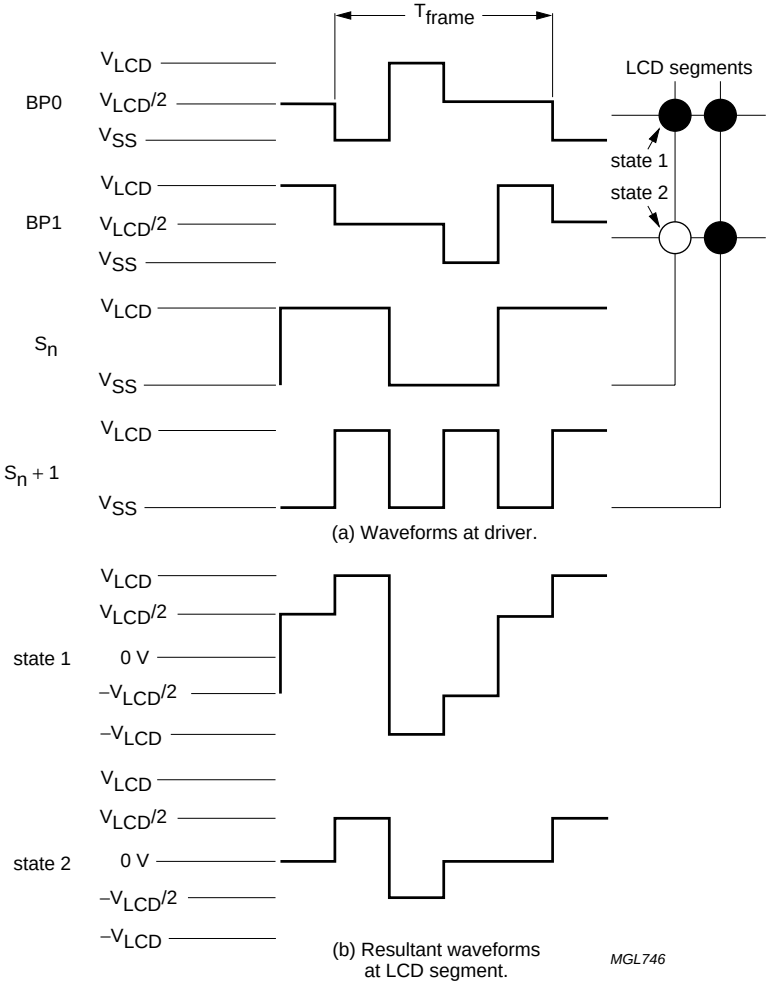


Fig.5 Static drive mode waveforms.

6.4.2 1 : 2 MULTIPLEX DRIVE MODE

The 1 : 2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½bias or ⅓bias as shown in Figs 6 and 7.



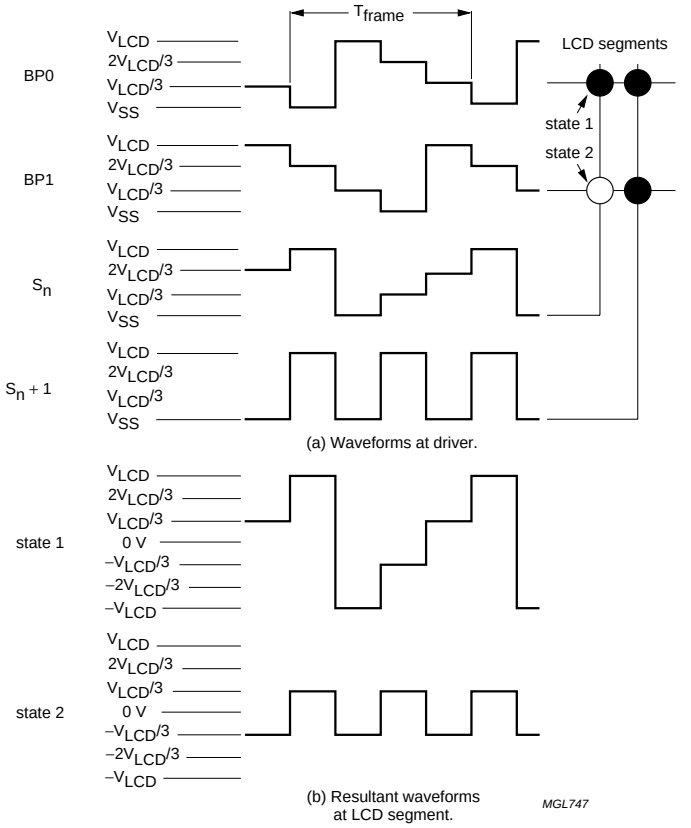
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.791 V_{LCD}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.354 V_{LCD}$

Fig.6 Waveforms for the 1 : 2 multiplex drive mode with ½ bias.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.745V_{LCD}$

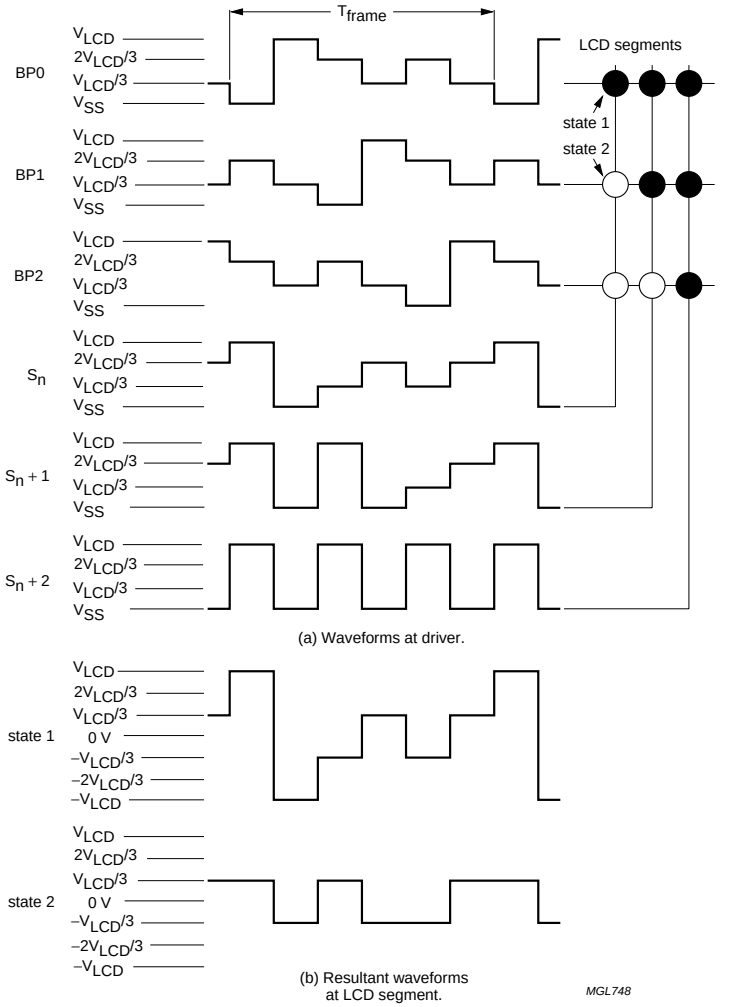
$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{LCD}$

Fig.7 Waveforms for the 1 : 2 multiplex drive mode with $\frac{1}{3}$ bias.

6.4.3 1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies (see Fig.8).



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0{\cdot}638V_{LCD}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{LCD}$

Fig.8 Waveforms for the 1 : 3 multiplex drive mode.

6.4.4 1 : 4 MULTIPLEX DRIVE MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies (see Fig.9).

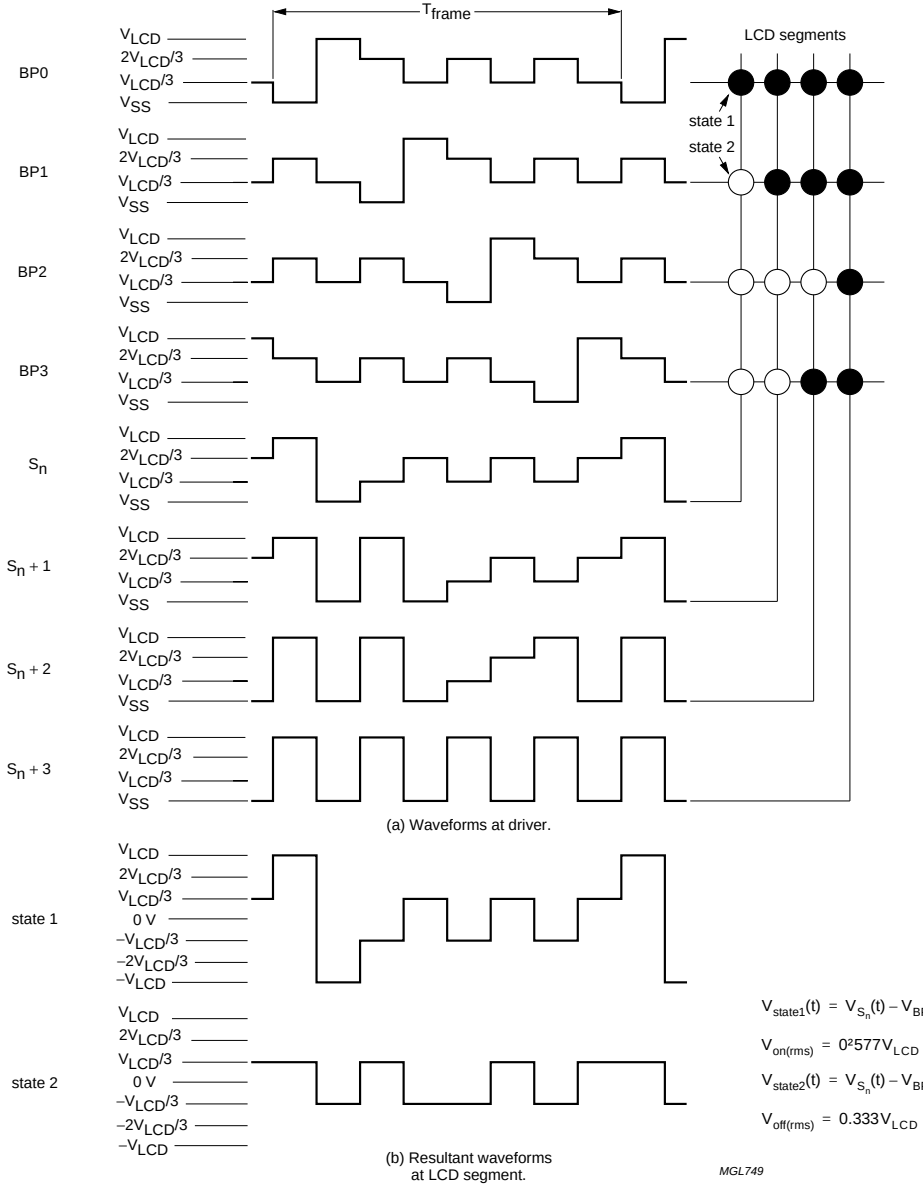


Fig.9 Waveforms for the 1 : 4 multiplex drive mode.

6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic of the PCF8562 and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. After power-up, pin SDA must be HIGH to guarantee that the clock starts.

6.5.2 EXTERNAL CLOCK

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

The LCD frame signal frequency is determined by the clock frequency (f_{CLK}).

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The PCF8562 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division integer of the clock frequency (nominally 64 kHz) from either the internal or an external clock.

Frame frequency = $\frac{f_{CLK}}{24}$

6.7 Display register

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and each column of the display RAM.

6.8 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display latch. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

6.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode, BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.10 Display RAM

The display RAM is a static 32 $\times$ 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on-state of the corresponding LCD segment; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 32 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8562, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. For example, in the 1 : 2 mode, the RAM data is stored every second bit. To illustrate the filling order, an example of a

7-segment numeric display showing all drive modes is given in Fig.10; the RAM filling organization depicted applies equally to other LCD types.

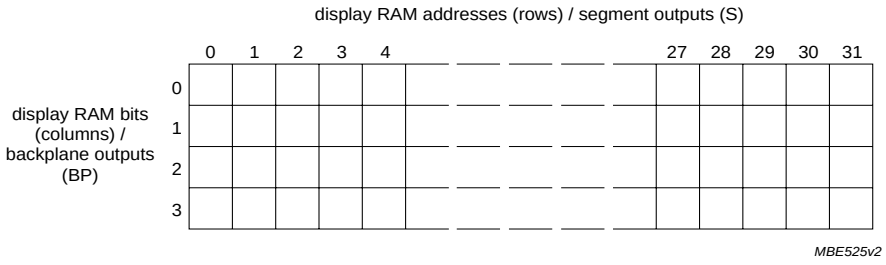


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs also between bits in a RAM word and the backplane outputs.

With reference to Fig.10, in the static drive mode, the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 mode, the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 mode, these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted.

In the 1 : 4 mode, the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

6.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored at the display RAM address indicated by the data pointer in accordance with the filling order shown in Fig.11. After each byte is stored, the contents of the data pointer are automatically incremented by a value dependent on the selected LCD drive mode: eight (static drive mode), four (1 : 2 mode), three (1 : 3 mode) or two (1 : 4 mode). If an I^2C-bus data access is terminated early then the state of the data pointer will be unknown. The data pointer should be re-written prior to further RAM accesses.

6.12 Device Select

Storage is allowed to take place when the internal select register agrees with the hardware subaddress applied to A0, A1 and A2.

The hardware subaddress should not be changed whilst the device is being accessed on the I^2C-bus interface.

6.13 Output bank selector

The output bank selector selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the selected LCD drive mode and on the instant in the multiplex sequence. In 1 : 4 mode, all RAM addresses of bit 0 are selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 mode, bits 0, 1 and 2 are selected sequentially. In 1 : 2 mode, bits 0 and 1 are selected and, in static mode, bit 0 is selected. Signal $\overline{\text{SYNC}}$ will reset these sequences to the following starting points; bit 3 for 1 : 4 mode, bit 2 for 1 : 3 mode, bit 1 for 1 : 2 mode and bit 0 for static mode.

The PCF8562 includes a RAM bank switching feature in the static and 1 : 2 drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1 : 2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This allows display information to be prepared in an alternative bank and then selected for display when it is assembled.

6.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. The BANK SELECT command can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 mode. The input bank selector functions are independent of the output bank selector.

6.15 Blinker

The PCF8562 has a very versatile display blinking capability. The whole display can blink at a frequency selected by the BLINK command. Each blink frequency is a multiple integer value of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected, as shown in Table 3.

An additional feature allows an arbitrary selection of LCD segments to be blinked in the static and 1 : 2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the BLINK command.

In the 1 : 3 and 1 : 4 drive modes, where no alternative RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

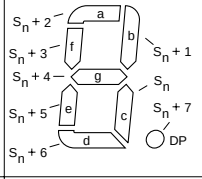
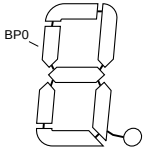
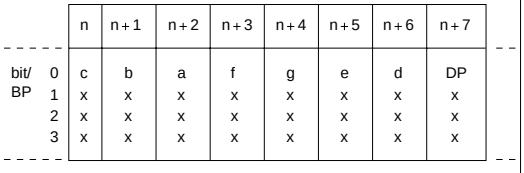
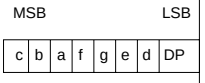
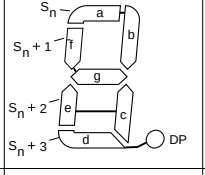
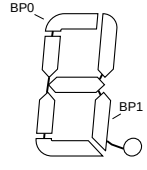
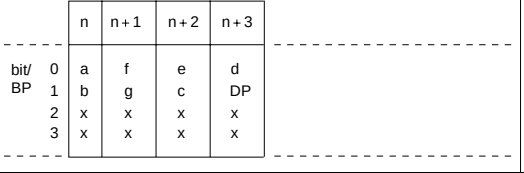
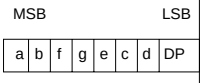
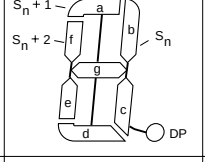
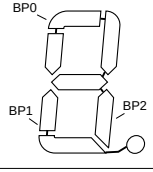
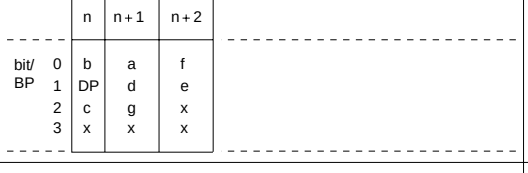
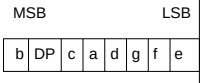
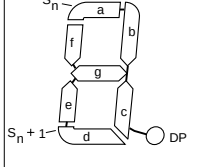
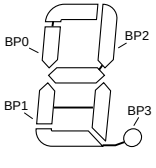
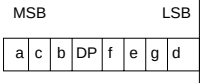
The entire display can be blinked at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 3 Blinking frequencies

BLINK MODE	NORMAL OPERATING MODE RATIO	NOMINAL BLINK FREQUENCY
Off	–	blinking off
2 Hz	$\frac{f_{CLK}}{768}$	2 Hz
1 Hz	$\frac{f_{CLK}}{1536}$	1 Hz
0.5 Hz	$\frac{f_{CLK}}{3072}$	0.5 Hz

Note

1. Blink modes 0.5, 1 and 2 Hz, and nominal blink frequencies 0.5, 1 and 2 Hz correspond to an oscillator frequency (f_{CLK}) of 1536 Hz at pin CLK. The oscillator frequency range is given in Chapter 11.

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

MGL751

x = data bit unchanged.

Fig.11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

In chip-on-glass applications where the track resistance from the SDA pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is therefore necessary to minimize the track resistance from the SDA pad to the system SDA line to guarantee a valid LOW-level during the acknowledge cycle.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Fig.12).

7.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P), (see Fig.13).

7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’, (see Fig.14).

7.4 Acknowledge

The number of data bytes that can be transferred from transmitter to receiver between the START and STOP conditions is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal on the bus that is asserted by the transmitter during which time the master generates an extra acknowledge related clock pulse. An addressed slave receiver must generate an acknowledge after receiving each byte. Also a master receiver must generate an acknowledge after receiving each byte that has been clocked out of the slave transmitter. The acknowledging device must pull-down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Fig.15).

7.5 PCF8562 I²C-bus controller

The PCF8562 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8562 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (01110000 and 01110010) are reserved for the PCF8562. The least significant bit of the slave address that a PCF8562 will respond to is defined by the level tied to its SA0 input. The PCF8562 is a write-only device and will not respond to a read access.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCF8562 slave addresses available. All PCF8562s whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF8562s whose SA0 inputs are set to the alternative level.

After an acknowledgement, one or more command bytes follow which define the status of the PCF8562.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see Fig.17). The command bytes are also acknowledged by all addressed PCF8562s on the bus.

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated.

An acknowledgement after each byte is asserted only by PCF8562s that are addressed via address lines A0, A1 and A2. After the last display byte, the I²C-bus master asserts a STOP condition (P). Alternately a START may be asserted to RESTART an I²C-bus access.

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position as shown in Fig.17. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8562 are defined in Table 4.

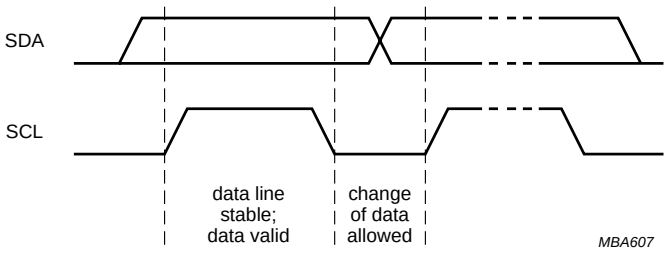


Fig.12 Bit transfer.

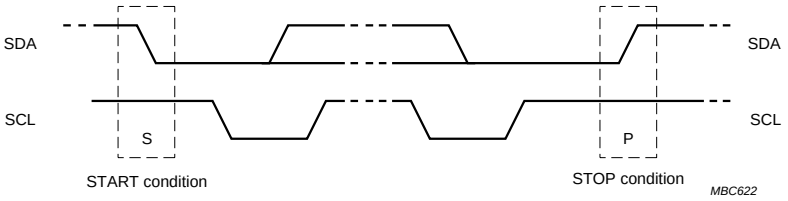


Fig.13 Definition of START and STOP conditions.

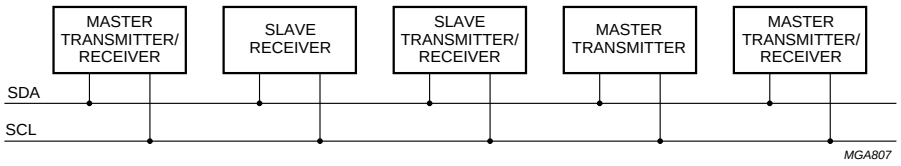


Fig.14 System configuration.

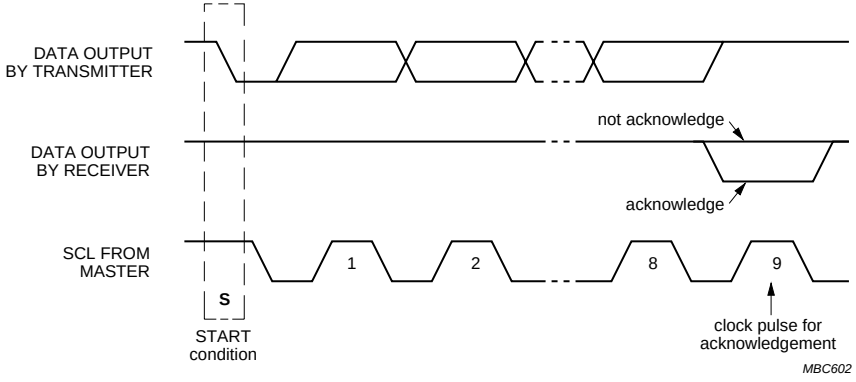


Fig.15 Acknowledgement on the I^2C-bus.

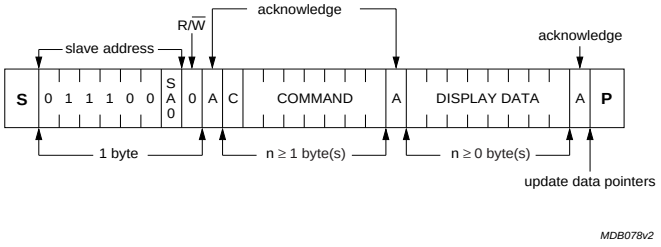
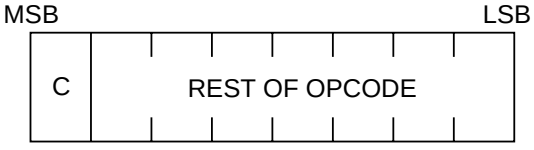


Fig.16 I^2C-bus protocol.



C = 0 = last command.
C = 1 = commands continue.

Fig.17 Format of command byte.

Table 4 Definition of PCF8562 commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
MODE SET	C	1	0	(1)	E	B	M1	M0	Table 5	Defines LCD drive mode.
									Table 6	Defines LCD bias configuration.
									Table 7	Defines display status; the possibility to disable the display allows implementation of blinking under external control.
LOAD DATA POINTER	C	0	P5	P4	P3	P2	P1	P0	Table 8	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of 32 display RAM addresses.
DEVICE SELECT	C	1	1	0	0	A2	A1	A0	Table 9	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses.
BANK SELECT	C	1	1	1	1	0	I	O	Table 10	Defines input bank selection (storage of arriving display data).
									Table 11	Defines output bank selection (retrieval of LCD display data); the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
BLINK	C	1	1	1	0	A	BF1	BF0	Table 12	Defines the blink frequency.
									Table 13	Selects the blink mode; normal operation with frequency set by BF1, BF0 or blinking by alternating display RAM banks; alternating RAM bank blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

Note

1. Not used.

Table 5 Mode set option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	**BACKPLANE**	**M1**	**M0**
Static	BP0	0	1
1 : 2	BP0, BP1	1	0
1 : 3	BP0, BP1, BP2	1	1
1 : 4	BP0, BP1, BP2, BP3	0	0

Table 6 Mode set option 2

LCD BIAS	BIT B
1⁄3bias	0
1⁄2bias	1

Table 7 Mode set option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 8 Load data pointer option 1

DESCRIPTION	BITS					
6 bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 9 Device select option 1

DESCRIPTION	BITS		
3 bit binary value of 0 to 7	A2	A1	A0

Table 10 Bank select option 1 (input)

MODE		BIT I
STATIC	**1 : 2**	
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 11 Bank select option 2 (output)

MODE		BIT O
STATIC	**1 : 2**	
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 12 Blink option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 13 Blink option 2

BLINK MODE	BIT A
Normal blinking	0
Alternate RAM bank blinking	1

Note

1. Normal blinking is assumed when LCD multiplex drive modes 1 : 3 or 1 : 4 are selected.

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and co-ordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

7.10 Multiple chip operation

For large display configurations please refer to the PCF8576D device.

Please refer to PCF8576D if you need to drive more segments (>128 elements).

Table 14 $\overline{\text{SYNC}}$ contact resistance

NUMBER OF DEVICES	MAXIMUM CONTACT RESISTANCE
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
10 to 16	700 Ω

The contact resistance between the $\overline{\text{SYNC}}$ input/output on each cascaded device must be controlled. If the resistance is too high, the device will not be able to synchronize properly; this is particularly applicable to chip-on-glass applications. The maximum $\overline{\text{SYNC}}$ contact resistance allowed for the number of devices in cascade is given in Table 14.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_{LCD}	LCD supply voltage	V_{SS} – 0.5	+7.5	V
V_{i1}	input voltage CLK, $\overline{\text{SYNC}}$, SA0, OSC, A0 to A2	V_{SS} – 0.5	V_{DD} + 0.5	V
V_{i2}	input voltage SCL and SDA	V_{SS} – 0.5	+6.5	V
V_O	output voltage S0 to S39, BP0 to BP3	V_{SS} – 0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}	V_{DD} current	–50	+50	mA
I_{SS}	V_{SS} current	–50	+50	mA
I_{LCD}	V_{LCD} current	–50	+50	mA
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

10 DC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	5.5	V
V_{LCD}	LCD supply voltage	note 1	2.5	–	6.5	V
I_{DD}	supply current	note 2; f_{CLK} = 1536 Hz	–	8	20	µA
I_{LCD}	LCD supply current	note 2; f_{CLK} = 1536 Hz	–	24	60	µA
Logic						
V_{IL}	LOW-level input voltage CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		$0.7V_{DD}$	–	V_{DD}	V
V_{IL2}	LOW-level input voltage SCL, SDA		V_{SS}	–	$0.3V_{DD}$	V
V_{IH2}	HIGH-level input voltage SCL, SDA	note 3	$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW-level output current CLK, $\overline{SYNC}$	V_{OL} = 0.4 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH-level output current CLK	V_{OH} = 4.6 V; V_{DD} = 5 V	−1	–	–	mA
I_{OL2}	LOW-level output current SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current CLK, SCL, SDA, A0 to A2 and SA0	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
I_{L2}	leakage current OSC	$V_I = V_{DD}$	−1	–	+1	µA
V_{POR}	power-on reset voltage level		1.0	1.3	1.6	V
C_I	input capacitance	note 4	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage tolerance BP0 to BP3		−100	–	+100	mV
V_S	DC voltage tolerance S0 to S31		−100	–	+100	mV
R_{BP}	output resistance BP0 to BP3	note 5; V_{LCD} = 5 V	–	1.5		kΩ
R_S	output resistance S0 to S31	note 5; V_{LCD} = 5 V	–	6.0		kΩ

Notes

1. V_{LCD} > 3 V for $\frac{1}{3}$bias.
2. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
3. When tested, I^2C pins SCL and SDA have no diode to V_{DD} and may be driven according to the V_{i2} limiting values given in Chapter 8. Also see Fig.21.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK}	oscillator frequency	note 1	960	1890	2640	Hz
t_{CLKH}	input CLK HIGH time		60	–	–	µs
t_{CLKL}	input CLK LOW time		60	–	–	µs
$t_{PD(\overline{SYNC})}$	SYNC propagation delay		–	30	–	ns
$t_{\overline{SYNC}L}$	SYNC LOW time		1	–	–	µs
$t_{PD(LCD)}$	driver delays with test loads	V_{LCD} = 5 V; note 2	–	–	30	µs
Timing characteristics: I²C-bus; note 3						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{BUF}	bus free time between a STOP and START		1.3	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Notes

1. Typical output duty factor: 50% measured at the CLK output pin.
2. Not tested in production.
3. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

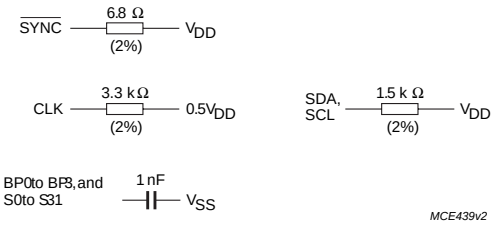


Fig.18 Test loads.

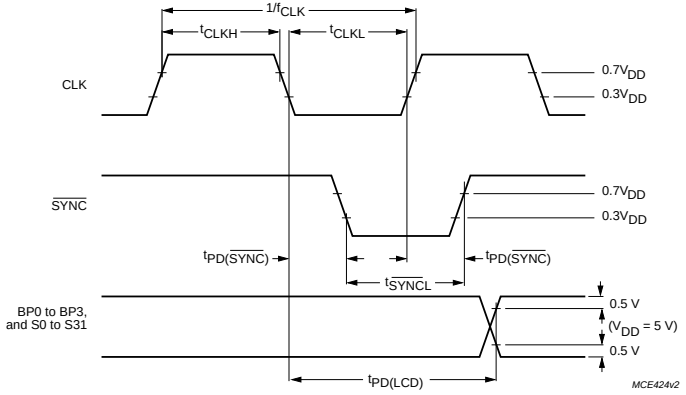


Fig.19 Driver timing waveforms.

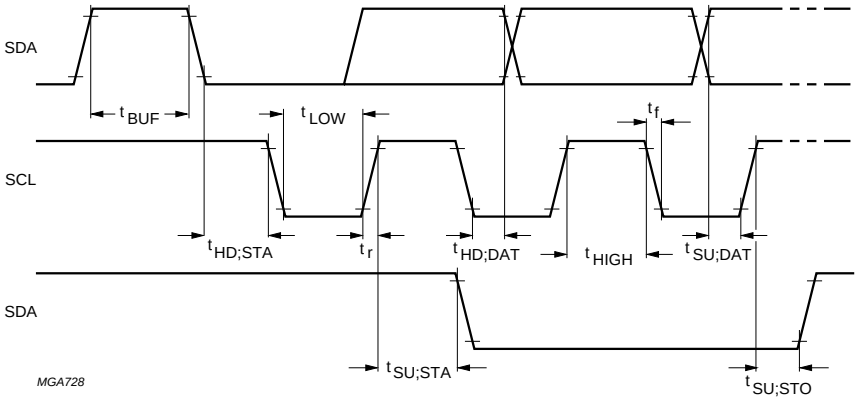


Fig.20 I²C-bus timing waveforms.

12 DEVICE PROTECTION

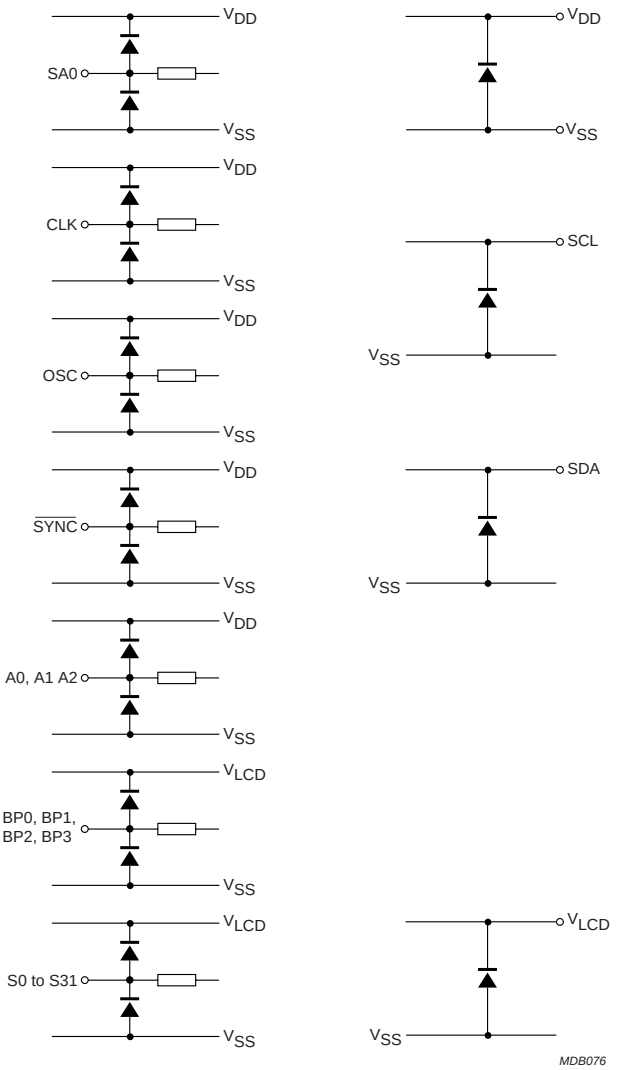
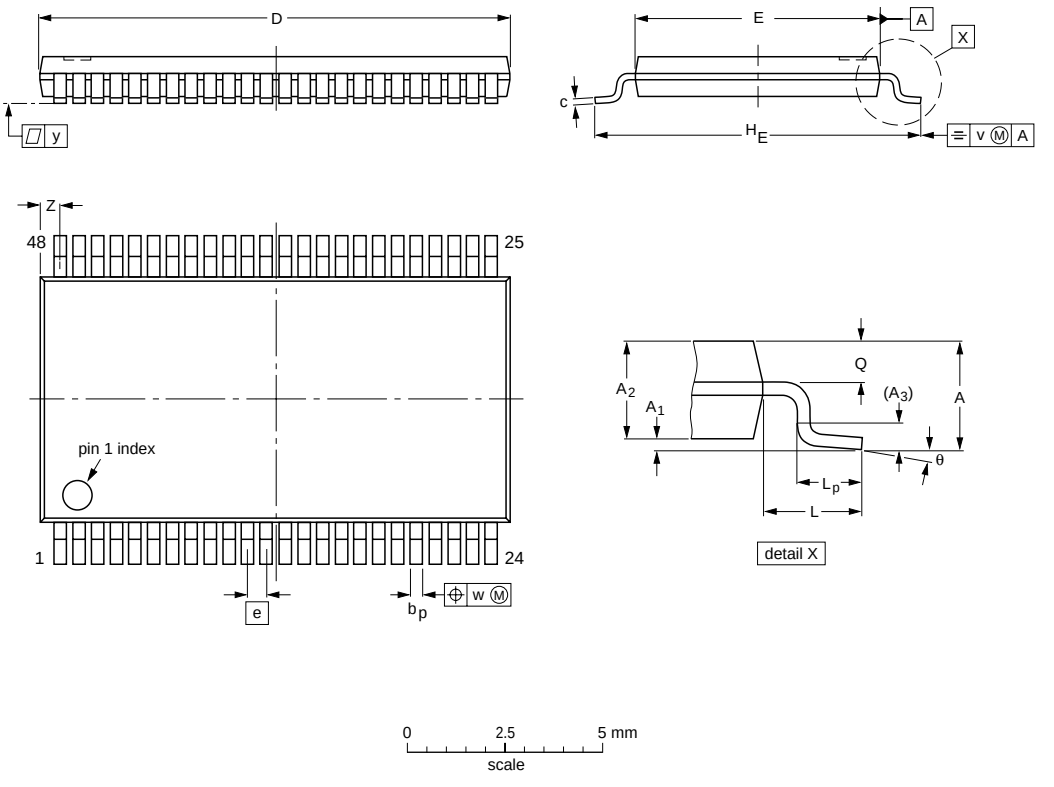


Fig.21 Device protection diagram.

13 PACKAGE OUTLINES

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness ≥Š 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE(1)	SOLDERING METHOD	
	WAVE	REFLOW(2)
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable(3)	suitable
PLCC(4), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(4)(5)	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended(6)	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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