19-1762; Rev 0; 7/00

MAXIM

±15kV ESD-Protected, Low-Voltage, Dual, SPST, CMOS Analog Switches

General Description

The MAX4575/MAX4576/MAX4577 are low-voltage, high electrostatic discharge (ESD)-protected, dual single-pole/single-throw (SPST) analog switches. The normally closed (NO) and normally open (NC) pins are protected against ±15kV ESD without latchup or damage. Each switch can handle Rail-to-Rail® analog signals. Off-leakage current is 0.5nA at +25°C. These analog switches are suitable for low-distortion audio applications and are the preferred solution over mechanical relays in automated test equipment or applications where current switching is required. They have low power requirements (0.5µW), require less board space, and are more reliable than mechanical relays. Each device is controlled by TTL/CMOS input voltage levels and is bilateral.

These switches feature guaranteed operation from a single supply of +2V to +12V, making them ideal for use in battery-powered applications. On-resistance is 70Ω (max), matched between switches to 0.5Ω (typ) and flat (2Ω typ) over the specified signal range.

The MAX4575 has two NO switches, the MAX4576 has two NC switches, and the MAX4577 has one NO and one NC switch. These devices are available in 8-pin µMAX and SO packages.

Applications

Battery-Powered Systems

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Sample-and-Hold Circuits

Communications Circuits

Relay Replacement

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4575EUA	-40°C to +85°C	8 µMAX
MAX4575ESA	-40°C to +85°C	8 SO
MAX4576EUA	-40°C to +85°C	8 µMAX
MAX4576ESA	-40°C to +85°C	8 SO
MAX4577EUA	-40°C to +85°C	8 µMAX
MAX4577ESA	-40°C to +85°C	8 SO

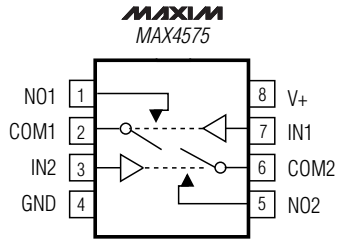
Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Features

- **ESD-Protected NO/NC Pins**
  - **±15kV (Human Body Model)**
  - **±15kV (IEC 1000-4-2 Air-Gap Discharge)**
  - **±8kV (IEC 1000-4-2 Contact Discharge)**
- **Pin Compatible with MAX4541/MAX4542/MAX4543**
- **Guaranteed On-Resistance**
  - **70Ω (max) at +5V**
  - **150Ω (max) at +3V**
- **On-Resistance Flatness**
  - **2Ω (typ) at +5V**
  - **6Ω (typ) at +3V**
- **On-Resistance Matching**
  - **0.5Ω (typ) at +5V**
  - **0.6Ω (typ) at +3V**
- **Guaranteed 0.5nA Leakage Current at T_A = +25°C**
- **+2V to +12V Single-Supply Voltage**
- **TTL/CMOS-Logic Compatible**
- **Low Distortion: 0.015%**
- **-3dB Bandwidth >300MHz**
- **Rail-to-Rail Signal Range**

Pin Configurations/ Functional Diagrams/Truth Tables

TOP VIEW



SO/µMAX

MAX4575	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Pin Configurations/Functional Diagrams/Truth Tables continued at end of data sheet.

±15kV ESD-Protected, Low-Voltage, Dual, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +13V
IN_, COM_, NO_, NC_ to GND (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current (NO_, NC_, COM).....±10mA
Peak Current (NO_, NC_, COM_; pulsed at 1ms 10% duty cycle).....±30mA
ESD Protection per Method IEC 1000-4-2 (NO_, NC_)
Air-Gap Discharge.....±15kV
Contact Discharge.....±8kV
ESD Protection per Method 3015.7
NO_, NC_.....±15kV
V+, GND, IN_, COM_.....±2.5kV

Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.1mW/°C above +70°C).....330mW
8-Pin SO (derate 8mW/°C above +70°C).....640mW
Operating Temperature Range
MAX457_E_A.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Maximum Die Temperature.....+150°C
Lead Temperature (soldering, 10s).....+300°C

Note 1: Signals on NO_, NC_, COM_, or IN_ exceeding V+ or GND are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—SINGLE +5V SUPPLY

(V+ = +4.5V to +5.5V, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V+ = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Input Voltage Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +4.5V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	T_A = +25°C		45	70	Ω
			T_A = T_{MIN} to T_{MAX}			75	
On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V+ = +4.5V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	T_A = +25°C		0.5	2	Ω
			T_A = T_{MIN} to T_{MAX}			3	
On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V+ = +4.5V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ or $V_{NC\_}$ = 1V, 2.25V, 3.5V	T_A = +25°C		2	4	Ω
			T_A = T_{MIN} to T_{MAX}			5	
Off-Leakage Current (NO_ or NC_) (Note 5)	$I_{NO\_}$, $I_{NC\_}$	V+ = 5.5V $V_{COM\_}$ = 1V, 4.5V $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1V	T_A = +25°C	-0.5	0.01	0.5	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	
COM_ Off-Leakage Current (Note 5)	$I_{COM\_(OFF)}$	V+ = 5.5V $V_{COM\_}$ = 1V, 4.5V $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1V	T_A = +25°C	-0.5	0.01	0.5	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	
COM_ On-Leakage Current (Note 5)	$I_{COM\_(ON)}$	V+ = 5.5V $V_{COM\_}$ = 1V, 4.5V $V_{NO\_}$ or $V_{NC\_}$ = 1V, 4.5V or floating	T_A = +25°C	-1	0.02	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	

ELECTRICAL CHARACTERISTICS—SINGLE +5V SUPPLY (continued)

(V+ = +4.5V to +5.5V, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V+ = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUT							
IN_ Input High	V_{IH}			2.4			V
IN_ Input Low	V_{IL}					0.8	V
Logic Input Leakage	I_{IN}	V_{IN} = 0 or V+		-1		1	µA
SWITCH DYNAMIC							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 1	T_A = +25°C		90	150	ns
			T_A = T_{MIN} to T_{MAX}			180	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 1	T_A = +25°C		50	80	ns
			T_A = T_{MIN} to T_{MAX}			100	
Break-Before-Make (MAX4577 only)		$V_{COM\_}$ = 3V, R_L = 300Ω, C_L = 35pF	T_A = +25°C	5	45		ns
			T_A = T_{MIN} to T_{MAX}	4			
On-Channel Bandwidth -3dB	BW	Signal = 0dBm, R_{IN} = R_{OUT} = 50Ω, C_L = 5pF, Figure 2			300		MHz
Charge Injection	Q	V_{GEN} = 2V, C_L = 1.0nF, R_{GEN} = 0, Figure 3			4		pC
NO_ or NC_ Off-Capacitance	C_{OFF}	$V_{NO\_}$ = $V_{NC\_}$ = GND, f = 1MHz, Figure 4			20		pF
COM_ Off-Capacitance	$C_{COM(OFF)}$	$V_{COM\_}$ = GND, f = 1MHz, Figure 4			12		pF
COM_ On-Capacitance	$C_{COM(ON)}$	$V_{COM\_}$ = $V_{NO\_}$, $V_{NC\_}$ = GND, f = 1MHz,			20		pF
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 2			-75		dB
		R_L = 50Ω, C_L = 5pF, f = 10MHz, Figure 2			-45		
Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6			-90		dB
		R_L = 50Ω, C_L = 5pF, f = 10MHz, Figure 6			-70		
Total Harmonic Distortion	THD	R_L = 600Ω, f = 20Hz to 20kHz			0.015		%
ESD SCR Holding Current	I_H				110		mA
ESD SCR Holding Voltage	V_H				3		V
POWER SUPPLY							
Power-Supply Range	V+			2		12	V
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0 or V+	T_A = +25°C			1	µA
			T_A = T_{MIN} to T_{MAX}			10	

±15kV ESD-Protected, Low-Voltage, Dual, SPST, CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—SINGLE +3V SUPPLY

(V+ = +2.7V to +3.6V, V_{IH} = 2.0V, V_{IL} = 0.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Input Voltage Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 2.7V; $I_{COM\_}$ = 1mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		70	120	Ω
			T_A = T_{MIN} to T_{MAX}			150	
On-Resistance Match Between Channels (Notes 3, 8)	ΔR_{ON}	V+ = 2.7V; $I_{COM\_}$ = 1mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		0.6	3	Ω
			T_A = T_{MIN} to T_{MAX}			4	
On-Resistance Flatness (Notes 4, 8)	$R_{FLAT(ON)}$	V+ = 2.7V; $I_{COM\_}$ = 1mA; $V_{NO\_}$ or $V_{NC\_}$ = 0.5V, 1.5V, 2.2V	T_A = +25°C		6	12	Ω
			T_A = T_{MIN} to T_{MAX}			15	
LOGIC INPUT							
IN_ Input High	V_{IH}			2.0			V
IN_ Input Low	V_{IL}					0.6	V
Logic Input Leakage Current	I_{IN}	V_{IN} = 0 or V+		-1		1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1	T_A = +25°C		150	250	ns
			T_A = T_{MIN} to T_{MAX}			300	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1	T_A = +25°C		60	100	ns
			T_A = T_{MIN} to T_{MAX}			150	
Break-Before-Make (MAX4577 only)		$V_{COM\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF	T_A = +25°C	5			ns
			T_A = T_{MIN} to T_{MAX}	4			
Charge Injection	Q	V_{GEN} = 1.5V, C_L = 1.0nF, R_{GEN} = 0, Figure 3			5		pC
ESD SCR Holding Current	I_H				110		mA
ESD SCR Holding Voltage	V_H				3		V
POWER SUPPLY							
Power-Supply Range	V+			2		12	V
Positive Supply Current	I+	V+ = 3.6V, V_{IN} = 0 or V+	T_A = +25°C			1	µA
			T_A = T_{MIN} to T_{MAX}			10	

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.

Note 3: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and the minimum values of on-resistance as measured over the specified analog signal ranges.

Note 5: Leakage parameters are 100% tested at $T_{A(MAX)}$, and guaranteed by correlation at +25°C.

Note 6: Off-Isolation = $20\log_{10}(V_{COM} / V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

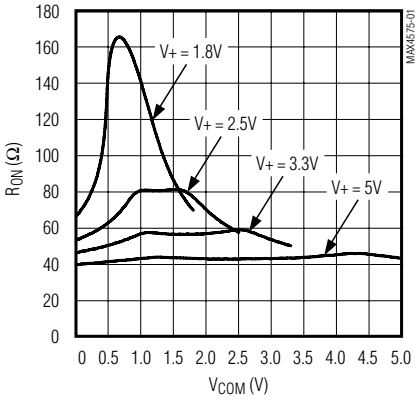
Note 7: Between any two switches.

Note 8: Guaranteed by design.

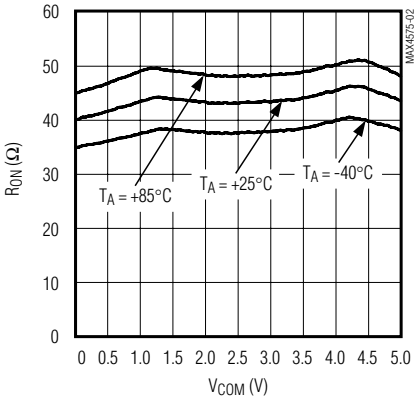
Typical Operating Characteristics

(V+ = 5V, T_A = +25°C, unless otherwise specified.)

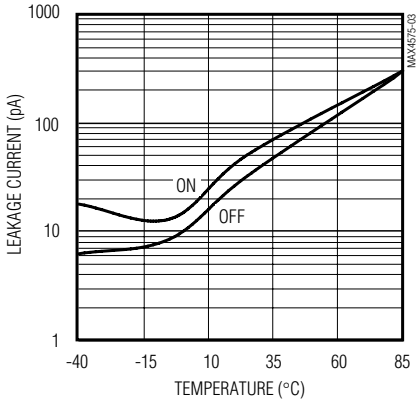
ON-RESISTANCE vs. V_{COM} AND SUPPLY VOLTAGE



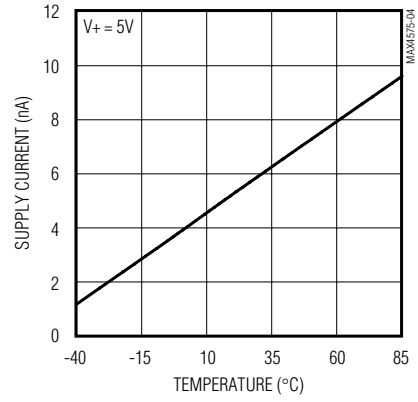
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



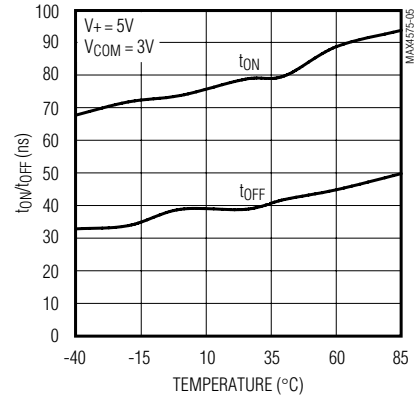
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



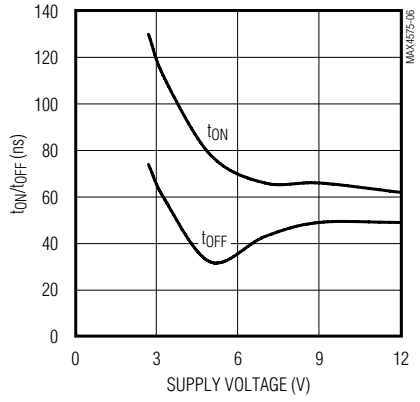
SUPPLY CURRENT vs. V_{CC} AND TEMPERATURE



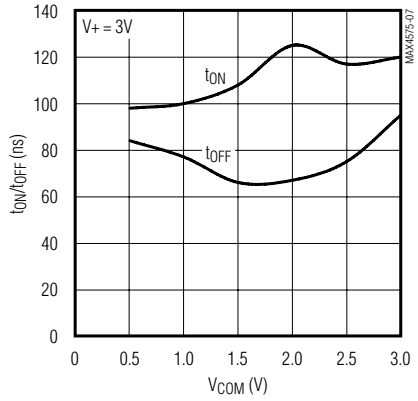
TURN-ON/TURN-OFF TIME vs. TEMPERATURE



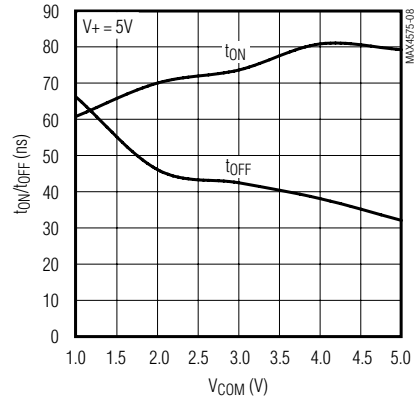
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



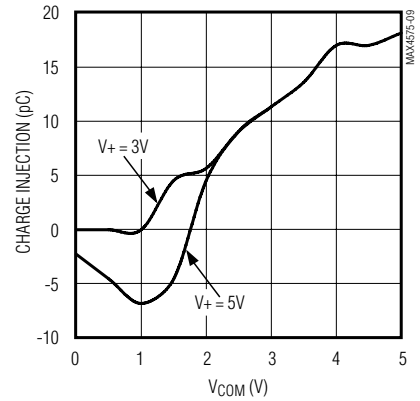
TURN-ON/TURN-OFF TIME vs. V_{COM} (V+ = 3V)



TURN-ON/TURN-OFF vs. V_{COM} (V+ = 5V)



CHARGE INJECTION vs. V_{COM}

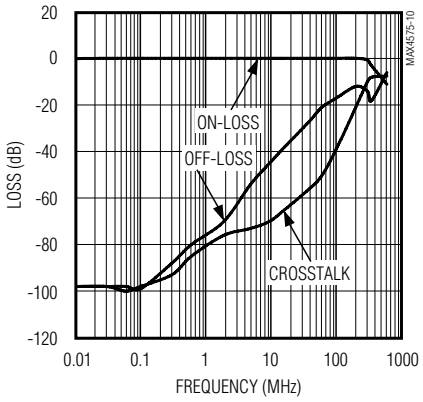


±15kV ESD-Protected, Low-Voltage, Dual, SPST, CMOS Analog Switches

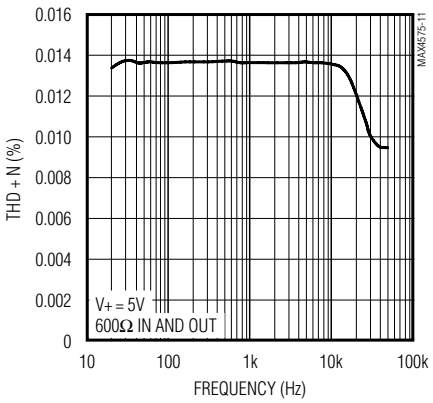
Typical Operating Characteristics (continued)

(V+ = 5V, T_A = +25°C, unless otherwise specified.)

FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



Pin Description

PIN			NAME	FUNCTION
MAX4575	MAX4576	MAX4577		
1	—	1	NO1	Analog Switch 1—Normally Open
—	1	—	NC1	Analog Switch 1—Normally Closed
2	2	2	COM1	Analog Switch 1—Common
3	3	3	IN2	Digital Control Input 2
4	4	4	GND	Ground
5	—	—	NO2	Analog Switch 2—Normally Open
—	5	5	NC2	Analog Switch 2—Normally Closed
6	6	6	COM2	Analog Switch 2—Common
7	7	7	IN1	Digital Control Input 1
8	8	8	V+	Positive Supply Voltage Input

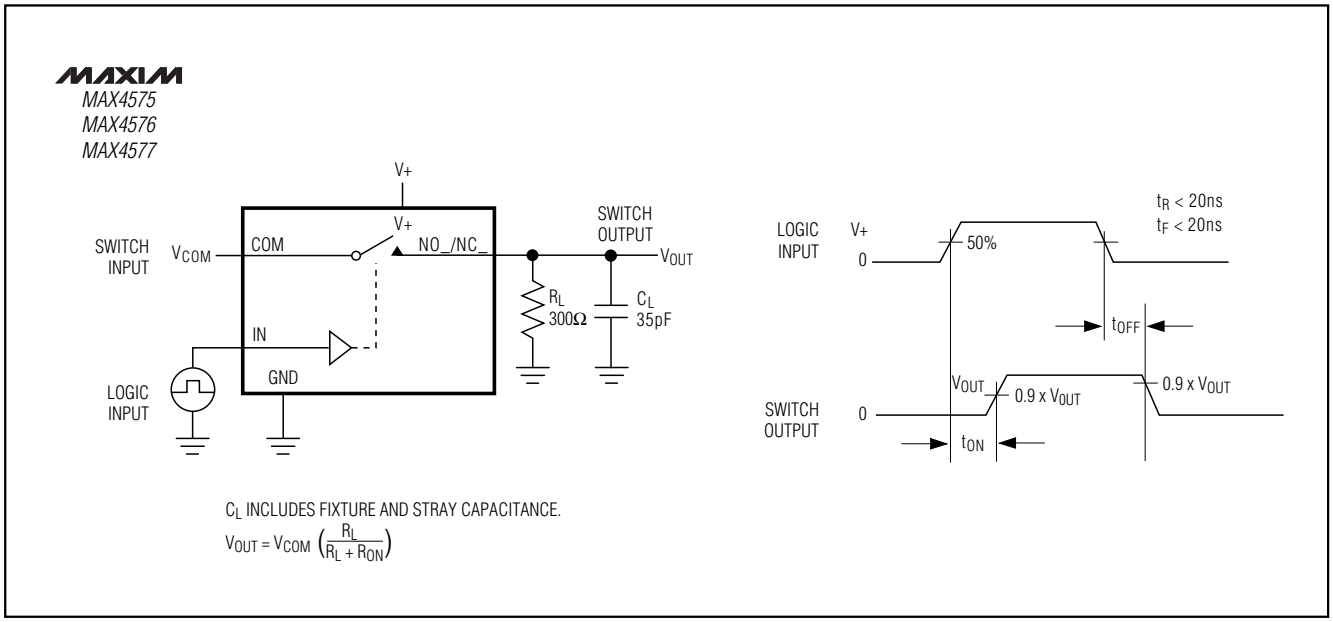


Figure 1. Switching Time

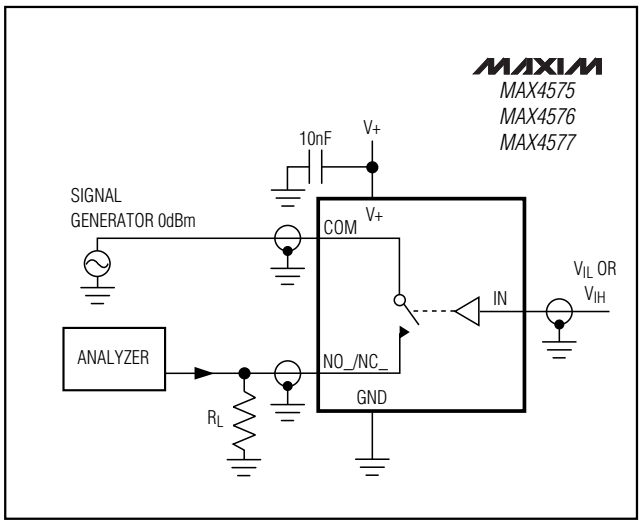


Figure 2. Off-Isolation/On-Channel Bandwidth

Detailed Description

The MAX4575/MAX4576/MAX4577 are dual SPST CMOS analog switches with circuitry providing ±15kV ESD protection on the NO and NC pins. The CMOS switch construction provides rail-to-rail signal handling while consuming virtually no power. Each of the two switches is independently controlled by a TTL/CMOS-level-compatible digital input.

Applications Information

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always sequence V+ on first, followed by the logic inputs, NO/NC, or COM.

Operating Considerations for High-Voltage Supply

The MAX4575/MAX4576/MAX4577 are capable of +12V single-supply operation with some precautions. The absolute maximum rating for V+ is +13V (referenced to GND). When operating near this region, bypass V+ with a minimum 0.1µF capacitor to ground as close to the IC as possible.

±15kV ESD Protection

The MAX4575/MAX4576/MAX4577 are ±15kV ESD protected (according to IEC 1000-4-2) at the NC/NO terminals. To accomplish this, bidirectional SCRs are included on-chip between these terminals. When the voltages at these terminals go Beyond-the-Rail™, the corresponding SCRs turns on in a few nanoseconds

Beyond-the-Rail is a trademark of Maxim Integrated Products.

±15kV ESD-Protected, Low-Voltage, Dual, SPST, CMOS Analog Switches

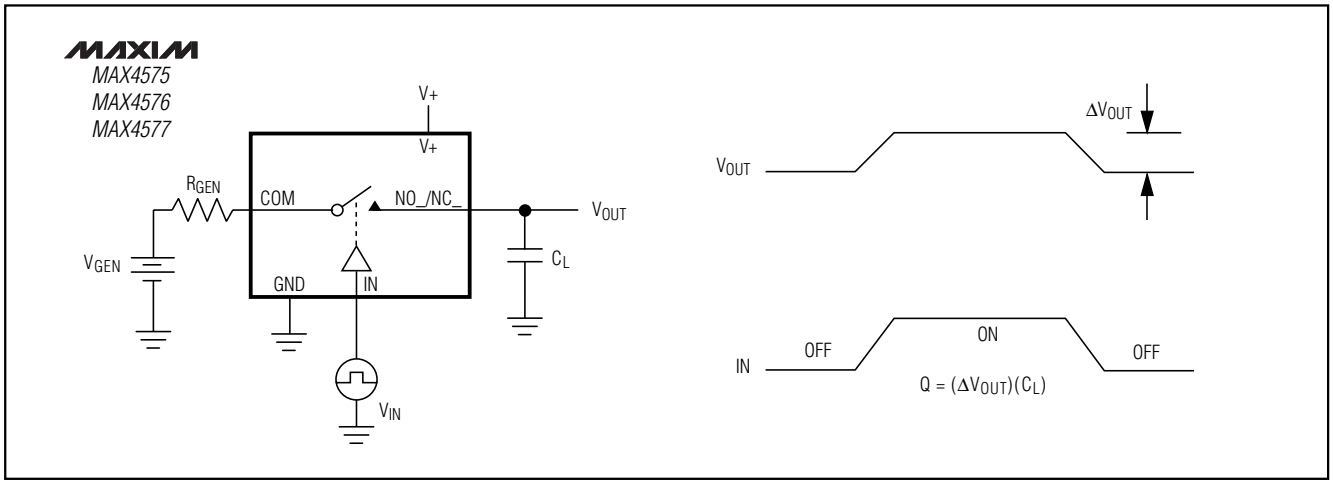


Figure 3. Charge Injection

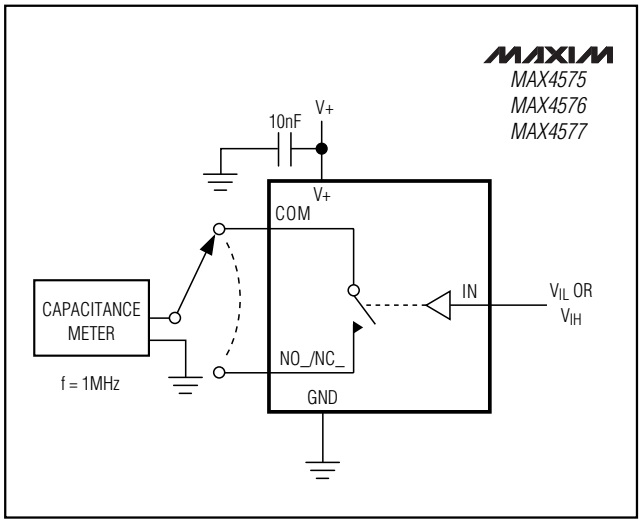


Figure 4. Channel Off/On-Capacitance

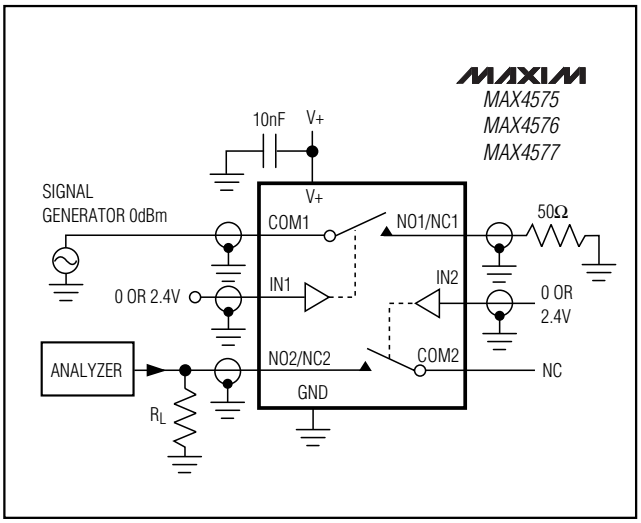


Figure 5. Crosstalk

and bypass the surge safely to ground. This method is superior to using diode clamps to the supplies because, unless the supplies are very carefully decoupled through low-ESR capacitors, the ESD current through the diode clamp could cause a significant spike in the supplies. This may damage or compromise the reliability of any other chip powered by those same supplies.

There are diodes from NC/NO to the supplies in addition to the SCRs. There is a resistance in series with each of these diodes to limit the current into the supplies during an ESD strike. The diodes protect these terminals from overvoltages that are not a result of ESD strikes. These diodes also protect the device from improper power-supply sequencing.

Once the SCR turns on because of an ESD strike, it continues to be on until the current through it falls below its "holding current." The holding current is typically 110mA in the positive direction (current flowing into the NC/NO terminal) at room temperature (see SCR Holding Current vs. Temperature in the *Typical Operating Characteristics*). Design the system so that any sources connected to NC/NO are current limited to a value below the holding current to ensure the SCR

turns off when the ESD event is finished and normal operation may be resumed. Also, keep in mind that the holding current varies significantly with temperature. The worst case is at +85°C when the holding currents drop to 70mA. Since this is a typical number to guarantee turn-off of the SCRs under all conditions, the sources connected to these terminals should be current limited to not more than half this value. When the SCR is latched, the voltage across it is about 3V, depending on the polarity of the pin current. The supply voltages do not affect the holding current appreciably. The sources connected to the COM side of the switches do not need to be current limited since the switches turn off internally when the corresponding SCR(s) latches.

Even though most of the ESD current flows to GND through the SCRs, a small portion of it goes into V+. Therefore, it is a good idea to bypass the V+ with 0.1µF capacitors directly to the ground plane.

ESD protection can be tested in various ways. Transmitter outputs and receiver inputs are characterized for protection to the following:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)
- ±15kV using the Air-Gap Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2).

ESD Test Conditions

Contact Maxim Integrated Products for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 6 shows the Human Body Model and Figure 7 shows the waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which can be discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4575/MAX4576/MAX4577 enable the design of equipment that meets Level 4 (the highest level) of IEC 1000-4-2, without additional ESD protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 8), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 9 shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Chip Information

TRANSISTOR COUNT: 78

PROCESS: CMOS

±15kV ESD-Protected, Low-Voltage, Dual, SPST, CMOS Analog Switches

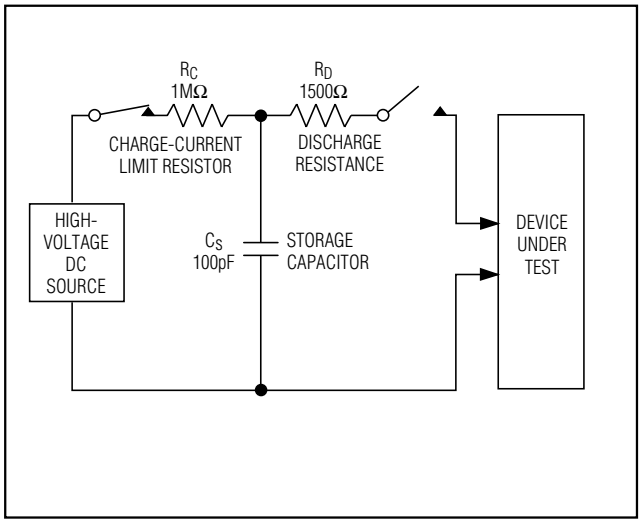


Figure 6. Human Body ESD Test Model

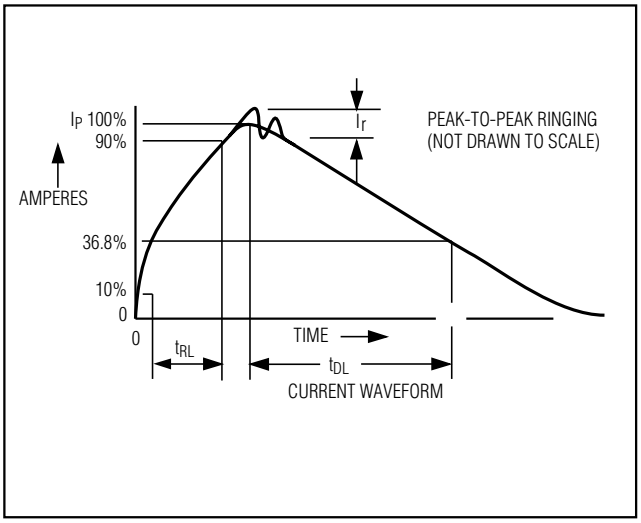


Figure 7. Human Body Model Current Waveform

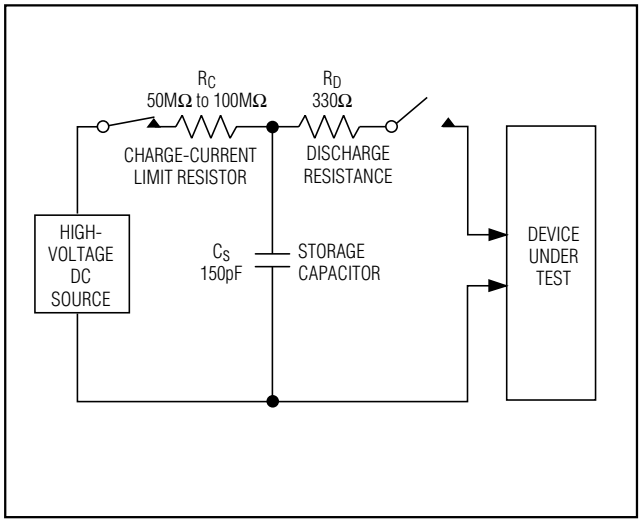


Figure 8. IEC 1000-4-2 ESD Test Model

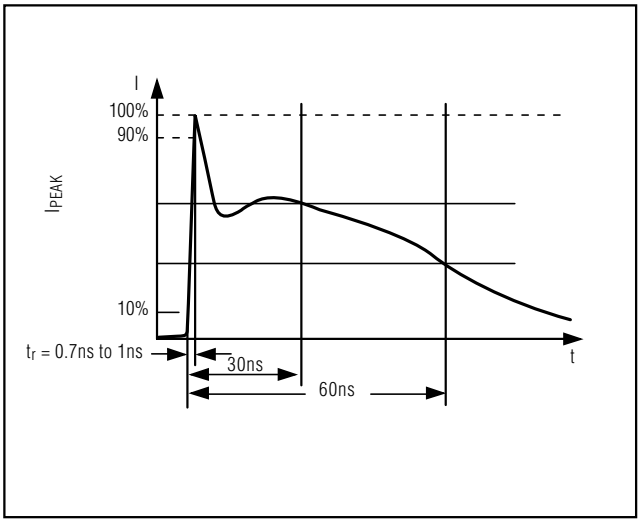
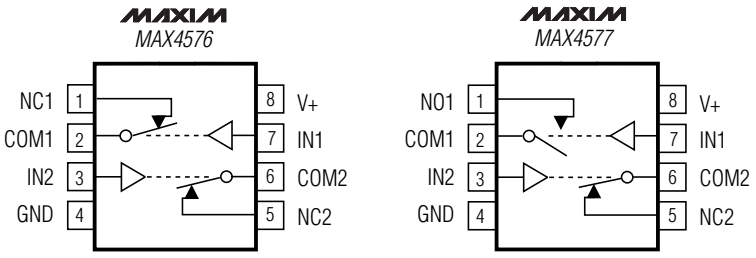


Figure 9. IEC 1000-4-2 ESD Generator Current Waveform

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



SO/μMAX

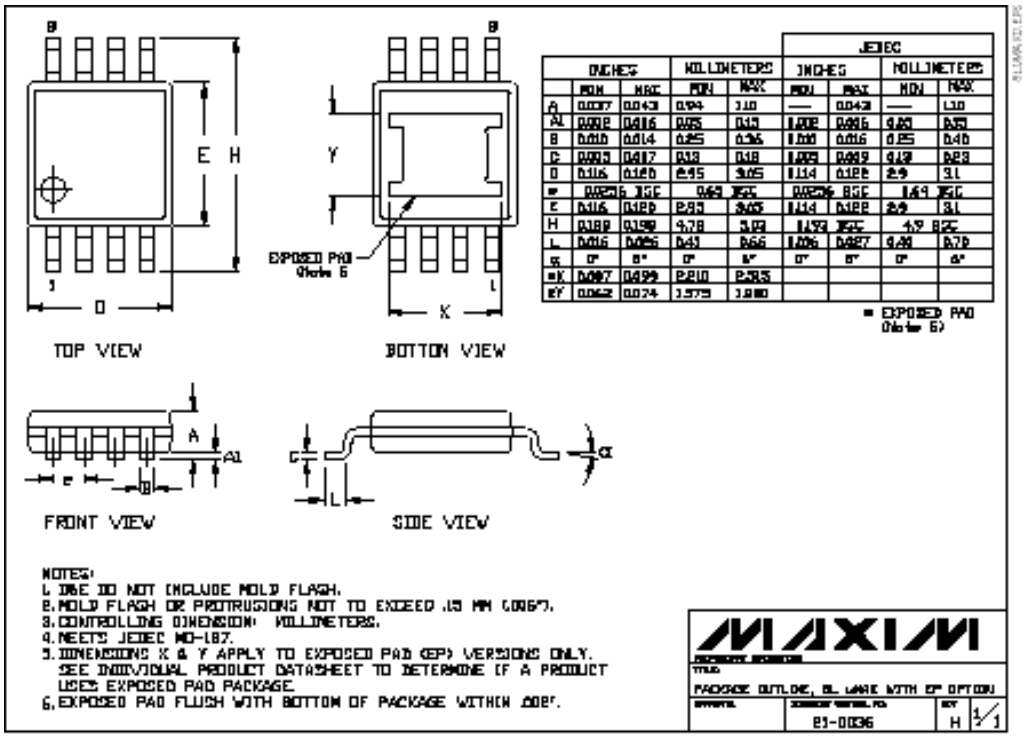
SO/μMAX

MAX4576	
LOGIC	SWITCH
0	ON
1	OFF

MAX4577		
LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

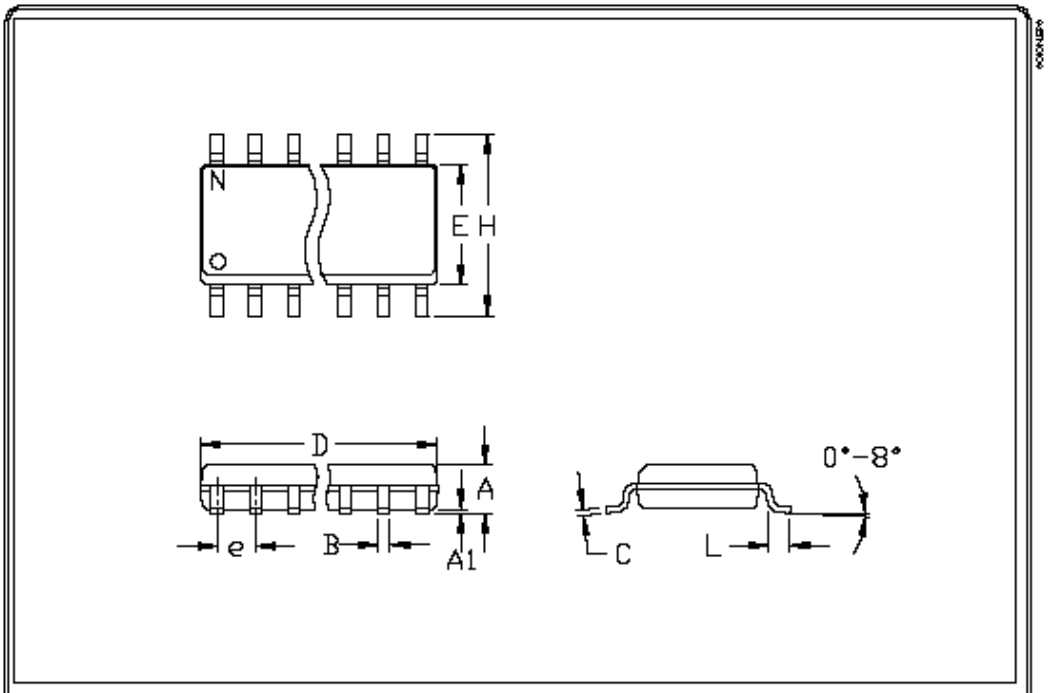
SWITCHES SHOWN FOR LOGIC "0" INPUT

Package Information



±15kV ESD-Protected, Low-Voltage, Dual, SPST, CMOS Analog Switches

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A