PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

M5M82C55AP-5

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

MITSUBISHI(MICMPTR/MIPRC)

DESCRIPTION

This is a family of general-purpose programmable input/output devices designed for use with the 8/16-bit parallel CPU as input/output ports.

This device is fabricated using silicon-gate CMOS technology for a single supply voltage. This LSI is a simple input and output interface for TTL circuits, having 24 input/output pins which correspond to three 8-bit input/output ports.

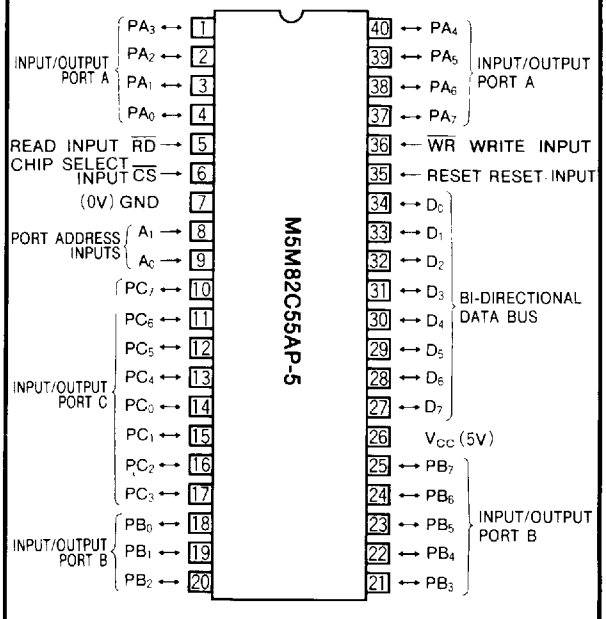
FEATURES

- 24 programmable I/O pins
- Single 5 V supply voltage
- TTL-compatible I_{OL}=2.5mA (max.)
- Direct bit set/reset capability
- Improved DC driving capability
- Improved timing characteristics
- Fully compatible with MELPS85, MELPS86, MELPS88 microprocessor series

APPLICATION

Input/output ports for MELPS85, MELPS86, MELPS88 microprocessor

PIN CONFIGURATION (TOP VIEW)

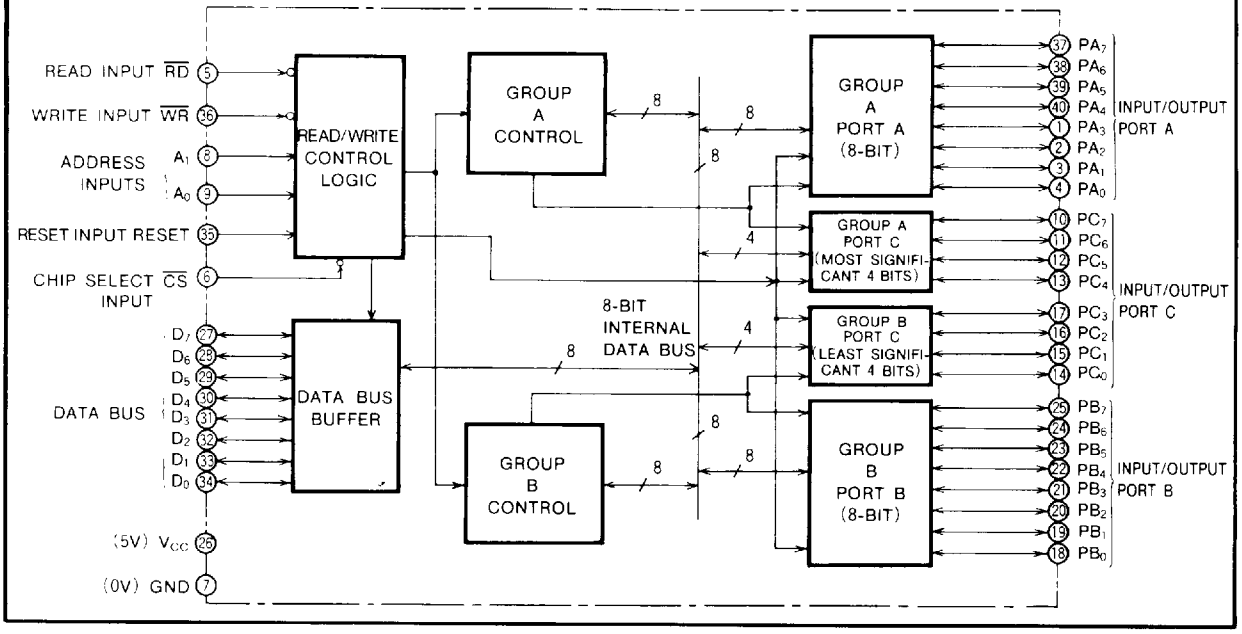


Outline 40P4

FUNCTION

These PPIs have 24 input/output pins which may be individually programmed in two 12-bit groups A and B with mode control commands from a CPU. They are used in three major modes of operation, mode 0 , mode 1 and mode 2 . Operating in mode 0 , each group of 12 pins may be programmed in sets of 4 to be inputs or outputs. In mode 1 , the 24 I/O terminals may be programmed in two 12-bit groups, group A and group B. Each group contains one 8-bit data port, which may be programmed to serve as input or output, and one 4-bit control port used for handshaking and interrupt control signals. Mode 2 is used with group A only, as one 8-bit bidirectional bus port and one 5-bit control port. Bit set/reset is controlled by CPU. A high-level reset input (RESET) clears all internal registers, and all ports are set to the input mode (high-impedance state).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, GND=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Output low voltage	I_{OL}=2.5mA			0.45	V
I_{OH}	High-level output current (Note 2)	GND=0V, V_{OH}=1.5V, R_{EXT}=750Ω	−1		−4	mA
I_{CC}	Supply current from V_{CC}	GND=0V. All input mode. RESET=0V. Other pins=V_{CC}.			10	μA
I_{IH}	High-level input voltage	GND=0V, V_I=V_{CC}			±10	μA
I_{IL}	Low-level input voltage	GND=0V, V_I=0V			±10	μA
I_{OZ}	Off-state output current	GND=0V, V_I=0~V_{CC}			±10	μA
C_i	Input capacitance	V_{IL}=GND, f=1MHz, 25mVrms T_a=25℃			10	pF
$C_{i/o}$	Input/output terminal capacitance	$V_{I/OL}$=GND, f=1MHz, 25mVrms, T_a=25℃			20	pF

Note 1: Current flowing into an IC is positive, out is negative.
2: It is valid for any 24input/output pins of PA, PB and PC.

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, GND=0V, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{w(R)}$	Read pulse width	t_{RR}		200			ns
$t_{su(PE-R)}$	Peripheral setup time before read	t_{IR}		0			ns
$t_{h(R-PE)}$	Peripheral hold time after read	t_{HR}		0			ns
$t_{su(A-R)}$	Address setup time before read	t_{AR}		0			ns
$t_{h(R-A)}$	Address hold time after read	t_{RA}		0			ns
$t_{w(W)}$	Write pulse width	t_{WW}		200			ns
$t_{su(DQ-W)}$	Data setup time before write	t_{DW}		100			ns
$t_{h(W-DQ)}$	Data hold time after write	t_{WD}		0			ns
$t_{su(A-W)}$	Address setup time before write	t_{AW}		0			ns
$t_{h(W-A)}$	Address hold time after write	t_{WA}		0			ns
$t_{w(ACK)}$	Acknowledge pulse width	t_{AK}		300			ns
$t_{w(STB)}$	Strobe pulse width	t_{ST}		350			ns
$t_{su(PE-STB)}$	Peripheral setup time before strobe	t_{PS}		0			ns
$t_{h(STB-PE)}$	Peripheral hold time after strobe	t_{PH}		150			ns
$t_{c(RW)}$	Read/write cycle time	t_{RV}		850			ns

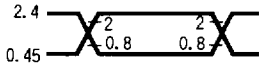
SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(R-DQ)}$	Propagation time from read to data output	t_{RD}	C_L=150pF			170	ns
$t_{PXZ(R-DQ)}$	Propagation time from read to data floating (Note 3)	t_{DF}		10		100	ns
$t_{PHL(W-PE)}$ $t_{PLH(W-PE)}$	Propagation time from write to output	t_{WB}				350	ns
$t_{PLH(STB-IBF)}$	Propagation time from strobe to IBF flag	t_{SIB}				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt	t_{SIT}				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt	t_{RIT}				400	ns
$t_{pHL(R-IBF)}$	Propagation time from read to IBF flag	t_{RIB}				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt	t_{WIT}				450	ns
$t_{PHL(W-OBF)}$	Propagation time from write to $\overline{OBF}$ flag	t_{WOB}				650	ns
$t_{pLH(ACK-OBF)}$	Propagation time from acknowledge to $\overline{OBF}$ flag	t_{AOB}				350	ns
$t_{PLH(ACK-INTR)}$	Propagation time from acknowledge to interrupt	t_{AIT}				350	ns
$t_{PZX(ACK-PE)}$	Propagation time from acknowledge to data output	t_{AD}				300	ns
$t_{PXZ(ACK-PE)}$	Propagation time from acknowledge to data floating (Note 3)	t_{KD}		20		250	ns

Note 3: Test conditions are not applied.

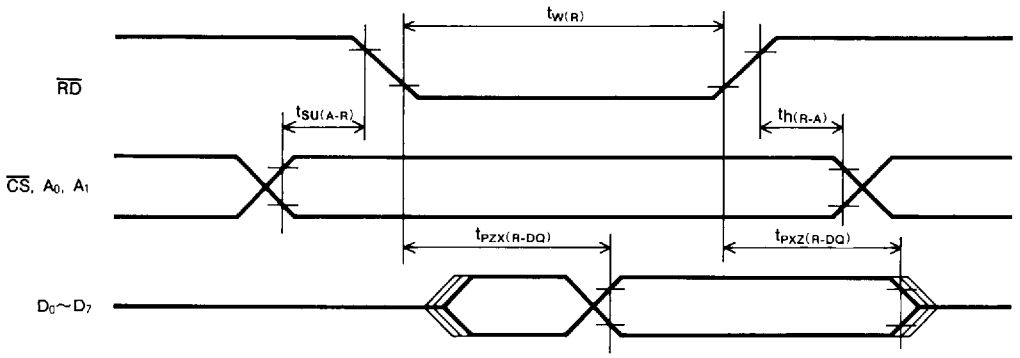
4: A.C Testing waveform

Input pulse level 0.45~2.4V
Input pulse rise time 10ns
Input pulse fall time 10ns
Reference level input V_{IH}=2V, V_{IL}=0.8V
Output V_{OH}=2V, V_{OL}=0.8V

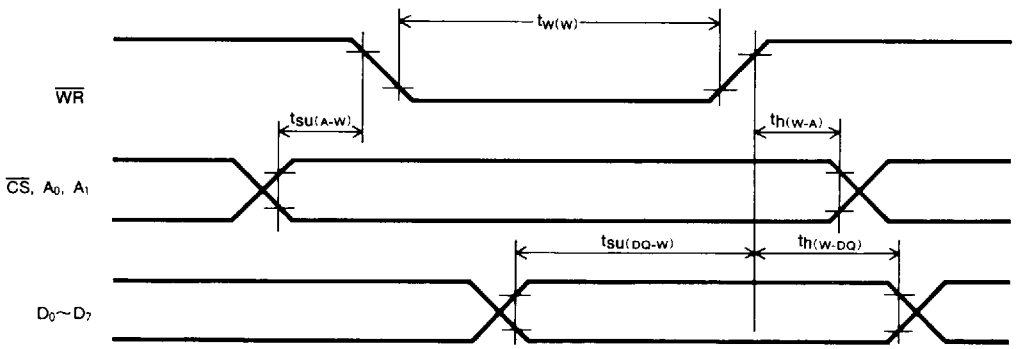


TIMING DIAGRAM

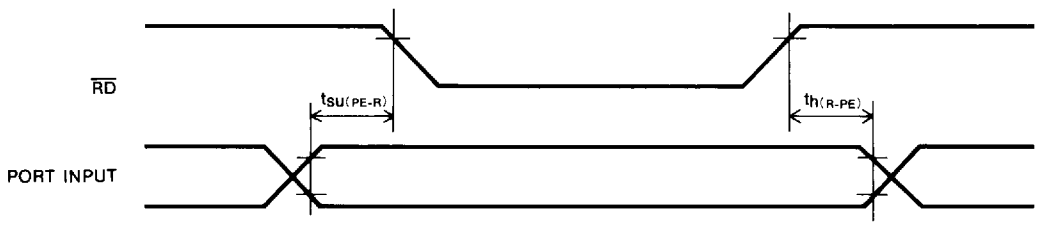
Data bus read operation



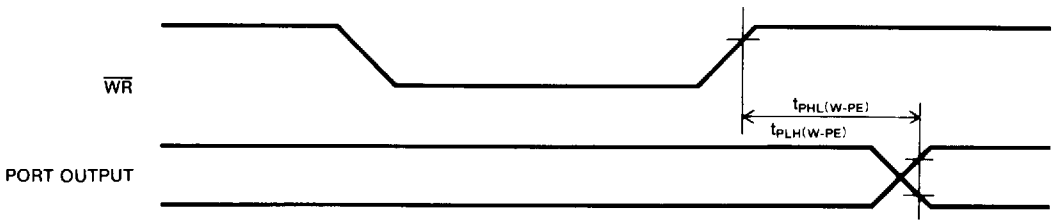
Data bus write operation



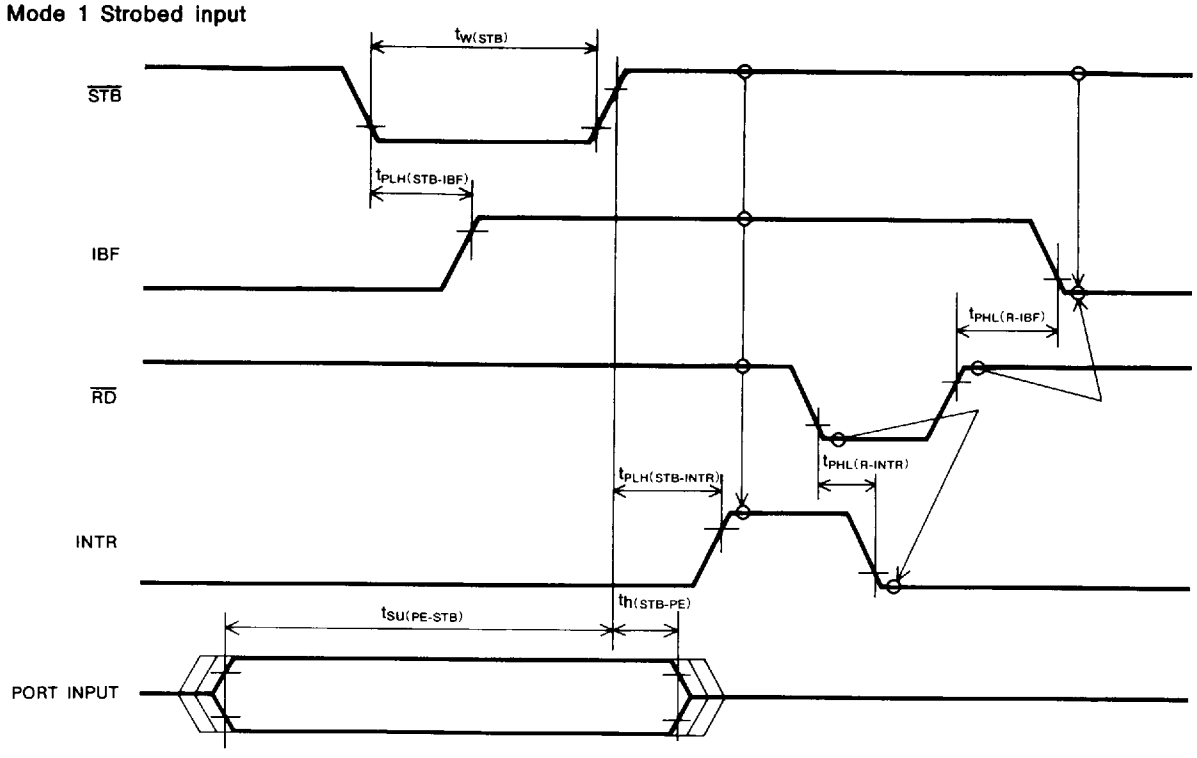
Mode 0 Port input



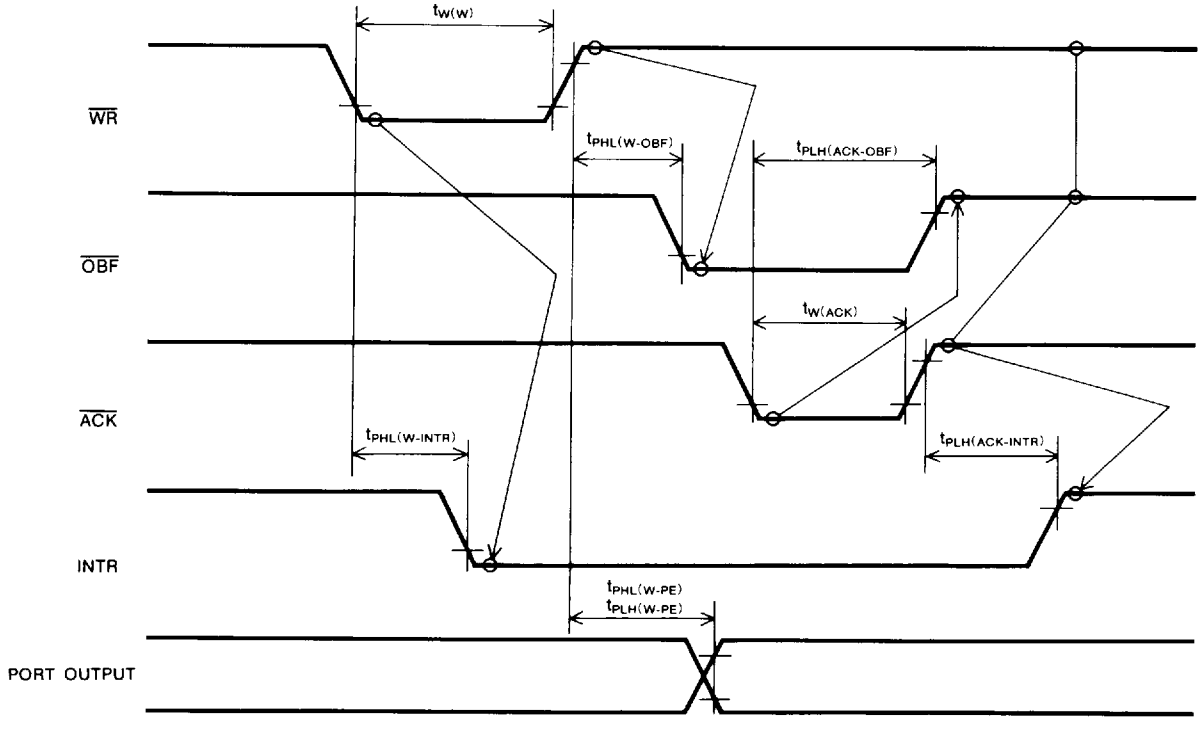
Mode 0, 1 Port output



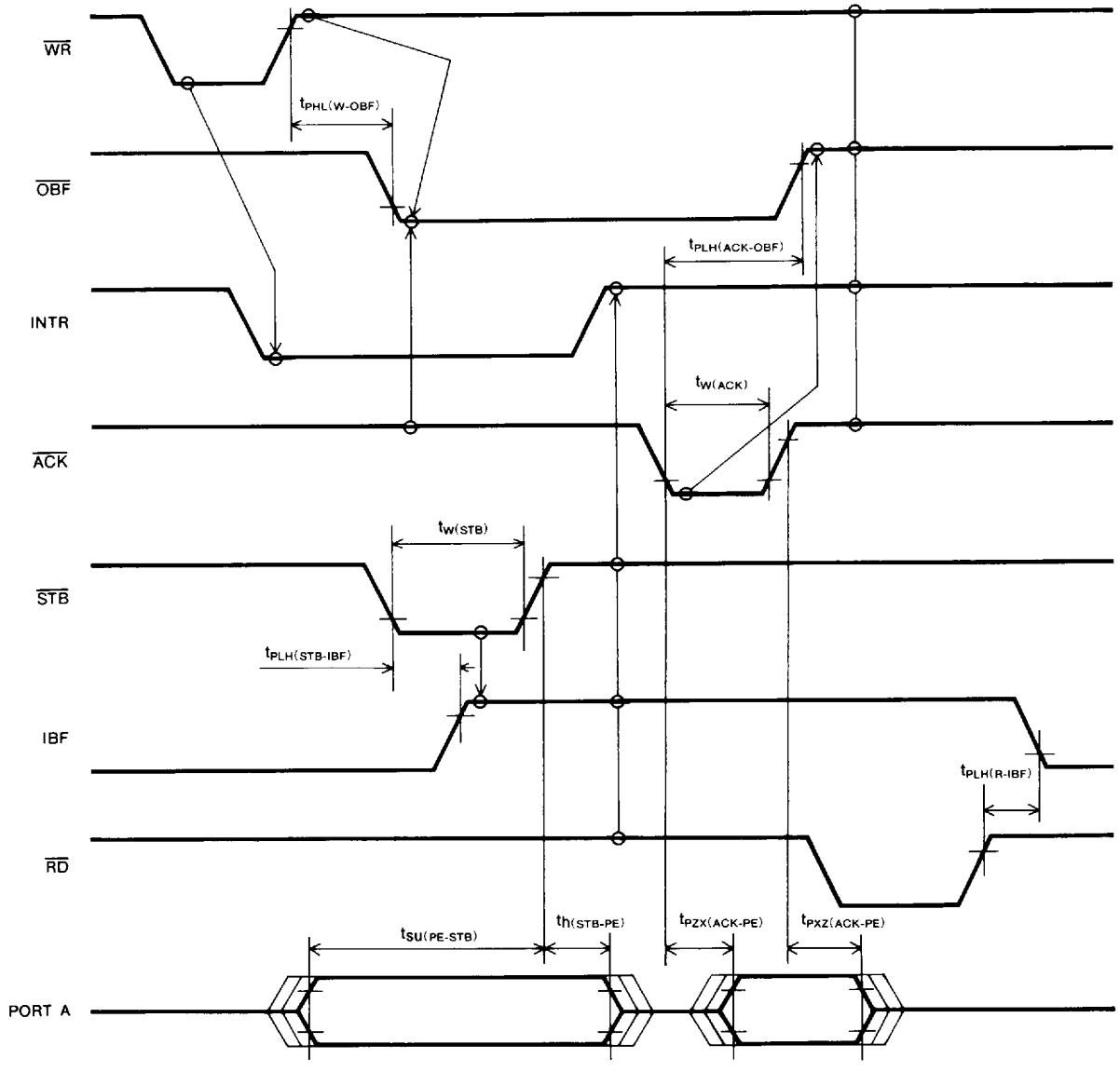
Mode 1 Strobed input



Mode 1 Strobed output



Mode 2 Bidirectional



Note 5: INTR=IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$