

MITSUBISHI MICROCOMPUTERS

38C3 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 38C3 group is the 8-bit microcomputer based on the 740 family core technology.

The 38C3 group has a LCD drive control circuit, a 10-channel A-D converter, and a Serial I/O as additional functions.

The various microcomputers in the 38C3 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 38C3 group, refer to the section on group expansion.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time 0.5 μ s
(at 8MHz oscillation frequency)
- Memory size
 - ROM 4 K to 48 K bytes
 - RAM 192 to 1024 bytes
- Programmable input/output ports 57
- Software pull-up/pull-down resistors
..... (Ports P0–P8 except Port P51)
- Interrupts 16 sources, 16 vectors
(includes key input interrupt)
- Timers 8-bit X 6, 16-bit X 1
- A-D converter 10-bit X 8 channels
- Serial I/O 8-bit X 1 (Clock-synchronized)

- LCD drive control circuit
 - Bias 1/1, 1/2, 1/3
 - Duty 1/1, 1/2, 1/3, 1/4
 - Common output 4
 - Segment output 32
- 2 Clock generating circuit
(connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
 - In high-speed mode 4.0 to 5.5 V
 - In middle-speed mode 2.5 to 5.5 V
 - In low-speed mode 2.5 to 5.5 V
- Power dissipation
 - In high-speed mode 32 mW
(at 8 MHz oscillation frequency)
 - In low-speed mode 45 μ W
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range – 20 to 85°C

APPLICATIONS

Camera, household appliances, consumer electronics, etc.

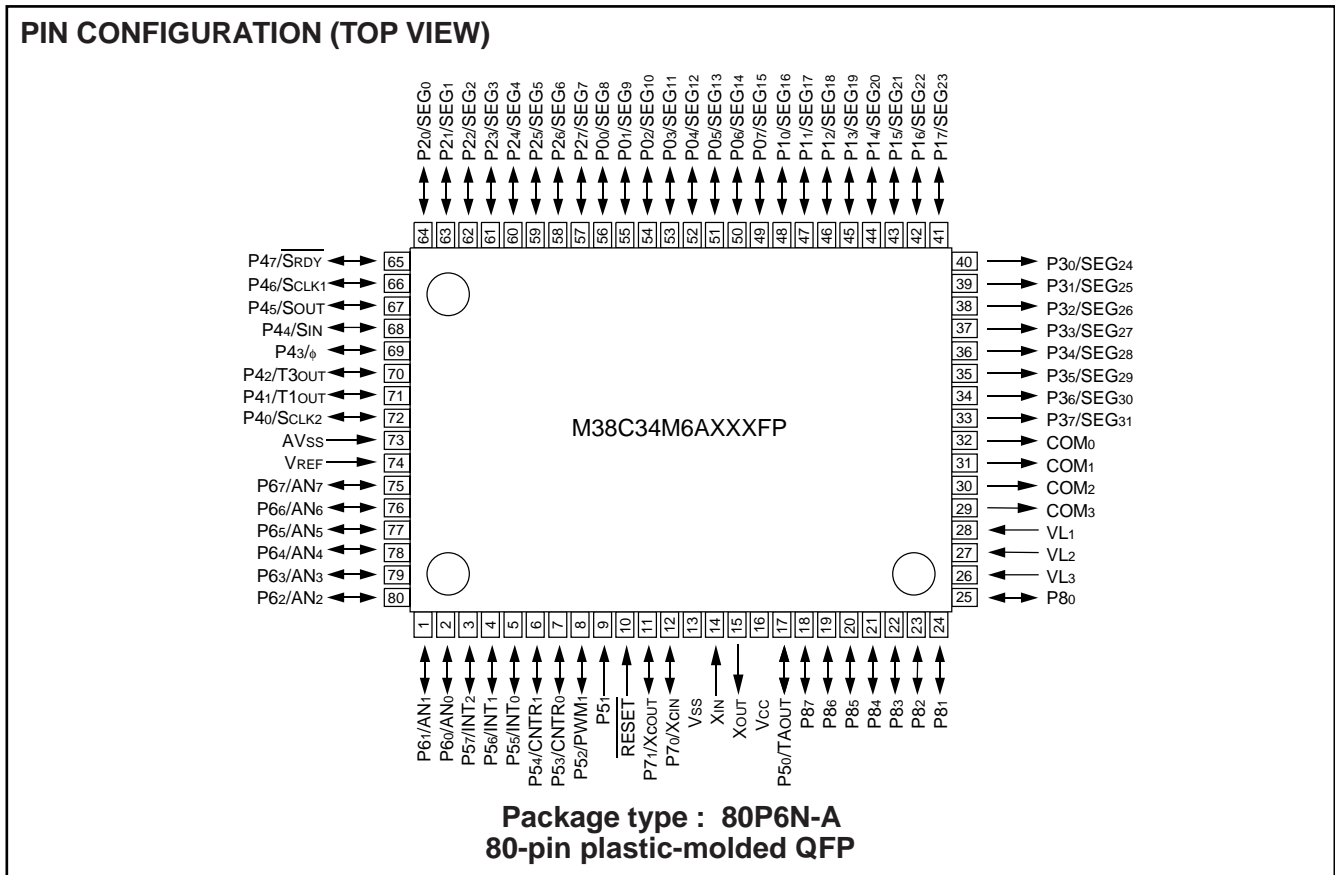


Fig. 1 M38C34M6AXXFP pin configuration

FUNCTIONAL BLOCK DIAGRAM

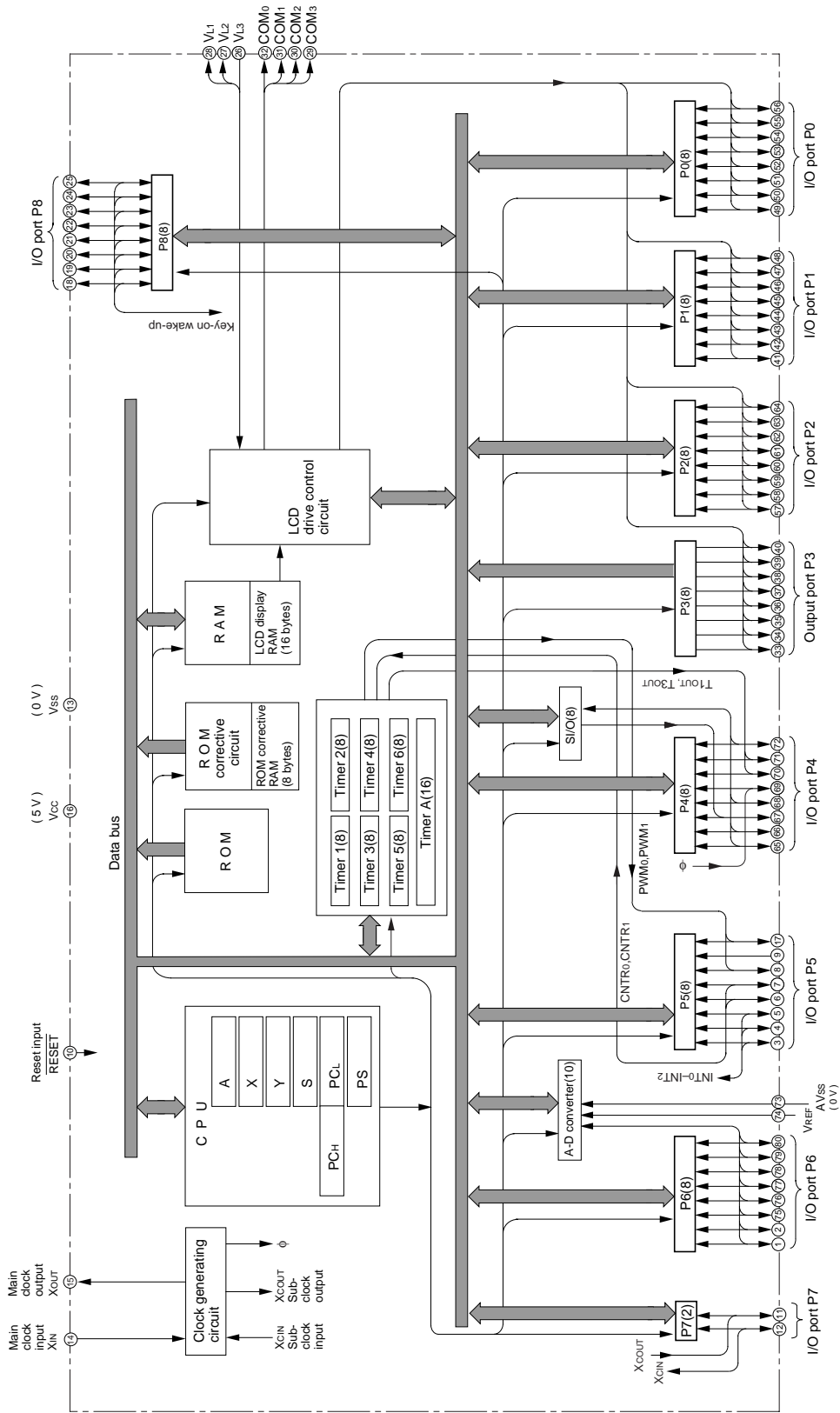


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	
			Function except a port function
Vcc, VSS	Power source	• Apply voltage of 2.5 V to 5.5 V to Vcc, and 0 V to Vss.	
VREF	Analog reference voltage	• Reference voltage input pin for A-D converter.	
AVSS	Analog power source	• GND input pin for A-D converter. • Connect to VSS.	
$\overline{\text{RESET}}$	Reset input	• Reset input pin for active "L."	
XIN	Clock input	<ul style="list-style-type: none"> • Input and output pins for the main clock generating circuit. • Feedback resistor is built in between XIN pin and XOUT pin. • Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. 	
XOUT	Clock output		
VL1 – VL3	LCD power source	<ul style="list-style-type: none"> • Input $0 \leq VL1 \leq VL2 \leq VL3 \leq Vcc$ voltage. • Input $0 - VL3$ voltage to LCD. 	
COM0 – COM3	Common output	<ul style="list-style-type: none"> • LCD common output pins. • COM1, COM2, and COM3 are not used at 1/1 duty ratio. • COM2 and COM3 are not used at 1/2 duty ratio. • COM3 is not used at 1/3 duty ratio. 	
P00/SEG9 – P07/SEG15	I/O port P0	<ul style="list-style-type: none"> • 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each port to be individually programmed as either input or output. • Pull-down control is enabled. 	• LCD segment pins
P10/SEG16 – P17/SEG23	I/O port P1		
P20/SEG0 – P27/SEG7	I/O port P2		
P30/SEG24 – P37/SEG31	Output port P3	<ul style="list-style-type: none"> • 8-bit output port. • CMOS state output. • Pull-down control is enabled. 	
P40/SCLK2	I/O port P4	<ul style="list-style-type: none"> • 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• Serial I/O function pin
P41/T1OUT			• Timer output pin
P42/T3OUT			• Timer output pin
P43/ ϕ			• ϕ output pin
P44/SIN, P45/SOUT, P46/SCLK1, P47/SRDY			• Serial I/O function pins

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
P51	Input port P5	<ul style="list-style-type: none"> • 1-bit input pin. • CMOS compatible input level. 	
P50/TAOUT	I/O port P5	<ul style="list-style-type: none"> • 7-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• Timer A output pin
P52/PWM1			• PWM1 output (timer output) pin
P53/CNTR0, P54/CNTR1			• External count I/O pins
P55/INT0, P56/INT1, P57/INT2			• External interrupt input pins
P60/AN0 – P67/AN7	I/O port P6	<ul style="list-style-type: none"> • 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• A-D conversion input pins
P70/XCOUT, P71/XCIN	I/O port P7	<ul style="list-style-type: none"> • 2-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• Sub-clock generating circuit I/O pins
P80 – P87	I/O port P8	<ul style="list-style-type: none"> • 8-bit I/O port. • TTL input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• Key input (Key-on wake-up) interrupt input pins

PART NUMBERING

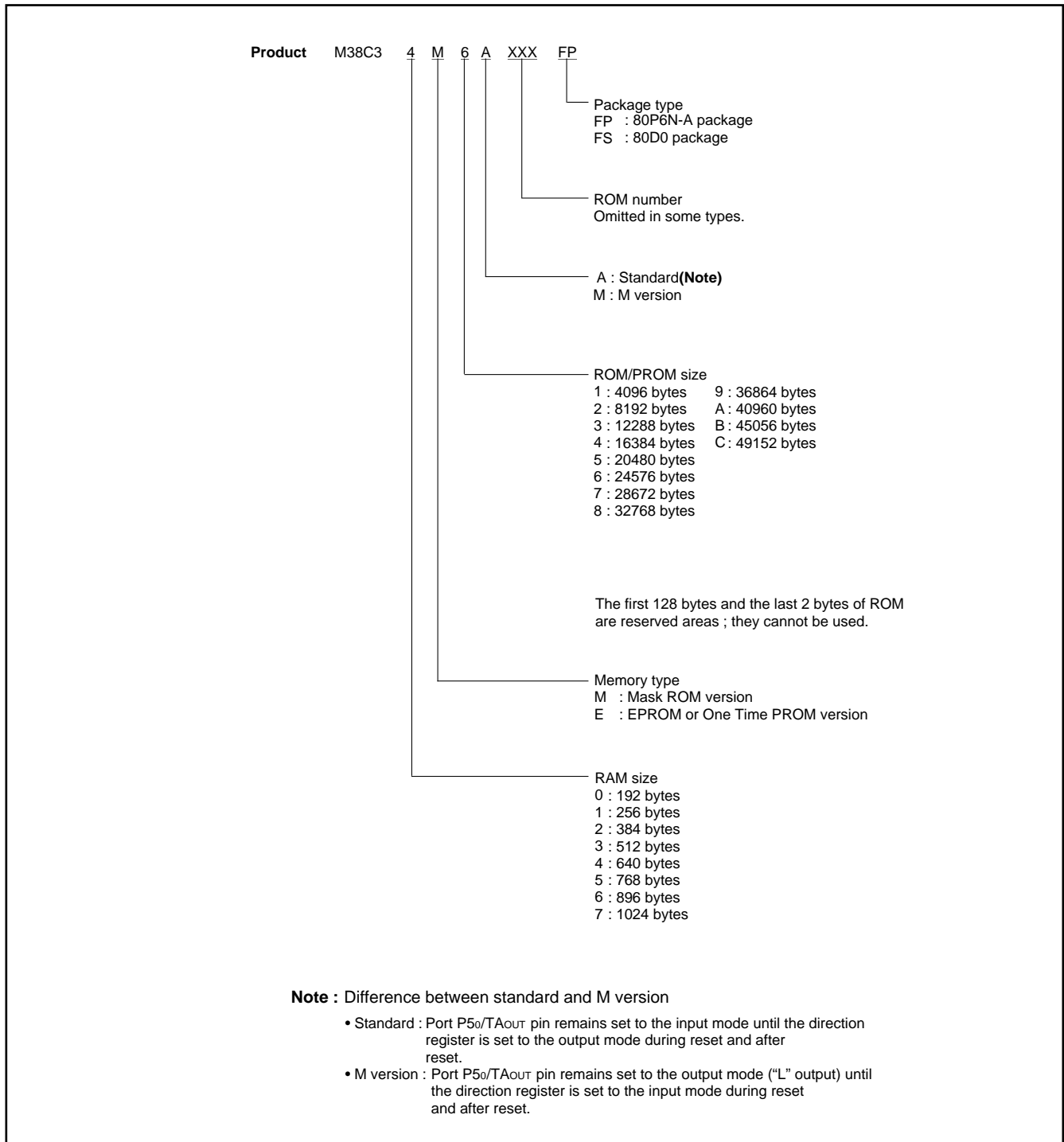


Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 38C3 group as follows.

Memory Type

Support for mask ROM, One Time PROM, and EPROM versions

Memory Size

ROM/PROM size 16 K to 48 K bytes

RAM size 512 to 1024 bytes

Packages

80P6N-A 0.8 mm-pitch plastic molded QFP

80D0 0.8 mm-pitch ceramic LCC (EPROM version)

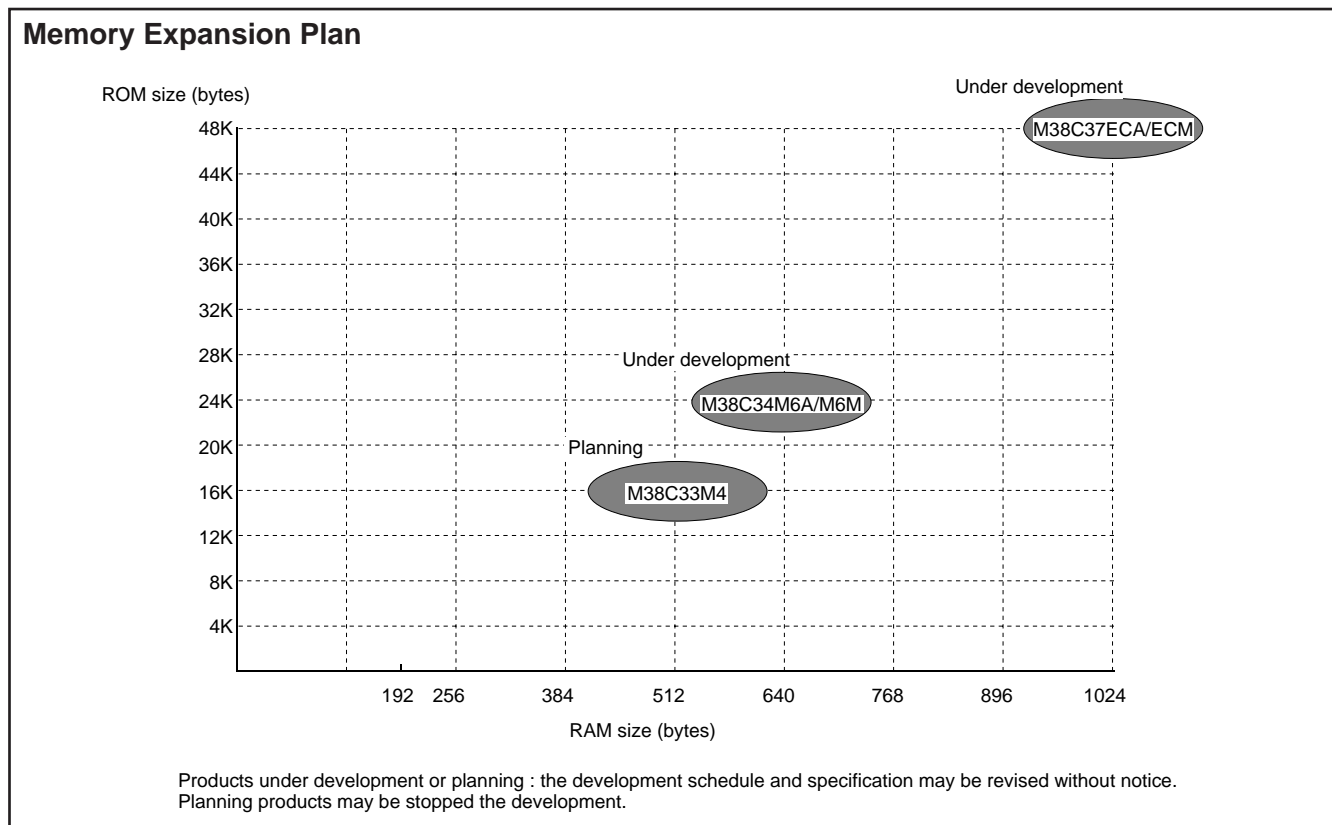


Fig. 4 Memory expansion plan

Currently planning products are listed below.

Table 3 Support products

As of April 1998

Product name	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38C34M6AXXFP	24576 (24446)	640	80P6N-A	Mask ROM version
M38C37ECAXXFP	49152 (49022)	1024		One Time PROM version
M38C37ECAFP			80D0	One Time PROM version (blank)
M38C37ECAFS	EPROM version			
M38C34M6MXXFP	24576 (24446)	640	80P6N-A	Mask ROM version
M38C37ECMXXFP	49152 (49022)	1024		One Time PROM version
M38C37ECMFP			80D0	One Time PROM version (blank)
M38C37ECMFS	EPROM version			

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 38C3 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

- The FST and SLW instruction cannot be used.
- The STP, WIT, MUL, and DIV instruction can be used.

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address 003B16.

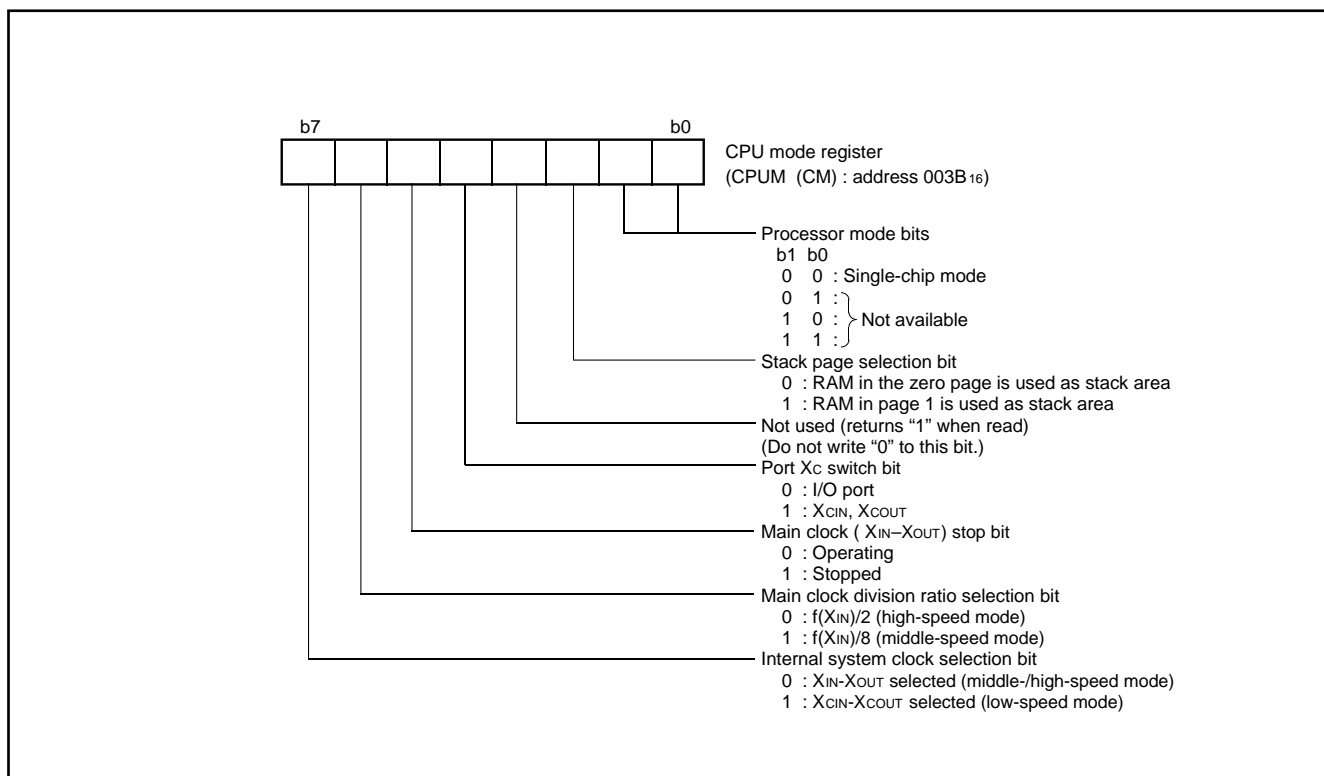


Fig. 5 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

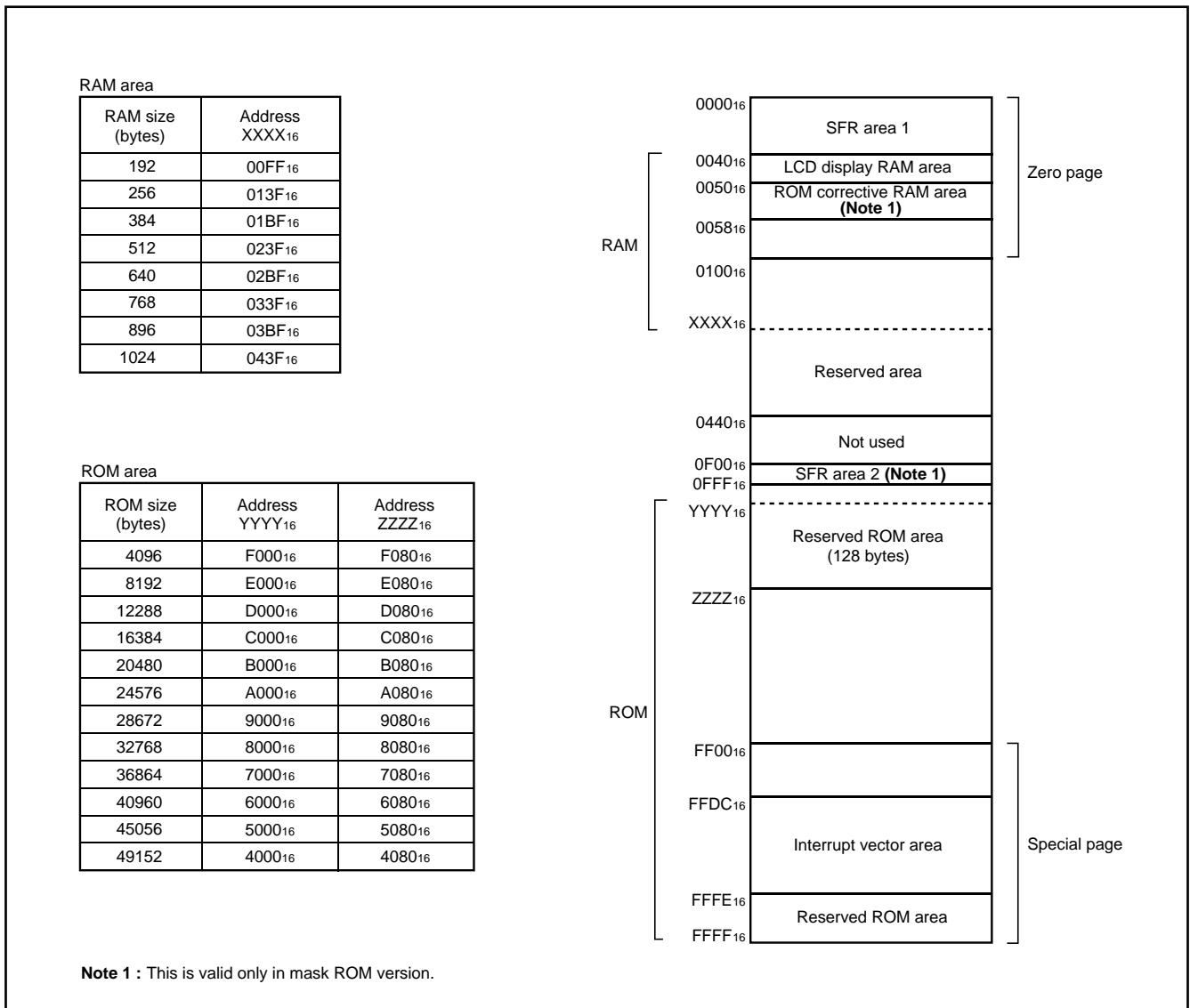


Fig. 6 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer 1 (T1)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 2 (T2)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 3 (T3)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer 4 (T4)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 5 (T5)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 6 (T6)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	
0007 ₁₆		0027 ₁₆	Timer 6 PWM register (T6PWM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer 12 mode register (T12M)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 34 mode register (T34M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Timer 56 mode register (T56M)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	φ output control register (CKOUT)
000C ₁₆	Port P6 (P6)	002C ₁₆	Timer A register (low) (TAL)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	Timer A register (high) (TAH)
000E ₁₆	Port P7 (P7)	002E ₁₆	Compare register (low) (CONAL)
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	Compare register (high) (CONAH)
0010 ₁₆	Port P8 (P8)	0030 ₁₆	Timer A mode register (TAM)
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	Timer A control register (TACON)
0012 ₁₆		0032 ₁₆	A-D control register (ADCON)
0013 ₁₆		0033 ₁₆	A-D conversion register (low) (ADL)
0014 ₁₆		0034 ₁₆	A-D conversion register (high) (ADH)
0015 ₁₆		0035 ₁₆	
0016 ₁₆	PULL register A (PULLA)	0036 ₁₆	
0017 ₁₆	PULL register B (PULLB)	0037 ₁₆	
0018 ₁₆	Port P8 output selection register (P8SEL)	0038 ₁₆	Segment output enable register (SEG)
0019 ₁₆	Serial I/O control register 1 (SIOCON1)	0039 ₁₆	LCD mode register (LM)
001A ₁₆	Serial I/O control register 2 (SIOCON2)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	Serial I/O register (SIO)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆		003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆		003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆		003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆		003F ₁₆	Interrupt control register 2 (ICON2)
0F01 ₁₆	ROM correct enable register 1 (Note)	0F0A ₁₆	ROM correct high-order address register 5 (Note)
0F02 ₁₆	ROM correct high-order address register 1 (Note)	0F0B ₁₆	ROM correct low-order address register 5 (Note)
0F03 ₁₆	ROM correct low-order address register 1 (Note)	0F0C ₁₆	ROM correct high-order address register 6 (Note)
0F04 ₁₆	ROM correct high-order address register 2 (Note)	0F0D ₁₆	ROM correct low-order address register 6 (Note)
0F05 ₁₆	ROM correct low-order address register 2 (Note)	0F0E ₁₆	ROM correct high-order address register 7 (Note)
0F06 ₁₆	ROM correct high-order address register 3 (Note)	0F0F ₁₆	ROM correct low-order address register 7 (Note)
0F07 ₁₆	ROM correct low-order address register 3 (Note)	0F10 ₁₆	ROM correct high-order address register 8 (Note)
0F08 ₁₆	ROM correct high-order address register 4 (Note)	0F11 ₁₆	ROM correct low-order address register 8 (Note)
0F09 ₁₆	ROM correct low-order address register 4 (Note)		

Note: This register is valid only in mask ROM version.

Fig. 7 Memory map of special function register (SFR)

I/O PORTS

[Direction Registers (ports P2, P4, P50, P52–P57, and P6–P8)]

The I/O ports P2, P4, P50, P52–P57, and P6–P8 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

[Direction Registers (ports P0 and P1)]

Ports P0 and P1 have direction registers which determine the input/output direction of each individual port.

Each port in a direction register corresponds to one port, each port can be set to be input or output.

When "0" is written to the bit 0 of a direction register, that port becomes an input port. When "1" is written to that port, that port becomes an output port. Bits 1 to 7 of ports P0 and P1 direction registers are not used.

Pull-up/Pull-down Control

By setting the PULL register A (address 0016₁₆) or the PULL register B (address 0017₁₆), ports except for ports P3 and P5₁ can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.

Port P8 Output Selection

Ports P8₀ to P8₇ can be switched to N-channel open-drain output by setting "1" to the port P8 output selection register.

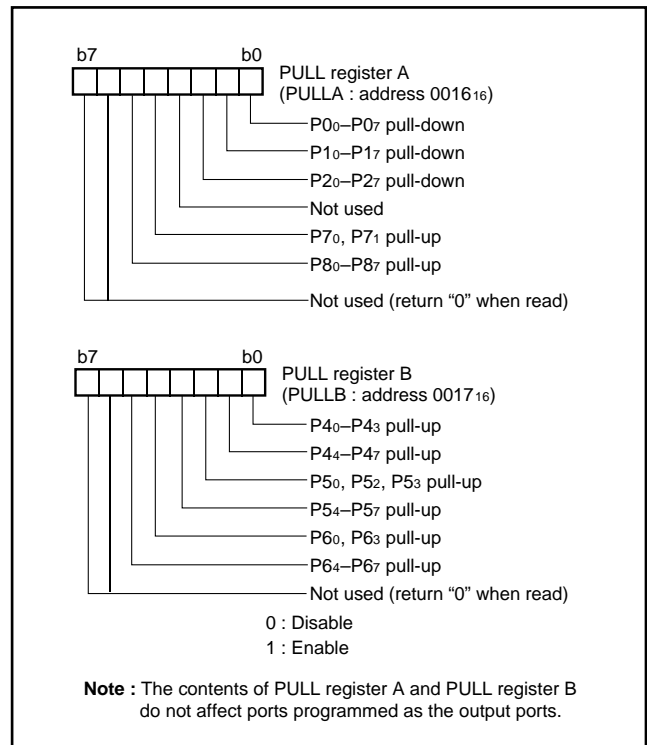


Fig. 8 Structure of PULL register A and PULL register B

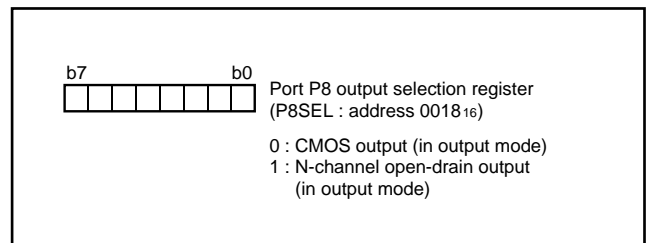


Fig. 9 Structure of port P8 output selection register

Table 4 List of I/O port function (1)

Pin	Name	Input/Output	I/O format	Non-port function	Related SFRs	Ref. No.
P0 ₀ /SEG ₈ – P0 ₇ /SEG ₁₅	Port P0	Input/Output, port unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P1 ₀ /SEG ₁₆ – P1 ₇ /SEG ₂₃	Port P1	Input/Output, port unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	
P2 ₀ /SEG ₀ – P2 ₇ /SEG ₇	Port P2	Input/Output, individual bits	CMOS compatible input CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	
P3 ₀ /SEG ₂₄ – P3 ₇ /SEG ₃₁	Port P3	Output, individual bits	CMOS 3-state output	LCD segment output	Segment output enable register	(2)

Table 5 List of I/O port function (2)

Pin	Name	Input/Output	I/O format	Non-port function	Related SFRs	Ref. No.		
P40/SCLK2	Port P4	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O function I/O	Serial I/O control registers 1, 2 PULL register B	(3)		
P41/T1OUT				Timer output	Timer 12 mode register PULL register B	(4)		
P42/T3OUT				Timer output	Timer 34 mode register PULL register B	(4)		
P43/ ϕ				ϕ clock output	ϕ output control register PULL register B	(5)		
P44/SIN P45/SOUT P46/SCLK1 P47/SRDY				Serial I/O function I/O	Serial I/O control registers 1, 2 PULL register B	(6)		
						(7)		
			(8)					
			(9)					
P50/TAOUT	Port P5	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Timer A output	Timer A mode register Timer A control register PULL register B	(10)		
P51				Input	CMOS compatible input level		(11)	
P52/PWM1				Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	PWM output	Timer 56 mode register PULL register B	(4)
P53/CNTR0 P54/CNTR1						External count I/O	Interrupt edge selection register PULL register B	(12)
						External interrupt input	Interrupt edge selection register PULL register B	(12)
P60/AN0 – P67/AN7	Port P6	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	A-D converter input	A-D control register PULL register B	(13)		
P70/XCIN	Port P7	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	CPU mode register PULL register A	(14)		
P71/XCOUT						(15)		
P80 – P87	Port P8	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	Interrupt control register 2 PULL register A	(17)		
COM0 – COM3	Common	Output	LCD common output		LCD mode register	(16)		

Notes 1: Make sure that the input level at each pin is either 0 V or Vcc during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

2: For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double function ports as function I/O ports, refer to the applicable sections.

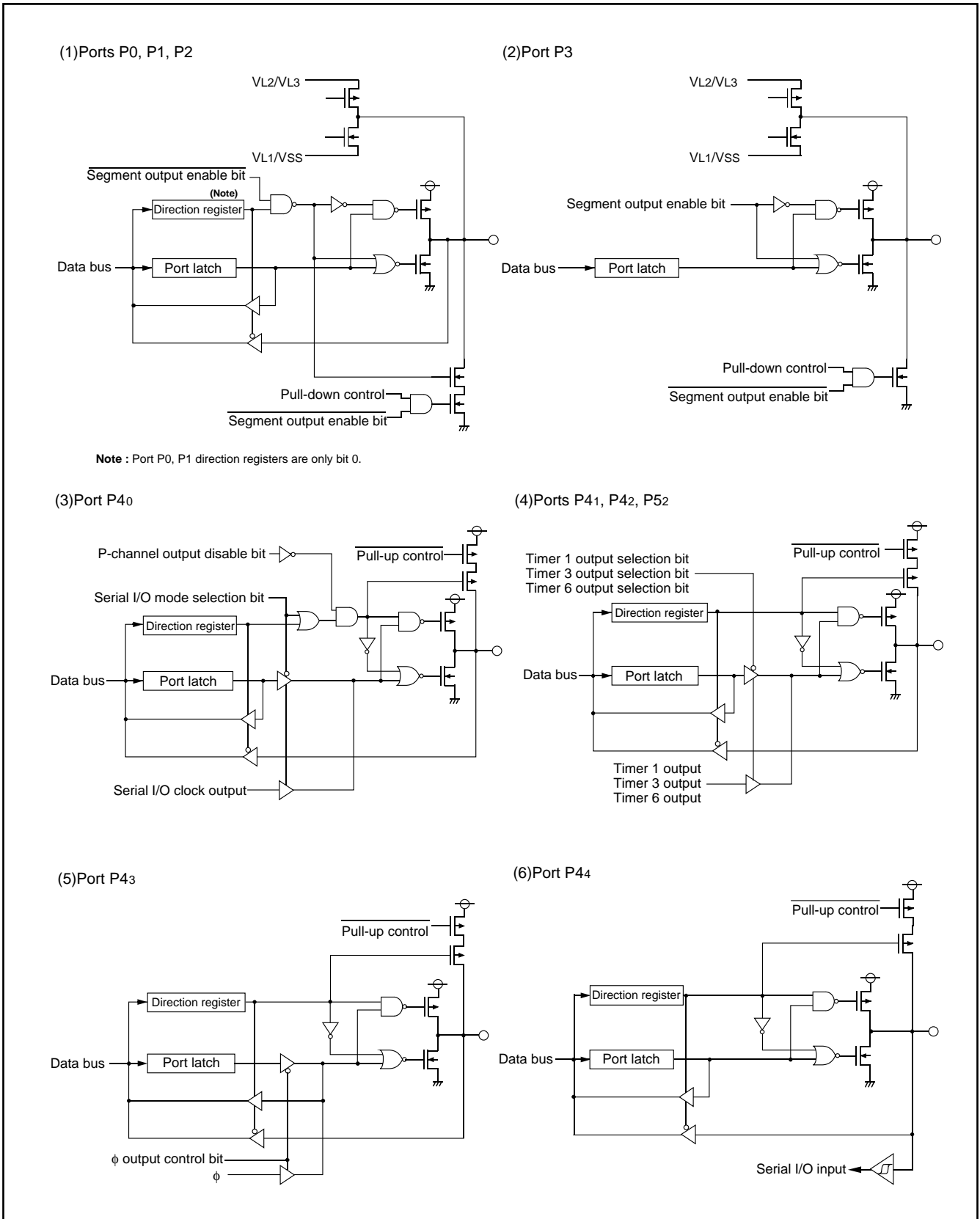


Fig. 10 Port block diagram (1)

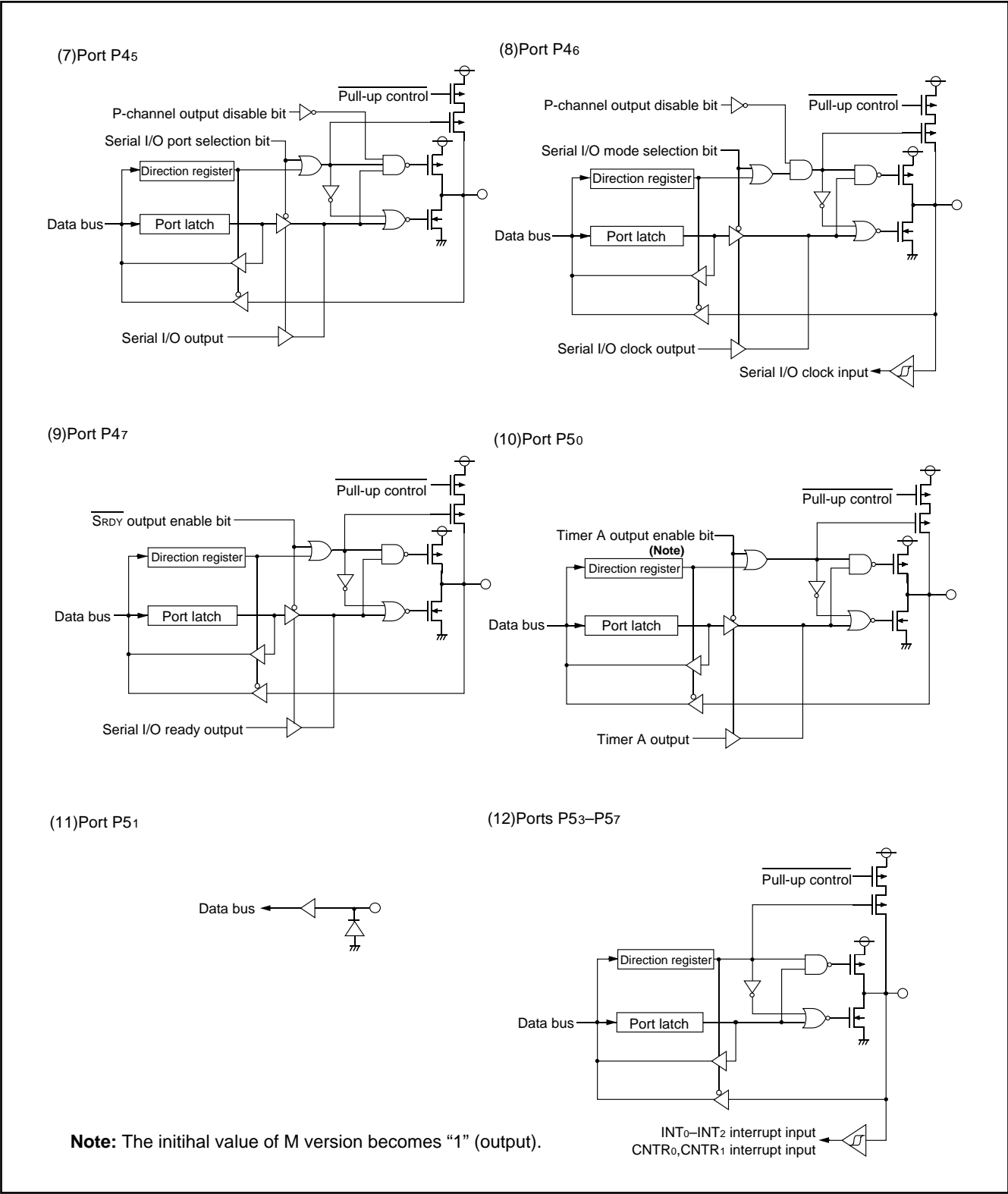


Fig. 11 Port block diagram (2)

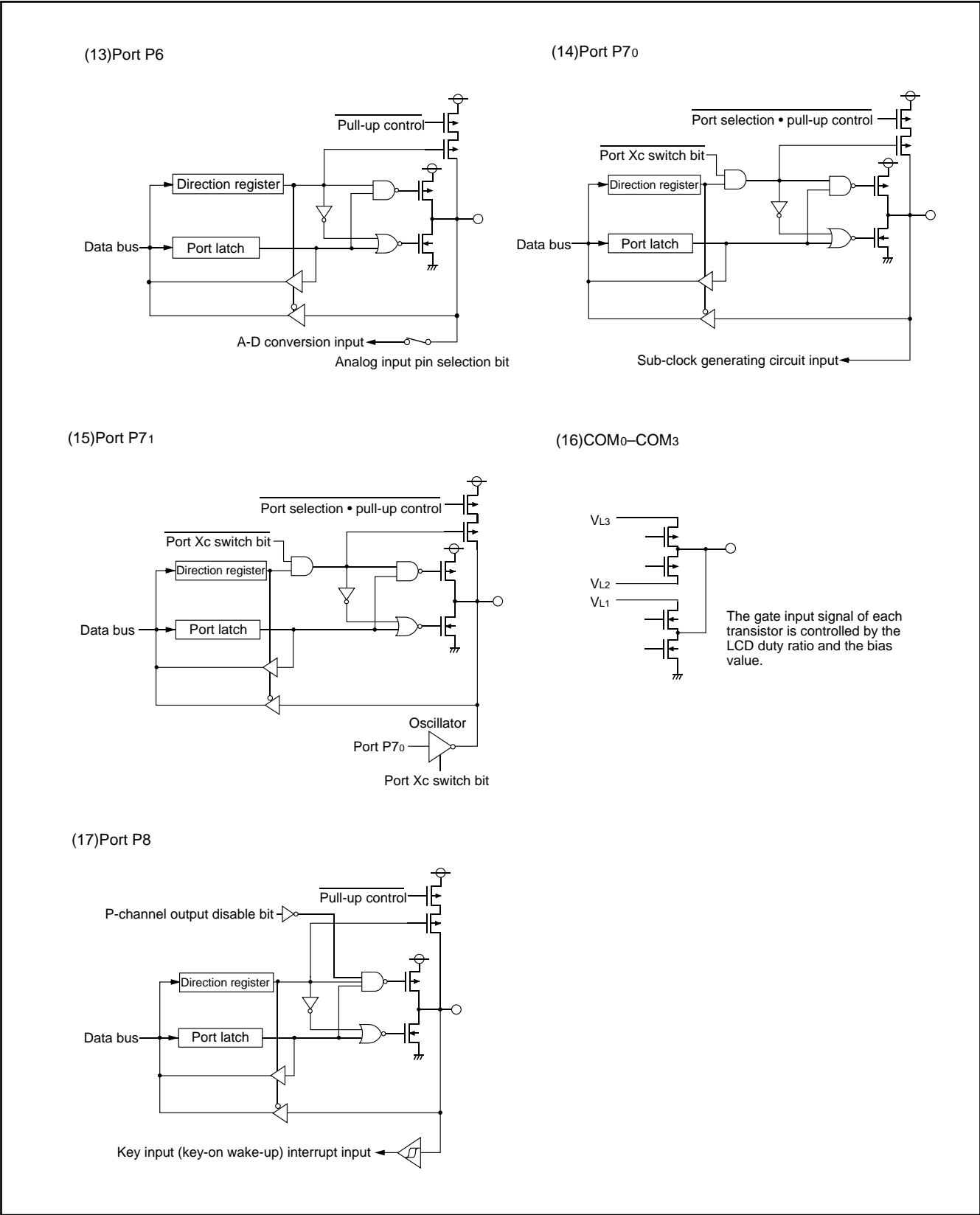


Fig. 12 Port block diagram (3)

INTERRUPTS

Interrupts occur by sixteen sources: six external, nine internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on Interrupts

When the active edge of an external interrupt (INT₀ – INT₂, CNTR₀ or CNTR₁) is set or an vector interrupt source where several interrupt source is assigned to the same vector address is switched, the corresponding interrupt request bit may also be set. Therefore, take following sequence:

- (1) Disable the interrupt.
- (2) Change the active edge in interrupt edge selection register.
- (3) Clear the set interrupt request bit to "0."
- (4) Enable the interrupt.

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
INT ₁	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
INT ₂	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT ₂ input	External interrupt (active edge selectable)
Serial I/O	5	FFF5 ₁₆	FFF4 ₁₆	At completion of serial I/O data transmit/receive	Valid when serial I/O is selected
Timer A	6	FFF3 ₁₆	FFF2 ₁₆	At timer A underflow	
Timer 1	7	FFF1 ₁₆	FFF0 ₁₆	At timer 1 underflow	
Timer 2	8	FFEF ₁₆	FFEE ₁₆	At timer 2 underflow	STP release timer underflow
Timer 3	9	FFED ₁₆	FFEC ₁₆	At timer 3 underflow	
Timer 4	10	FFEB ₁₆	FFEA ₁₆	At timer 4 underflow	
Timer 5	11	FFE9 ₁₆	FFE8 ₁₆	At timer 5 underflow	
Timer 6	12	FFE7 ₁₆	FFE6 ₁₆	At timer 6 underflow	
CNTR ₀	13	FFE5 ₁₆	FFE4 ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
CNTR ₁	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of CNTR ₁ input	External interrupt (active edge selectable)
Key input (Key-on wake-up)	15	FFE1 ₁₆	FFE0 ₁₆	At falling of port P8 (at input) input logical level AND	External interrupt (falling valid)
A-D conversion	16	FFDF ₁₆	FFDE ₁₆	At completion of A-D conversion	Valid when A-D conversion interrupt is selected
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

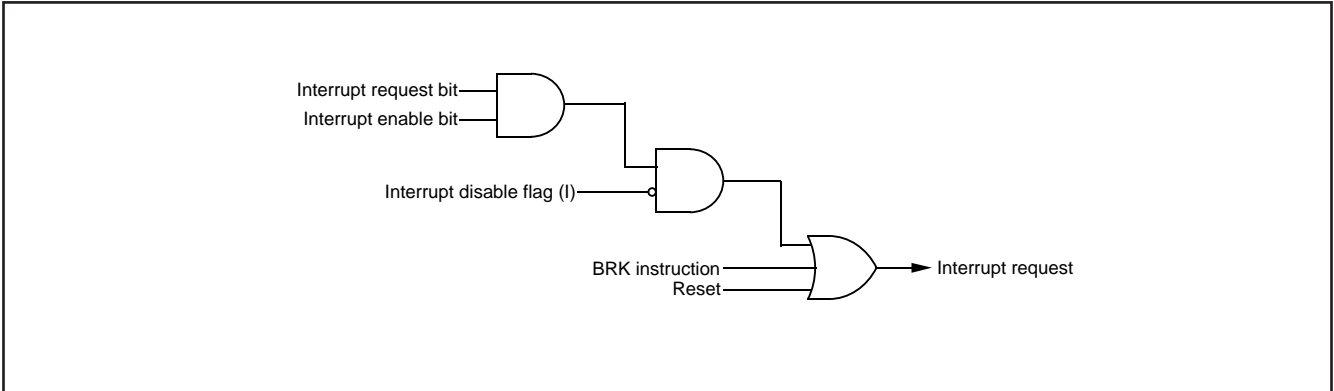


Fig. 13 Interrupt control

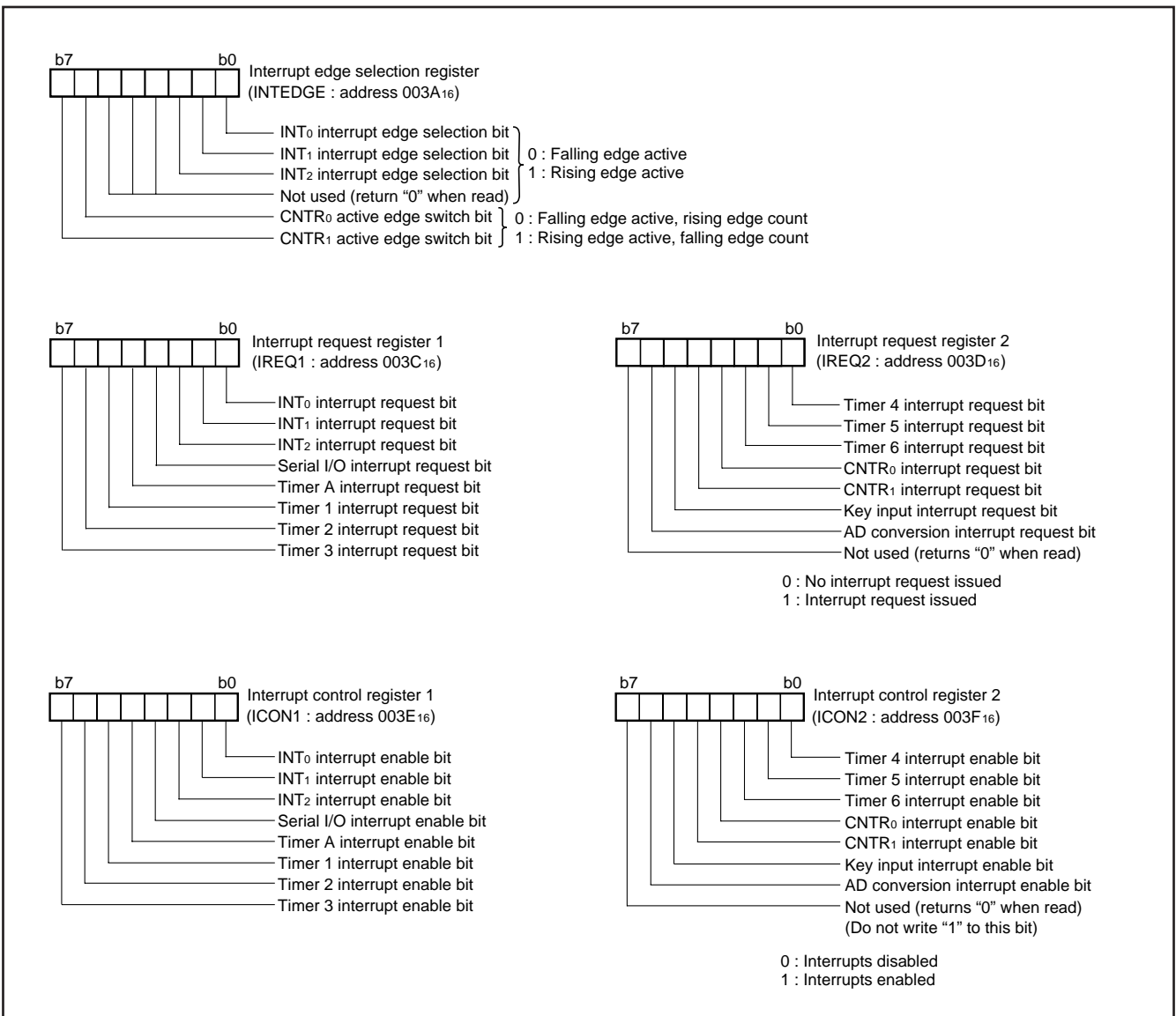


Fig. 14 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by applying "L" level to any pin of port P8 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example

of using a key input interrupt is shown in Figure 15, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P80–P83.

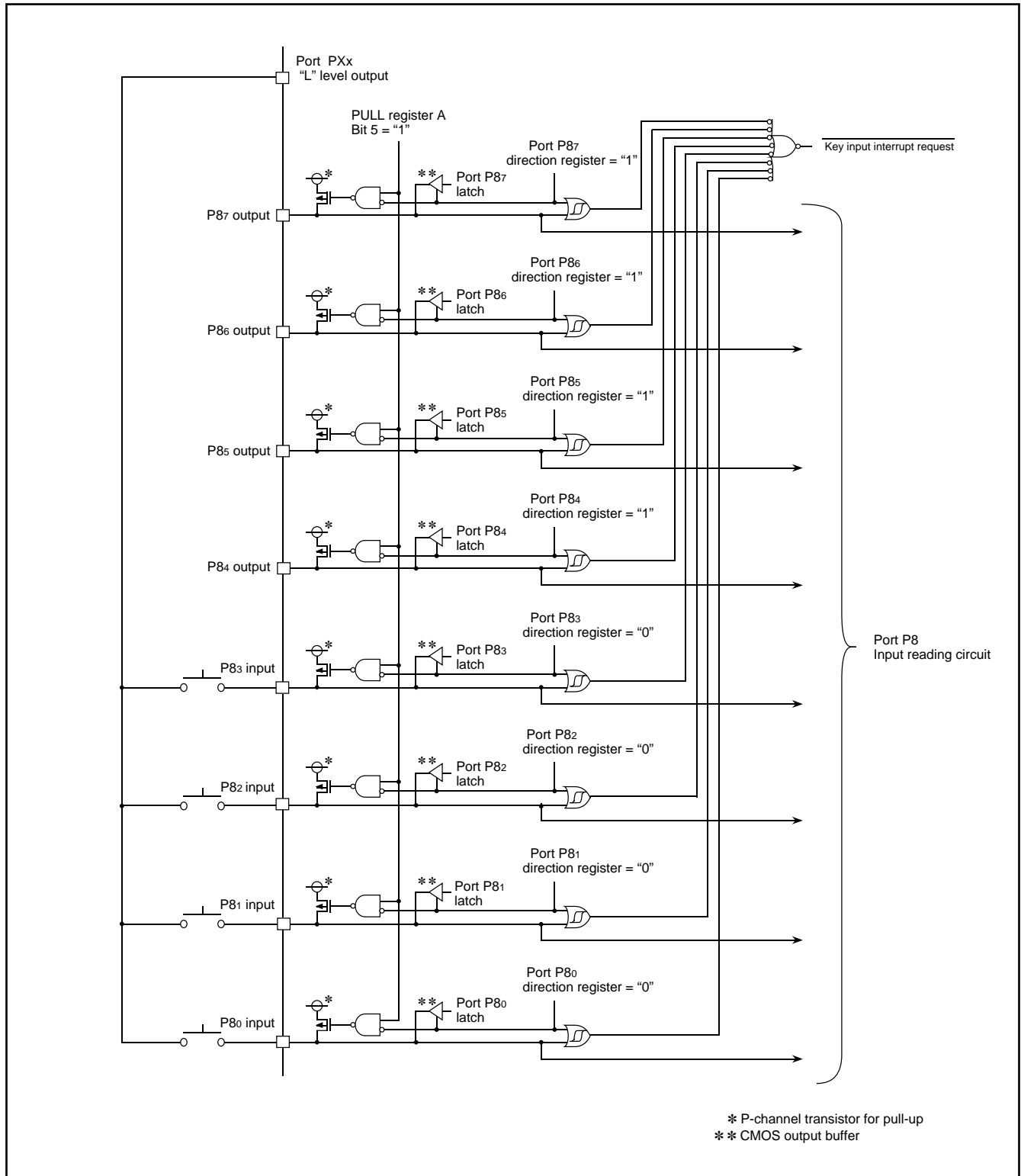


Fig. 15 Connection example when using key input interrupt and port P8 block diagram

TIMERS

8-Bit Timer

The 38C3 group has six built-in timers : Timer 1, Timer 2, Timer 3, Timer 4, Timer 5, and Timer 6.

Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches "0016," an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1."

The count can be stopped by setting the stop bit of each timer to "1." The system clock ϕ can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, timer internal count source is switched to either $f(X_{IN})$ or $f(X_{CIN})$.

●**Timer 1, Timer 2**

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 is output from the P41/T1OUT pin. The waveform polarity changes each time timer 1 overflows. The active edge of the external clock CNTR0 can be switched with the bit 6 of the interrupt edge selection register.

At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0," timer 1 is set to "FF16," and timer 2 is set to "0116."

●**Timer 3, Timer 4**

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 is output from the P42/T3OUT pin. The waveform polarity changes each time timer 3 overflows. The active edge of the external clock CNTR1 can be switched with the bit 7 of the interrupt edge selection register.

●**Timer 5, Timer 6**

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register. A rectangular waveform of timer 6 underflow signal divided by 2 can be output from the P52/PWM1 pin.

●**Timer 6 PWM1 Mode**

Timer 6 can output a rectangular waveform with "H" duty cycle $n/(n+m)$ from the P52/PWM1 pin by setting the timer 56 mode register (refer to Figure 17). The n is the value set in timer 6 latch (address 002516) and m is the value in the timer 6 PWM register (address 002716). If n is "0," the PWM output is "L," if m is "0," the PWM output is "H" (n = 0 is prior than m = 0). In the PWM mode, interrupts occur at the rising edge of the PWM output.

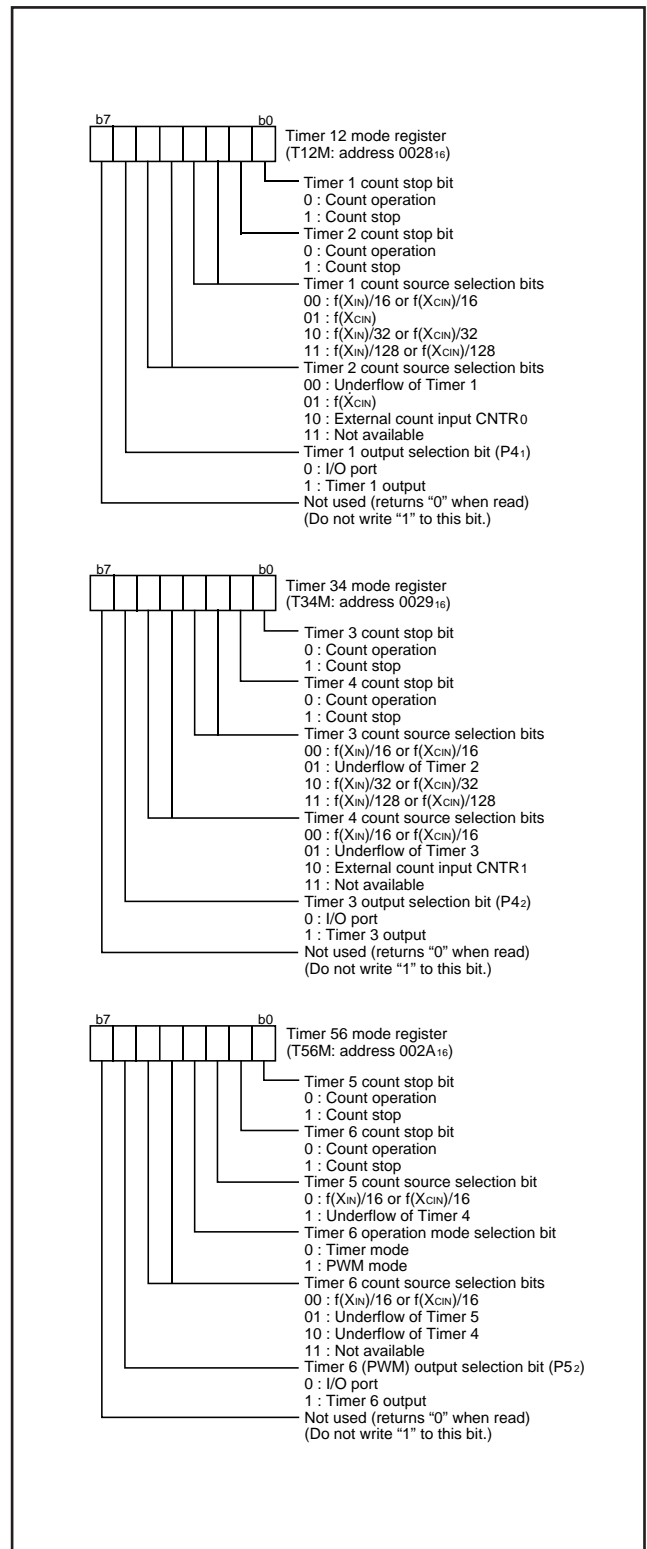


Fig. 16 Structure of Timer Related Register

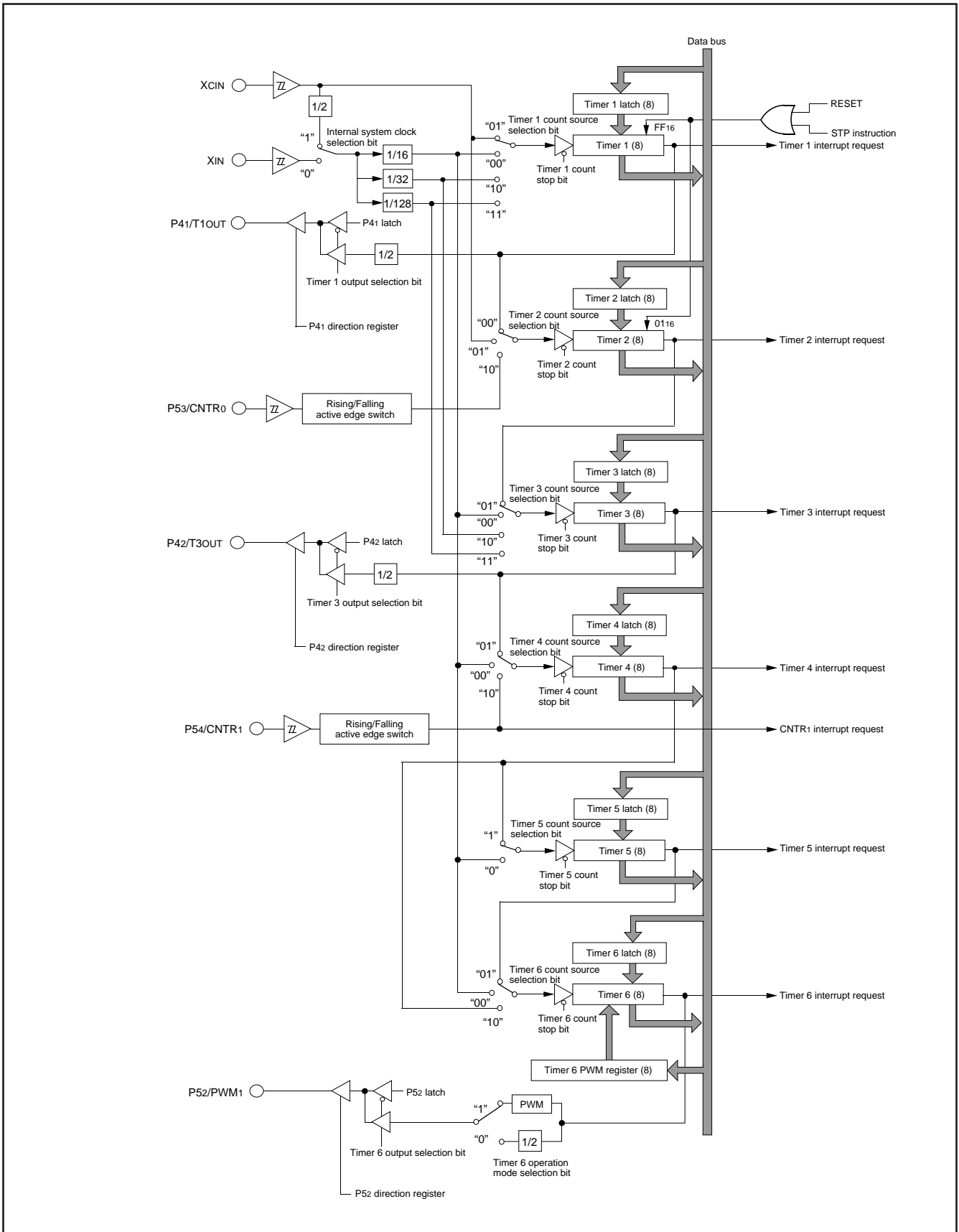


Fig. 17 Block diagram of timer

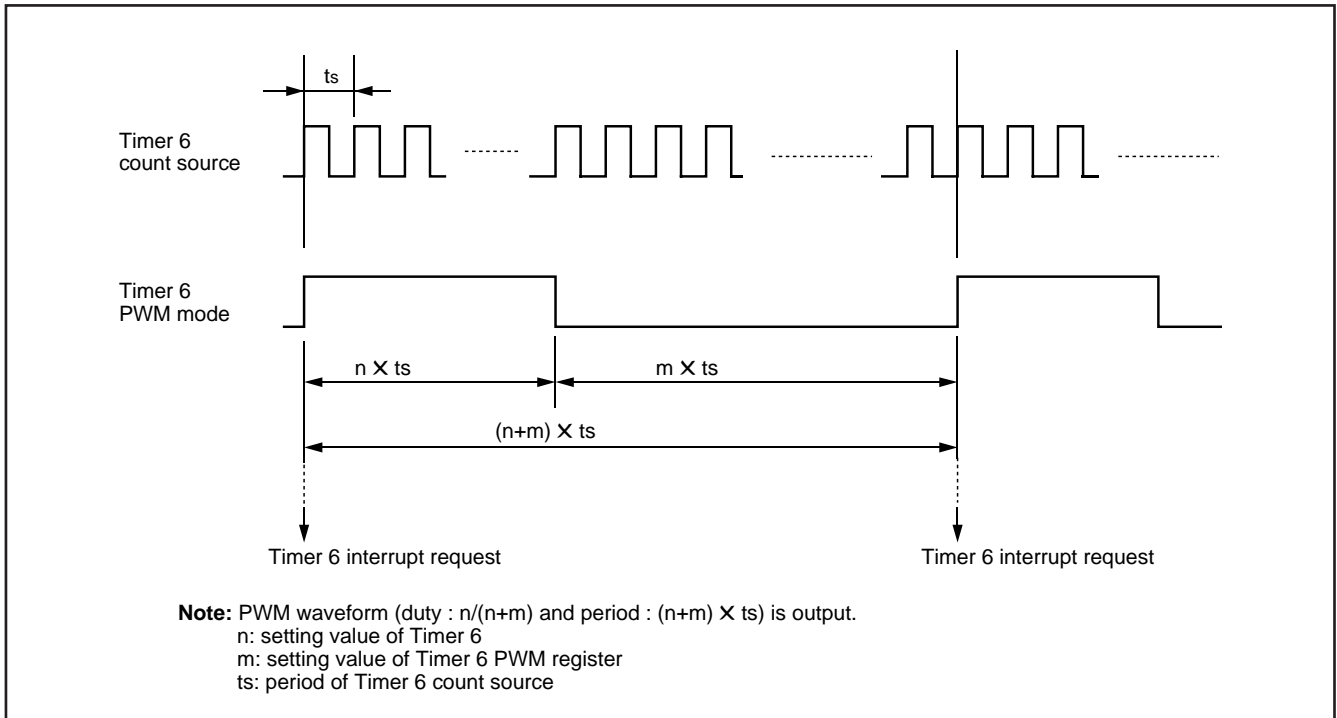


Fig. 18 Timing chart of timer 6 PWM1 mode

16-bit Timer

Timer A is a 16-bit timer that can be selected in one of four modes by the timer A mode register and the timer A control register.

●Timer A

The timer A operates as down-count. When the timer contents reach "000016", an underflow occurs at the next count pulse and the timer latch contents are reloaded. After that, the timer continues count-down. When the timer underflows, the interrupt request bit corresponding to the timer A is set to "1".

(1) Timer mode

The count source can be selected by setting the timer A mode register.

(2) Pulse output mode

Pulses of which polarity is inverted each time the timer underflows are output from the TAOUT pin. Except for that, this mode operates just as in the timer mode.

When using this mode, set port P50 sharing the TAOUT pin to output mode.

(3) IGBT output mode

After dummy output from the TAOUT pin, count starts with the INT0 pin input as a trigger. When the trigger is detected or the timer A underflows, "H" is output from the the TAOUT pin.

When the count value corresponds with the compare register value, the TAOUT output becomes "L". When the INT0 signal becomes "H", the TAOUT output is forced to become "L".

After noise is cleared by noise filters, judging continuous 4-time same levels with sampling clocks to be signals, the INT0 signal can use 4

types of delay time by a delay circuit.

When using this mode, set port P55 sharing the INT0 pin to input mode and set port P50 sharing the TAOUT pin to output mode.

It is possible to force the timer A output to be "L" using pins INT1 and INT2 by the timer A control register.

(4) PWM mode

IGBT dummy output, an external trigger with the INT0 pin and output control with pins INT1 and INT2 are not used. Except for those, this mode operates just as in the IGBT output mode.

The period of PWM waveform is specified by the timer A set value. The "H" term is specified by the compare register set value.

When using this mode, set port P50 sharing the TAOUT pin to output mode.

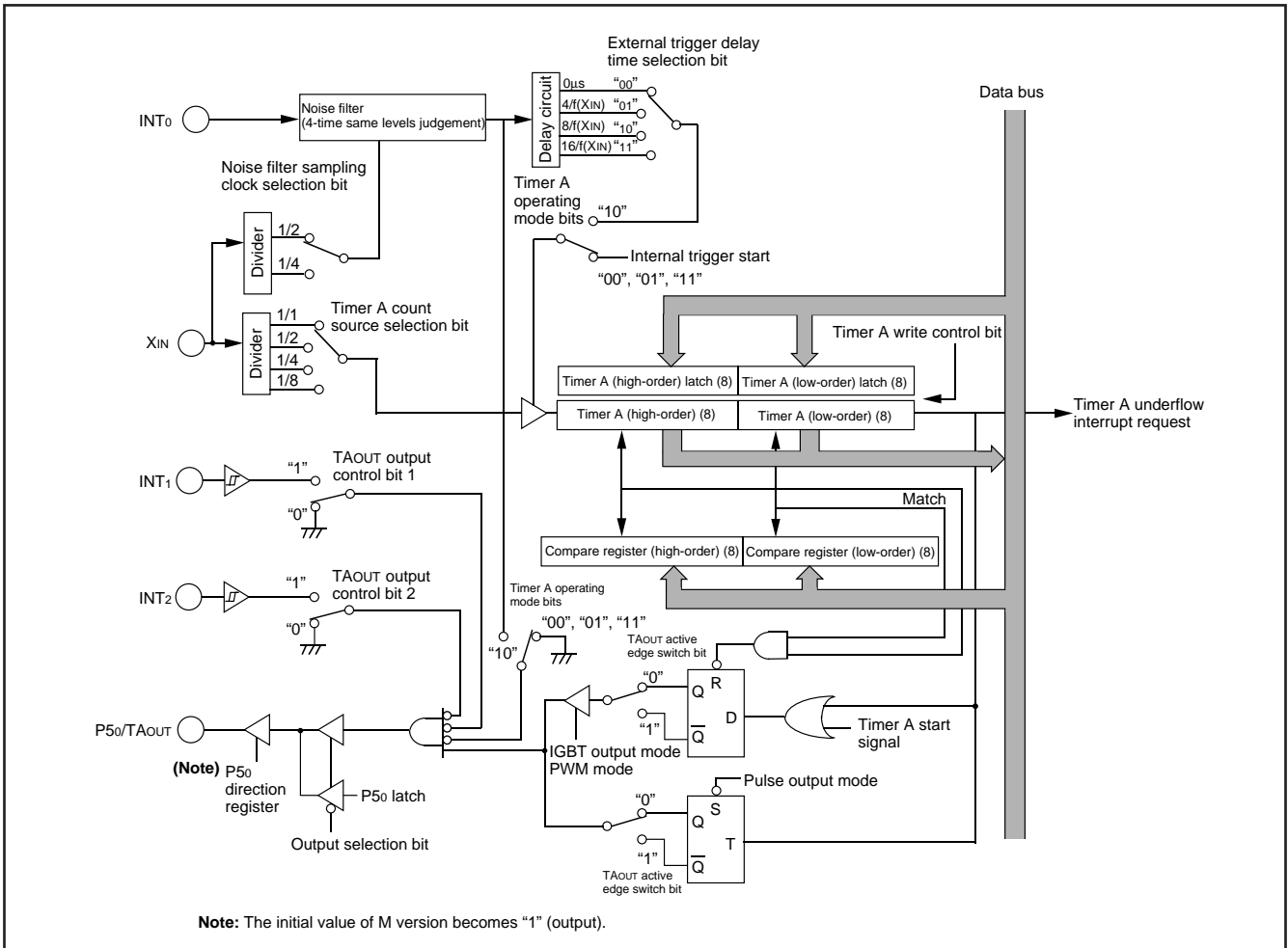


Fig. 19 Block diagram of timer A

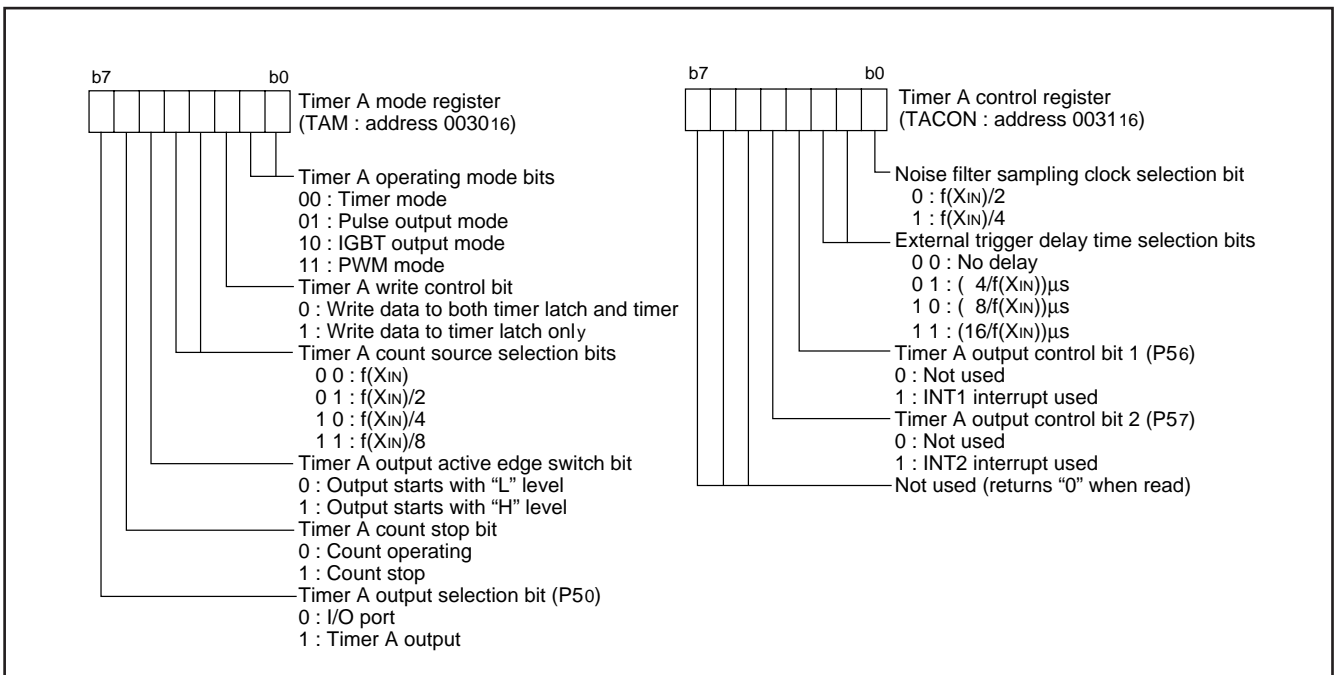


Fig. 20 Structure of timer A related registers

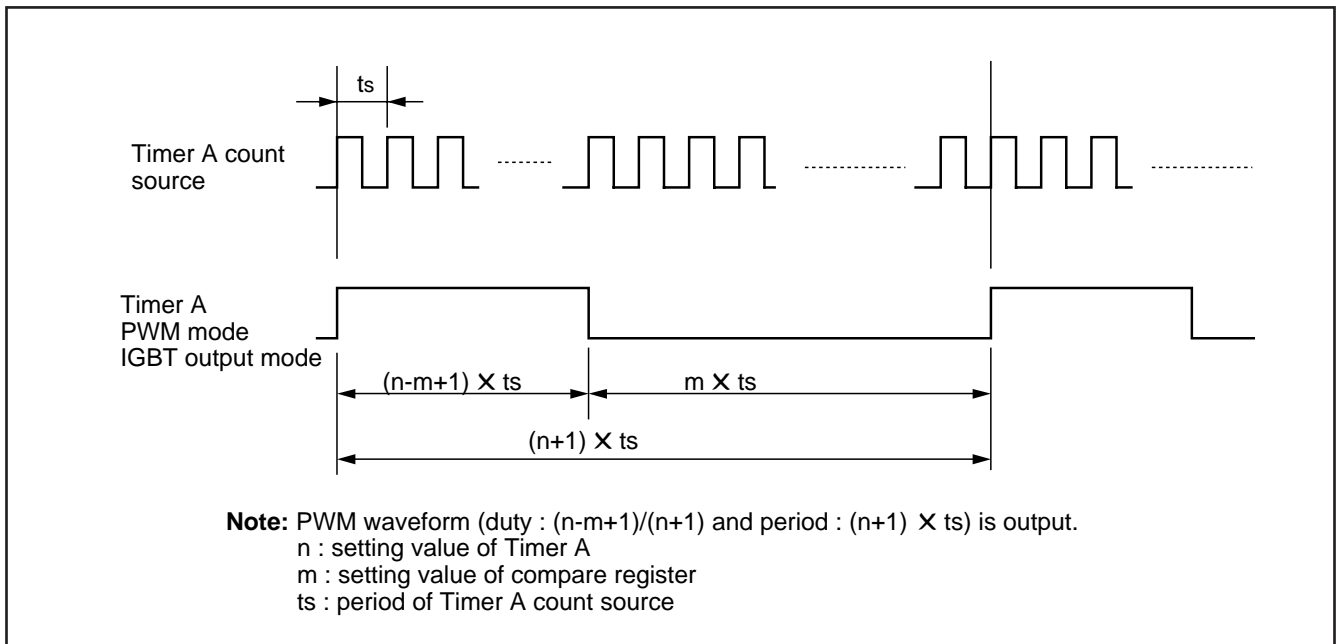


Fig. 21 Timing chart of timer A PWM, IGBT output modes

■Notes on Timer A

(1) Write order to timer A

- In the timer and pulse output modes, write to the timer A register (low-order) first and to the timer A register (high-order) next. Do not write to only one side.
- In the IGBT and PWM modes, write to the registers as follows:
 the compare register (high- and low-order)
 the timer A register (low-order)
 the timer A register (high-order).
 It is possible to use whichever order to write to the compare register (high- and low-order). However, write both the compare register and the timer A register at the same time.

(2) Read order to timer A

- In all modes, read to the timer A register (high-order) first and to the timer A register (low-order) next. Read order to the compare register is not specified.
- If reading to the timer A register during write operation or writing to it during read operation, normal operation will not be performed.

(3) Write to timer A

- When writing a value to the timer A address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. Normally, when writing a value to the timer A address, the value is set into the timer and the timer latch at the same time, because they are written at the same time.
 When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, an expected value may be set in the high-order counter.
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it. Additionally, when performing write to the latch and the timer at the same time, the timer count value may change large.

(4) Set of timer A mode register

Set the write control bit to "1" (write to the latch only) when setting the IGBT and PWM modes.

Output waveform simultaneously reflects the contents of both registers at the next underflow after writing to the timer A register (high-order).

(5) Output control function of timer A

When using the output control function (INT1 and INT2) in the IGBT mode, set the levels of INT1 and INT2 to "H" in the falling edge active or to "L" in the rising edge active before switching to the IGBT mode.

SERIAL I/O

The 38C3 group has a built-in 8-bit clock synchronous serial I/O. The

I/O pins of serial I/O also operate as I/O port P4, and their function is selected by the serial I/O control register 1 (address 001916).

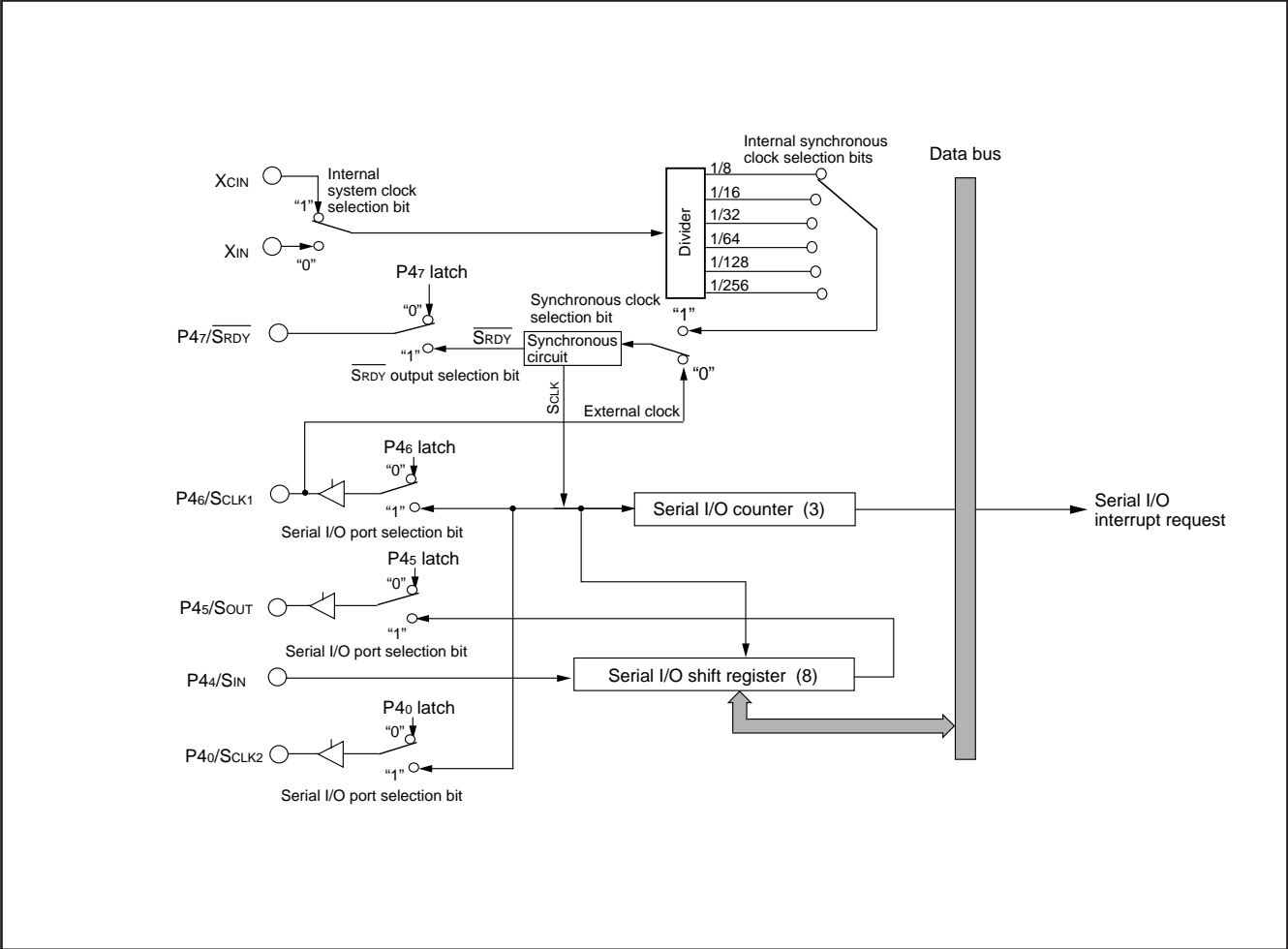


Fig. 22 Block diagram of serial I/O

[Serial I/O Control Registers 1, 2 (SIOCON1, SIOCON2)] 0019₁₆, 001A₁₆

Each of the serial I/O control registers 1, 2 contains 8 bits that select various control parameters of serial I/O.

●Operation in serial I/O mode

Either an internal clock or an external clock can be selected as the synchronous clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.

When internal clock is selected, serial I/O starts to transfer by a write signal to the serial I/O register (address 001B₁₆). After 8 bits have been transferred, the SOUT pin goes to high impedance.

When external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, the SOUT pin does not go to high impedance at the completion of data transfer.

The interrupt request bit is set at the end of the transfer of 8 bits, regardless of whether the internal or external clock is selected.

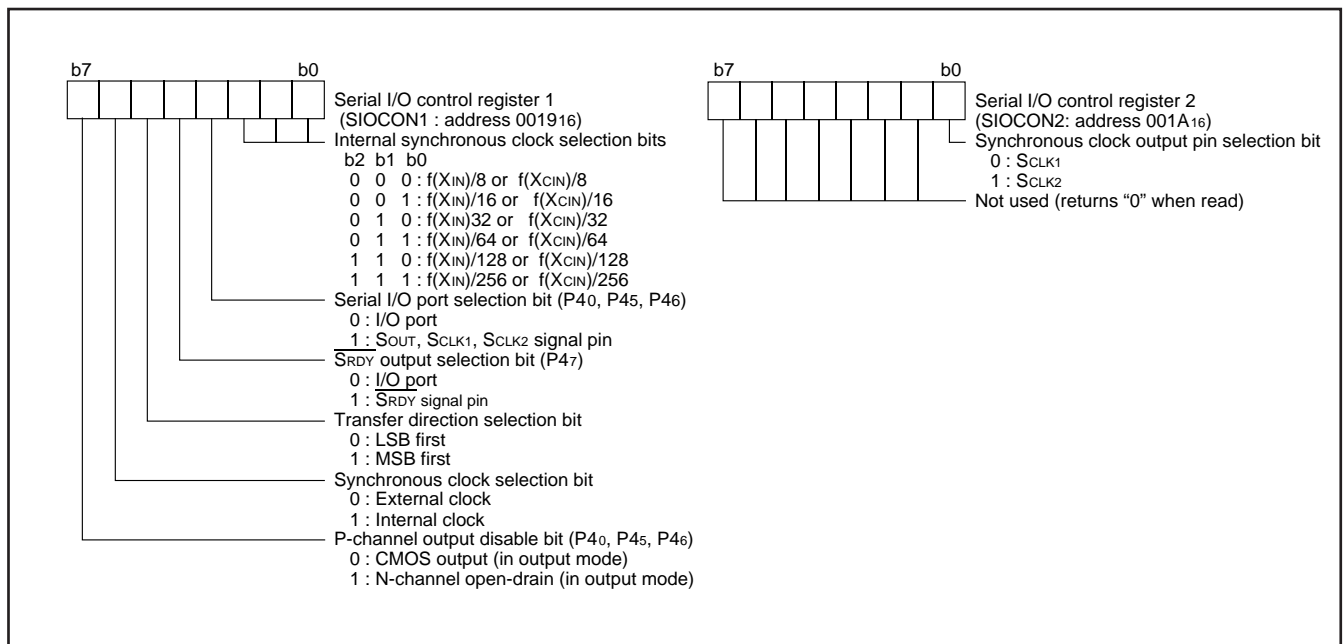


Fig. 23 Structure of serial I/O control register

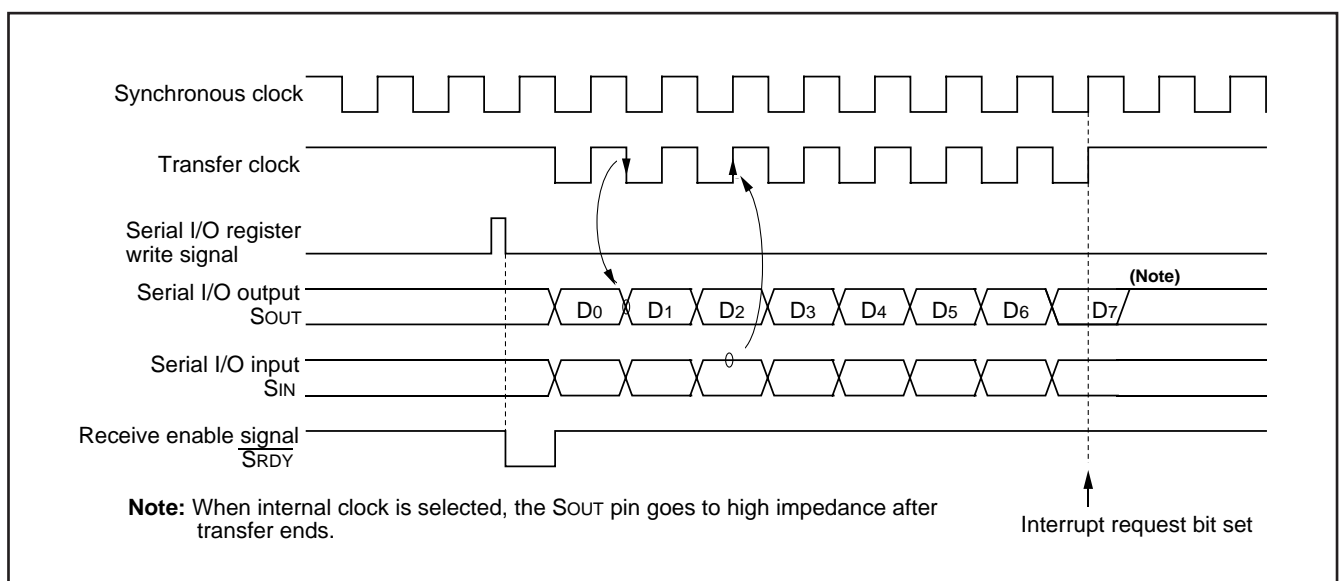


Fig. 24 Serial I/O timing (for LSB first)

A-D CONVERTER

The 38C3 group has a 10-bit A-D converter. The A-D converter performs successive approximation conversion.

[A-D Conversion Register (AD)] 003316, 003416

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A-D conversion register (high-order) (address 003416), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion register (low-order) (address 003316).

During A-D conversion, do not read these registers.

[A-D Control Register (ADCON)] 003216

This register controls A-D converter. Bits 2 to 0 are analog input pin selection bits. Bit 4 is an AD conversion completion bit and "0" during A-D conversion. This bit is set to "1" upon completion of A-D conversion.

A-D conversion is started by setting "0" in this bit.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AVSS and VREF, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports P67/AN7–P60/AN0 and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1."

Note that the comparator is constructed linked to a capacitor, so set $f(X_{IN})$ to at least 500 kHz during A-D conversion. Use a CPU system clock dividing the main clock X_{IN} as the internal system clock.

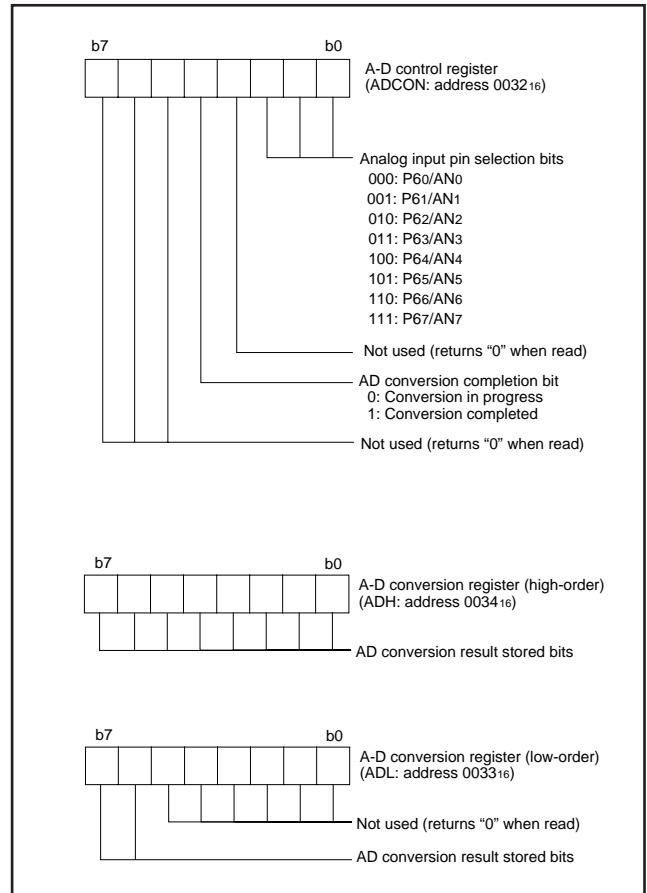


Fig. 25 Structure of A-D control register

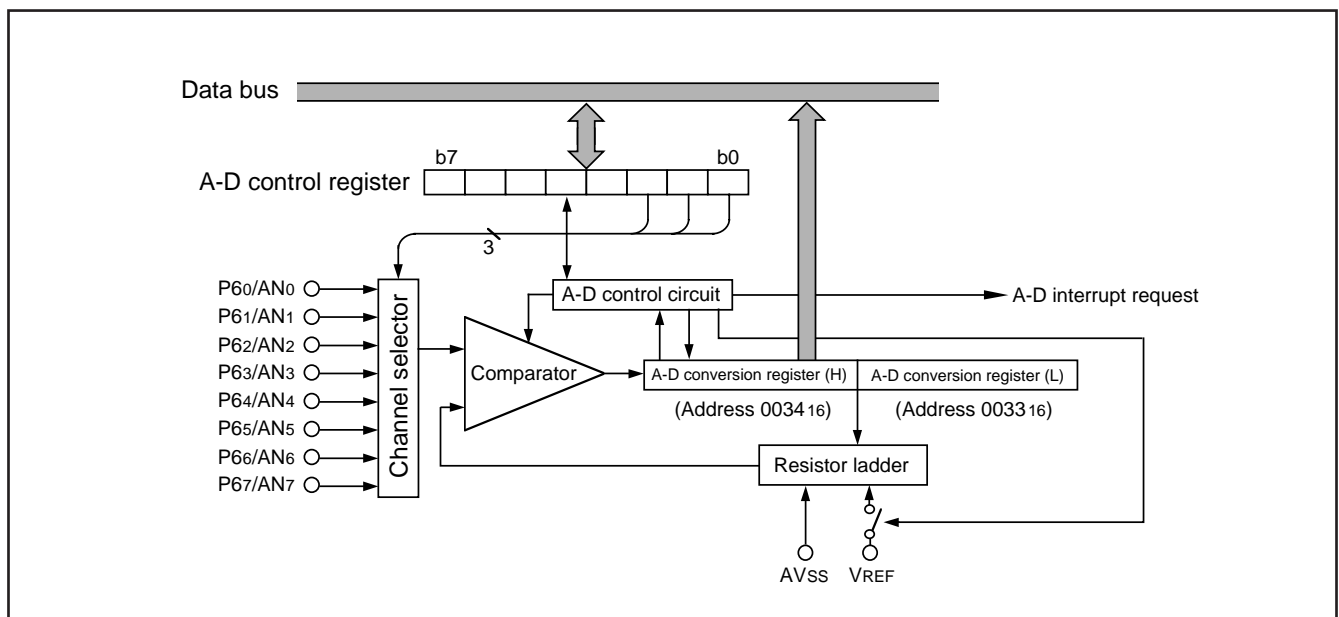


Fig. 26 Block diagram of A-D converter

LCD DRIVE CONTROL CIRCUIT

The 38C3 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output enable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 32 segment output pins and 4 common output pins can be used.

Up to 128 pixels can be controlled for a LCD display. When the LCD enable bit is set to "1" after data is set in the LCD mode register, the

segment output enable register, and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 7 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixels
1	32 dots or 8 segment LCD 4 digits
2	64 dots or 8 segment LCD 8 digits
3	96 dots or 8 segment LCD 12 digits
4	128 dots or 8 segment LCD 16 digits

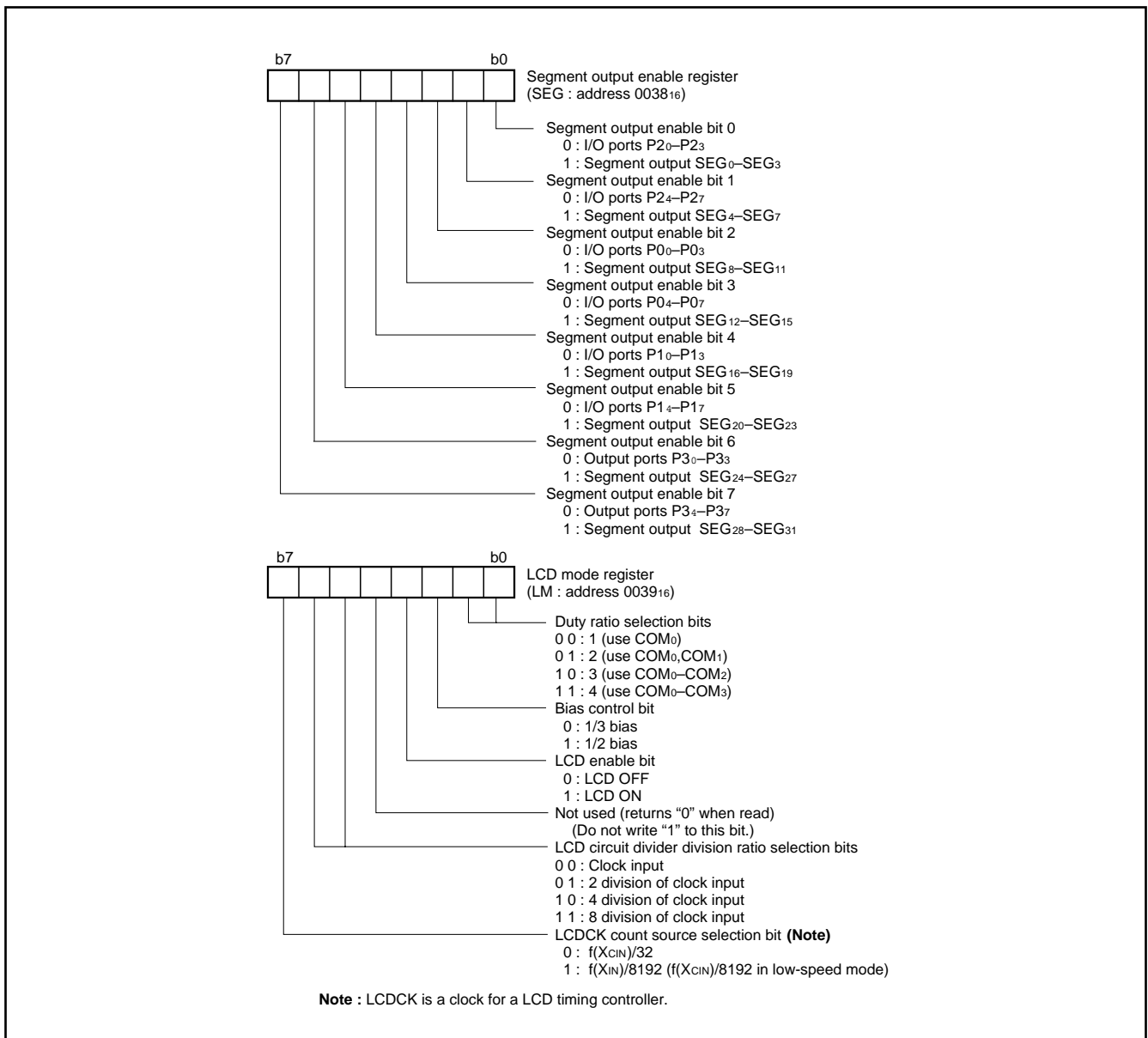


Fig. 27 Structure of LCD related registers

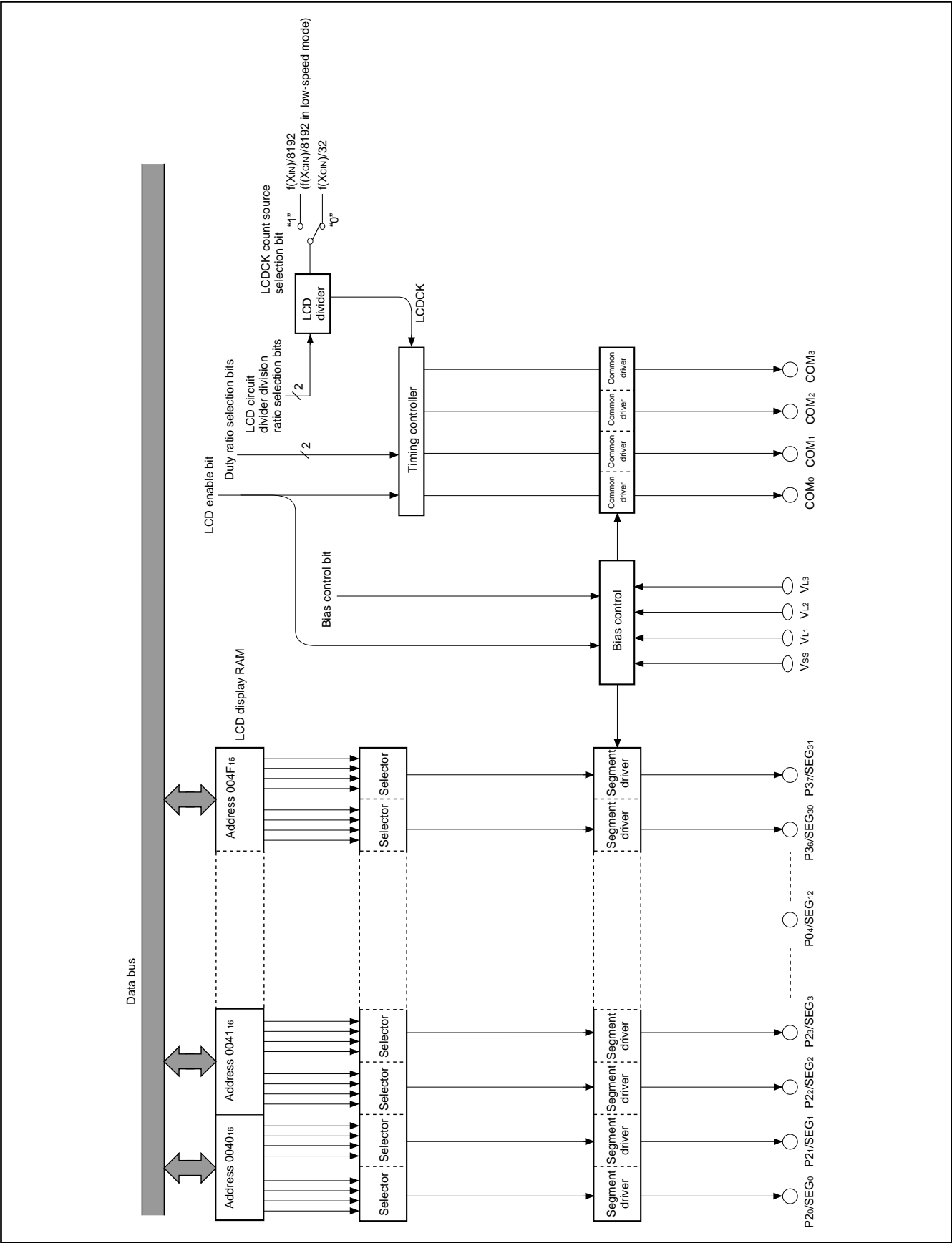


Fig. 28 Block diagram of LCD controller/driver

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (VL1–VL3), apply the voltage value shown in Table 8 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM0–COM3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

When selecting 1-duty ratio, 1/1 bias can be used.

Table 8 Bias control and applied voltage to VL1–VL3

Bias value	Voltage value
1/3 bias	VL3=VLCD VL2=2/3 VLCD VL1=1/3 VLCD
1/2 bias	VL3=VLCD VL2=VL1=1/2 VLCD
1/1 bias (1-duty ratio)	VL3=VLCD VL2=VL1=VSS

Note 1: VLCD is the maximum value of supplied voltage for the LCD panel.

Table 9 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
1	0	0	COM0 (Note 1)
2	0	1	COM0, COM1 (Note 2)
3	1	0	COM0–COM2 (Note 3)
4	1	1	COM0–COM3

Notes 1: COM1, COM2, and COM3 are open.

2: COM2 and COM3 are open.

3: COM3 is open.

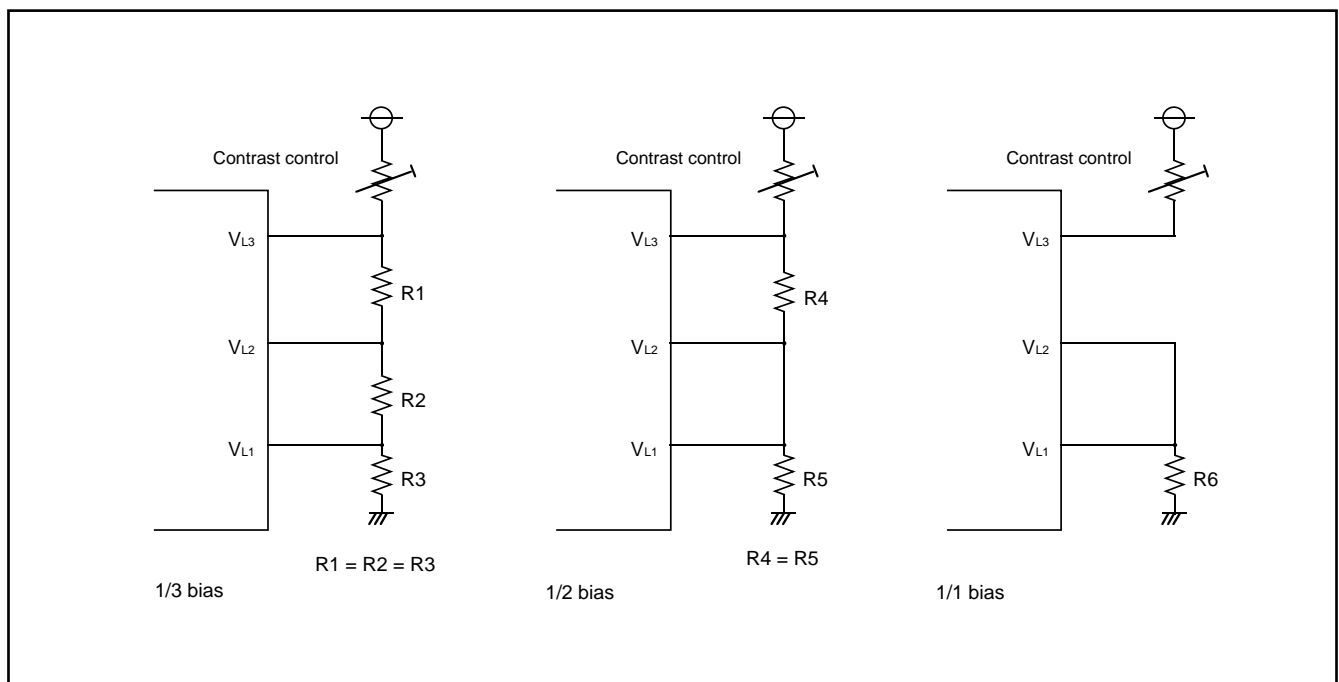


Fig. 29 Example of circuit at each bias

LCD Display RAM

Address 0040₁₆ to 004F₁₆ is the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{duty ratio}}$$

Address \ Bit	Bit							
	7	6	5	4	3	2	1	0
0040 ₁₆	SEG ₁				SEG ₀			
0041 ₁₆	SEG ₃				SEG ₂			
0042 ₁₆	SEG ₅				SEG ₄			
0043 ₁₆	SEG ₇				SEG ₆			
0044 ₁₆	SEG ₉				SEG ₈			
0045 ₁₆	SEG ₁₁				SEG ₁₀			
0046 ₁₆	SEG ₁₃				SEG ₁₂			
0047 ₁₆	SEG ₁₅				SEG ₁₄			
0048 ₁₆	SEG ₁₇				SEG ₁₆			
0049 ₁₆	SEG ₁₉				SEG ₁₈			
004A ₁₆	SEG ₂₁				SEG ₂₀			
004B ₁₆	SEG ₂₃				SEG ₂₂			
004C ₁₆	SEG ₂₅				SEG ₂₄			
004D ₁₆	SEG ₂₇				SEG ₂₆			
004E ₁₆	SEG ₂₉				SEG ₂₈			
004F ₁₆	SEG ₃₁				SEG ₃₀			
	COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀

Fig. 30 LCD display RAM map

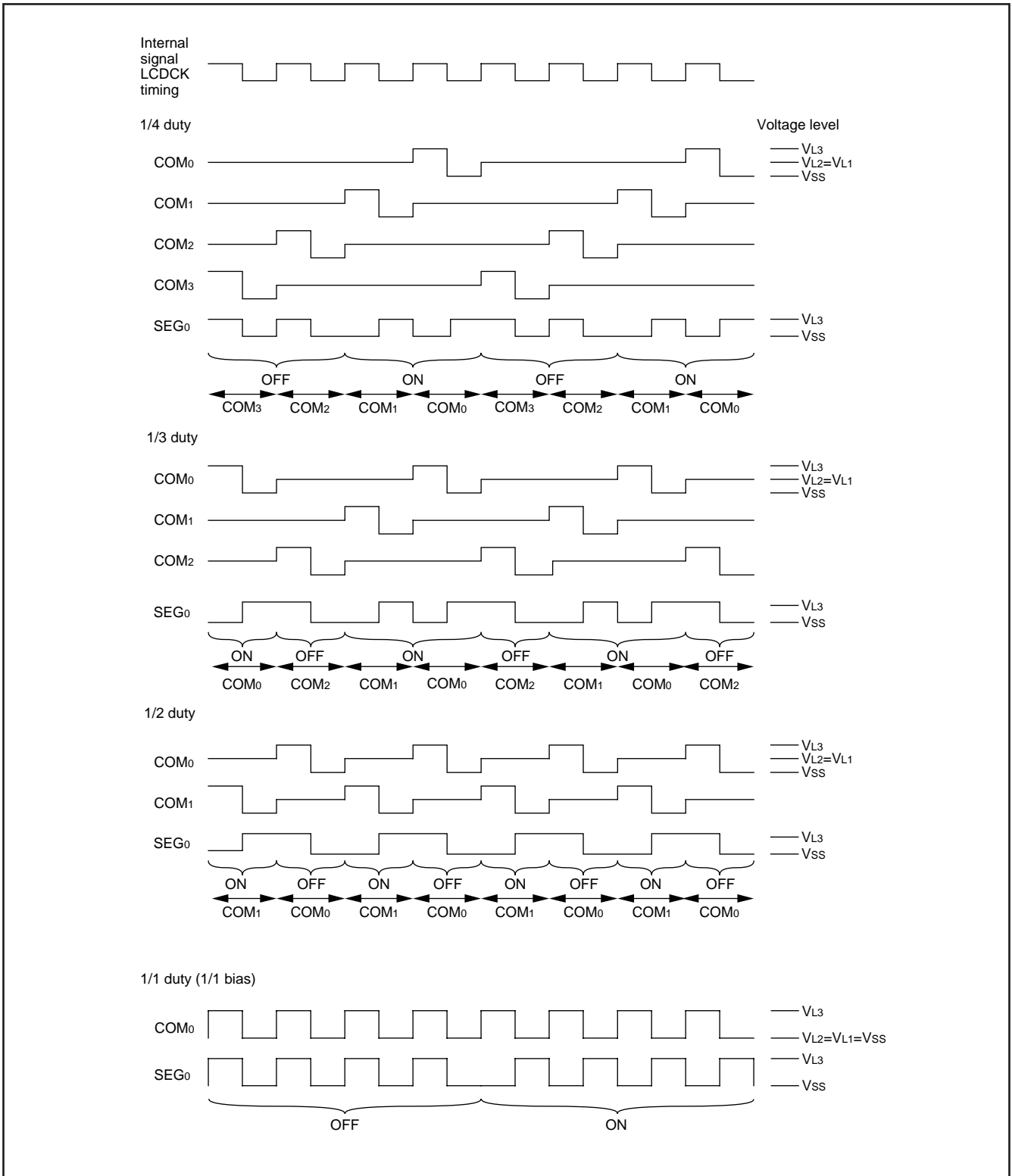


Fig. 31 LCD drive waveform (1/2 bias)

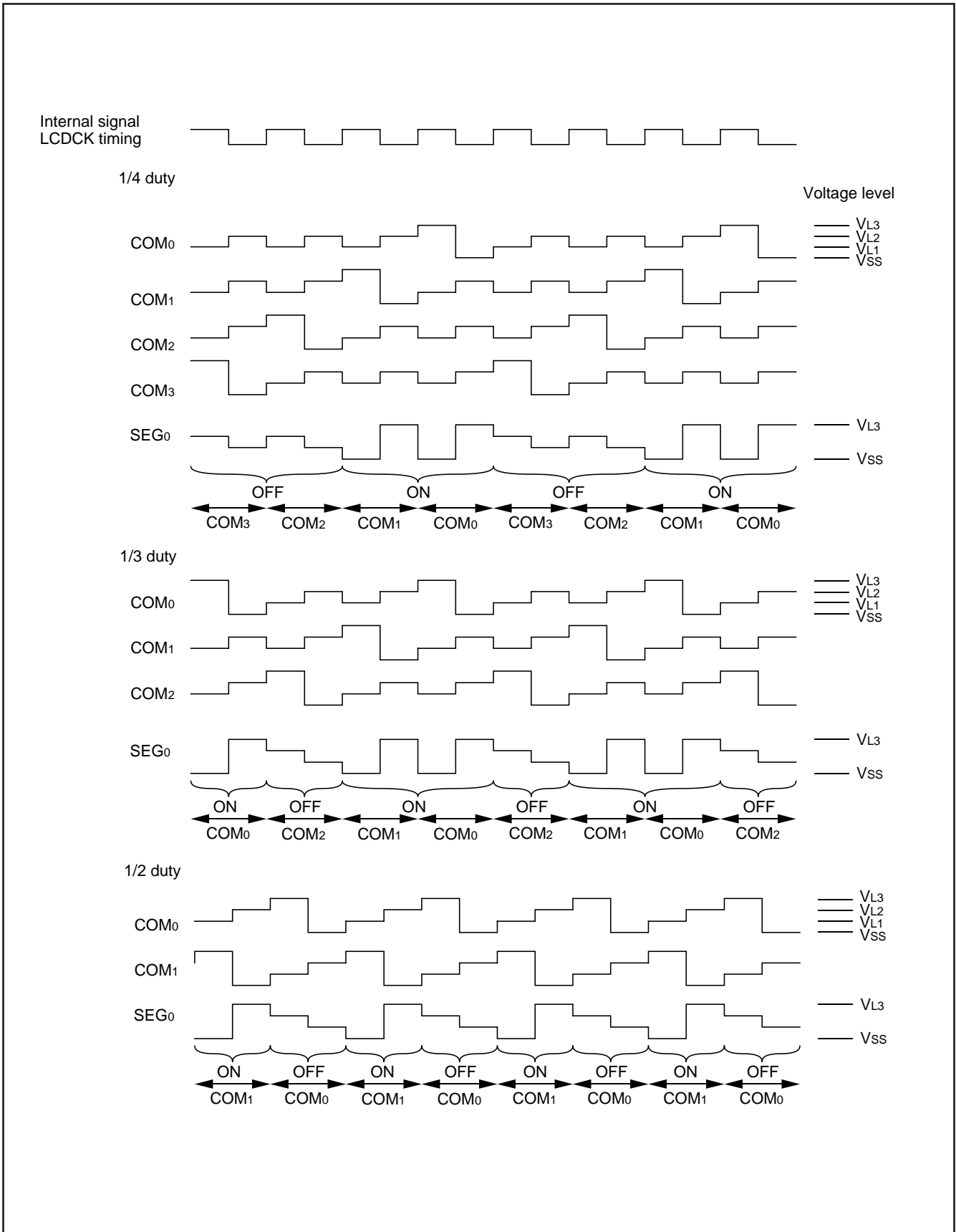


Fig. 32 LCD drive waveform (1/3 bias)

φ CLOCK OUTPUT FUNCTION

The internal system clock φ can be output from port P4₃ by setting the φ output control register. Set "1" to bit 3 of the port P4 direction register when outputting φ clock.

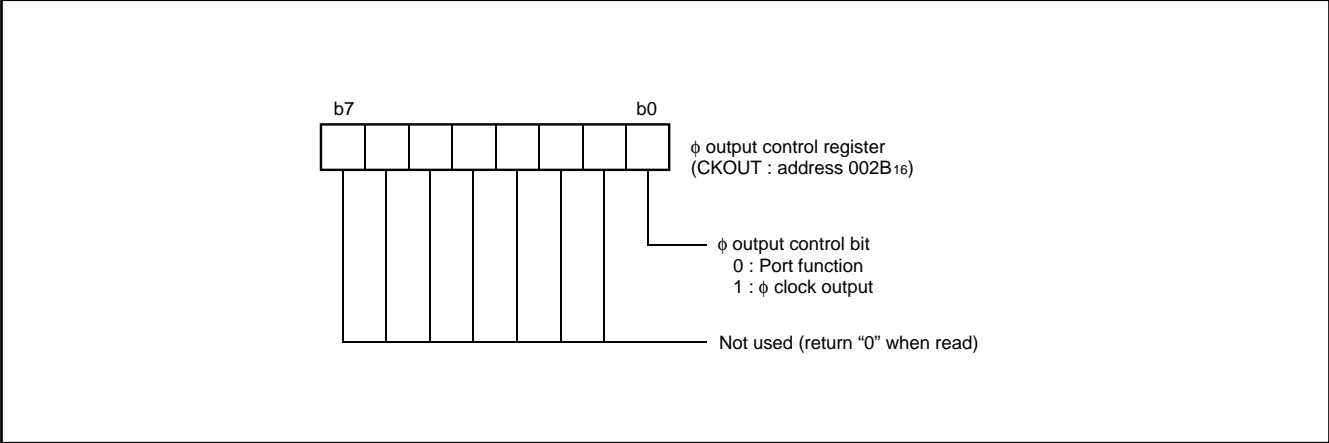


Fig. 33 Structure of φ output control register

ROM CORRECTION FUNCTION

The 38C3 group has the ROM correction function correcting data at the arbitrary addresses in the ROM area.

[ROM correct address register] 0F02₁₆ – 0F11₁₆

This is the register to store the address performing ROM correction. There are two types of registers to correct up to 8 addresses: one is the register to store the high-order address and the other is to store the low-order address.

[ROM correct enable register (RC1)] 0F01₁₆

This is the register to enable the ROM correction function. When setting the bit corresponding to the ROM correction address to “1”, the ROM correction function is enabled.

It becomes invalid to the addresses of which corresponding bit is “0”. All bits are “0” at the initial state.

[ROM correct data]

This is the register to store a correct data for the address specified by the ROM correct address register.

■Notes on ROM correction function

1. To use the ROM correction function, transfer data to each ROM correct data register in the initial setting.
2. Do not specify the same addresses in the ROM correct address register.

0F02 ₁₆	ROM correct high-order address register 1
0F03 ₁₆	ROM correct low-order address register 1
0F04 ₁₆	ROM correct high-order address register 2
0F05 ₁₆	ROM correct low-order address register 2
0F06 ₁₆	ROM correct high-order address register 3
0F07 ₁₆	ROM correct low-order address register 3
0F08 ₁₆	ROM correct high-order address register 4
0F09 ₁₆	ROM correct low-order address register 4
0F0A ₁₆	ROM correct high-order address register 5
0F0B ₁₆	ROM correct low-order address register 5
0F0C ₁₆	ROM correct high-order address register 6
0F0D ₁₆	ROM correct low-order address register 6
0F0E ₁₆	ROM correct high-order address register 7
0F0F ₁₆	ROM correct low-order address register 7
0F10 ₁₆	ROM correct high-order address register 8
0F11 ₁₆	ROM correct low-order address register 8

Fig. 34 Structure of ROM correct address register

0050 ₁₆	ROM correct data 1
0051 ₁₆	ROM correct data 2
0052 ₁₆	ROM correct data 3
0053 ₁₆	ROM correct data 4
0054 ₁₆	ROM correct data 5
0055 ₁₆	ROM correct data 6
0056 ₁₆	ROM correct data 7
0057 ₁₆	ROM correct data 8

Fig. 35 Structure of ROM correct data

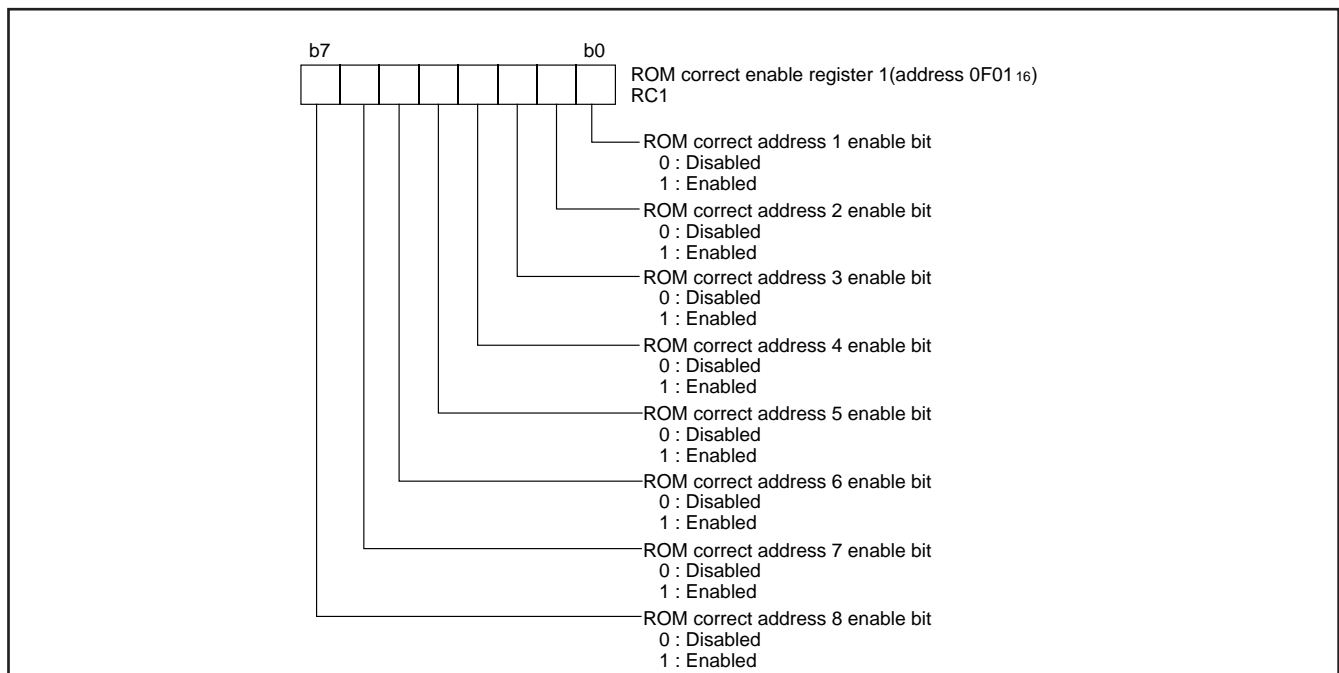


Fig. 36 Structure of ROM correct enable register 1

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.5 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD₁₆ (high-order byte) and address FFFC₁₆ (low-order byte). Make sure that the reset input voltage is less than 0.5 V for V_{CC} of 2.5 V (switching to the high-speed mode, a power source voltage must be between 4.0 V and 5.5 V).

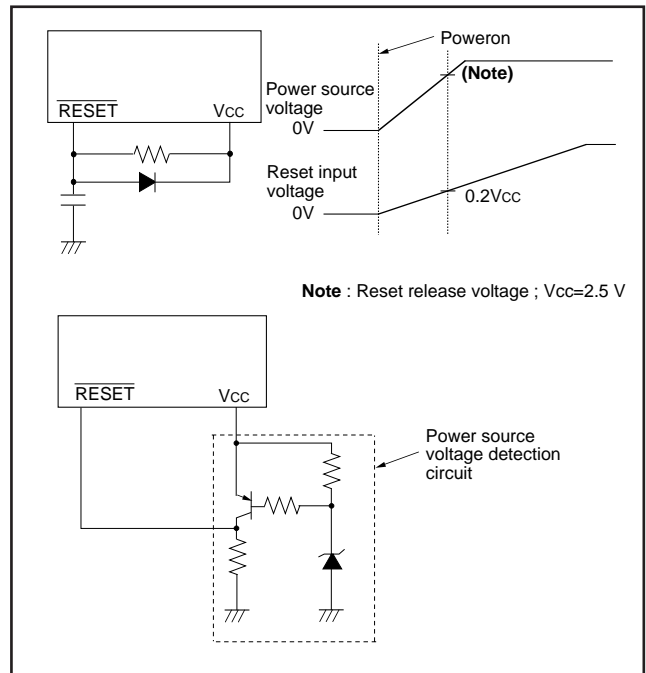


Fig. 37 Reset circuit example

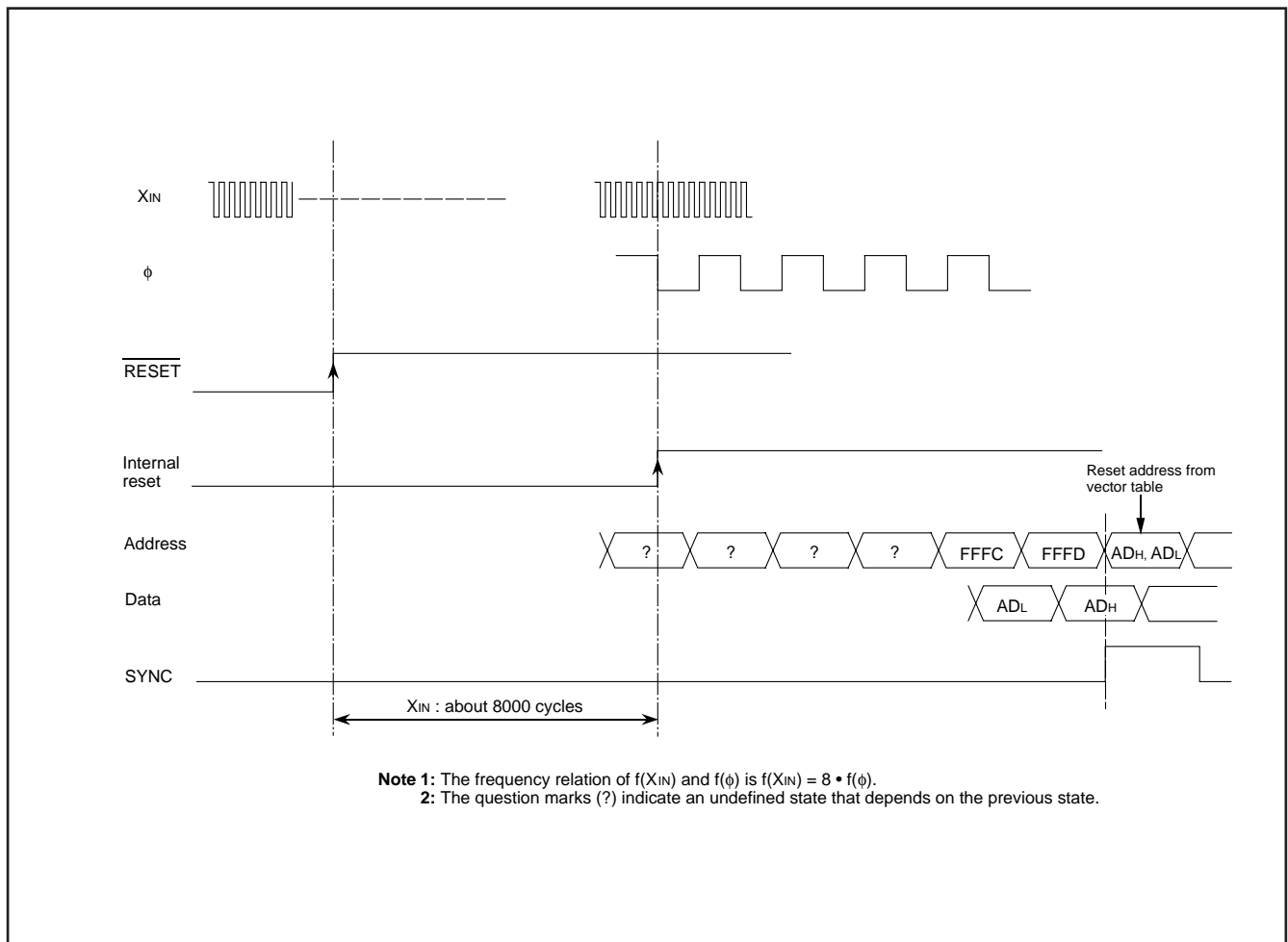


Fig. 38 Reset sequence

	Address	Register contents		Address	Register contents
(1) Port P0	0000 ₁₆	00 ₁₆	(34) Timer A (high-order)	002D ₁₆	FF ₁₆
(2) Port P0 direction register	0001 ₁₆	00 ₁₆	(35) Compare register (low-order)	002E ₁₆	00 ₁₆
(3) Port P1	0002 ₁₆	00 ₁₆	(36) Compare register (high-order)	002F ₁₆	00 ₁₆
(4) Port P1 direction register	0003 ₁₆	00 ₁₆	(37) Timer A mode register	0030 ₁₆	00 ₁₆
(5) Port P2	0004 ₁₆	00 ₁₆	(38) Timer A control register	0031 ₁₆	00 ₁₆
(6) Port P2 direction register	0005 ₁₆	00 ₁₆	(39) A-D control register	0032 ₁₆	10 ₁₆
(7) Port P3	0006 ₁₆	00 ₁₆	(40) Segment output enable register	0038 ₁₆	00 ₁₆
(8) Port P4	0008 ₁₆	00 ₁₆	(41) LCD mode register	0039 ₁₆	00 ₁₆
(9) Port P4 direction register	0009 ₁₆	00 ₁₆	(42) Interrupt edge selection register	003A ₁₆	00 ₁₆
(10) Port P5	000A ₁₆	00 ₁₆	(43) CPU mode register	003B ₁₆	01001000
(11) Port P5 direction register	000B ₁₆	00 ₁₆	(44) Interrupt request register 1	003C ₁₆	00 ₁₆
(12) Port P6	000C ₁₆	00 ₁₆	(45) Interrupt request register 2	003D ₁₆	00 ₁₆
(13) Port P6 direction register	000D ₁₆	00 ₁₆	(46) Interrupt control register 1	003E ₁₆	00 ₁₆
(14) Port P7	000E ₁₆	00 ₁₆	(47) Interrupt control register 2	003F ₁₆	00 ₁₆
(15) Port P7 direction register	000F ₁₆	00 ₁₆	(48) ROM correct enable register 1	0F01 ₁₆	00 ₁₆
(16) Port P8	0010 ₁₆	00 ₁₆	(49) ROM correct high-order address register 1	0F02 ₁₆	FF ₁₆
(17) Port P8 direction register	0011 ₁₆	00 ₁₆	(50) ROM correct low-order address register 1	0F03 ₁₆	FF ₁₆
(18) PULL register A	0016 ₁₆	0F ₁₆	(51) ROM correct high-order address register 2	0F04 ₁₆	FF ₁₆
(19) PULL register B	0017 ₁₆	00 ₁₆	(52) ROM correct low-order address register 2	0F05 ₁₆	FF ₁₆
(20) Port P8 output selection register	0018 ₁₆	00 ₁₆	(53) ROM correct high-order address register 3	0F06 ₁₆	FF ₁₆
(21) Serial I/O control register 1	0019 ₁₆	00 ₁₆	(54) ROM correct low-order address register 3	0F07 ₁₆	FF ₁₆
(22) Serial I/O control register 2	001A ₁₆	00 ₁₆	(55) ROM correct high-order address register 4	0F08 ₁₆	FF ₁₆
(23) Timer 1	0020 ₁₆	FF ₁₆	(56) ROM correct low-order address register 4	0F09 ₁₆	FF ₁₆
(24) Timer 2	0021 ₁₆	01 ₁₆	(57) ROM correct high-order address register 5	0F0A ₁₆	FF ₁₆
(25) Timer 3	0022 ₁₆	FF ₁₆	(58) ROM correct low-order address register 5	0F0B ₁₆	FF ₁₆
(26) Timer 4	0023 ₁₆	FF ₁₆	(59) ROM correct high-order address register 6	0F0C ₁₆	FF ₁₆
(27) Timer 5	0024 ₁₆	FF ₁₆	(60) ROM correct low-order address register 6	0F0D ₁₆	FF ₁₆
(28) Timer 6	0025 ₁₆	FF ₁₆	(61) ROM correct high-order address register 7	0F0E ₁₆	FF ₁₆
(29) Timer 12 mode register	0028 ₁₆	00 ₁₆	(62) ROM correct low-order address register 7	0F0F ₁₆	FF ₁₆
(30) Timer 34 mode register	0029 ₁₆	00 ₁₆	(63) ROM correct high-order address register 8	0F10 ₁₆	FF ₁₆
(31) Timer 56 mode register	002A ₁₆	00 ₁₆	(64) ROM correct low-order address register 8	0F11 ₁₆	FF ₁₆
(32) φ output control register	002B ₁₆	00 ₁₆	(65) Processor status register	(PS)	X X X X X 1 X X
(33) Timer A (low-order)	002C ₁₆	FF ₁₆	(66) Program counter	(PC _H)	FFFD ₁₆ contents
				(PC _L)	FFFC ₁₆ contents

X: Not fixed
 Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.
 In the M version, bit 0 of the port P5 direction register becomes "1."

Fig. 39 Internal status at reset

CLOCK GENERATING CIRCUIT

The 38C3 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feedback resistor exists on-chip. However, an external feedback resistor is needed between XCIN and XCOUT.

Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency control

(1) Middle-speed mode

The internal system clock is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal system clock is the frequency of XIN divided by 2.

(3) Low-speed mode

The internal system clock is the frequency of XCIN divided by 2.

■Notes on clock generating circuit

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(XIN) > 3f(XCIN)$.

Oscillation control

(1) Stop mode

If the STP instruction is executed, the internal system clock stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116."

Either XIN divided by 16 or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to "0." Set the interrupt enable bits of the timer 1 and timer 2 to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal system clock is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait mode

If the WIT instruction is executed, the internal system clock stops at an "H" level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The internal system clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

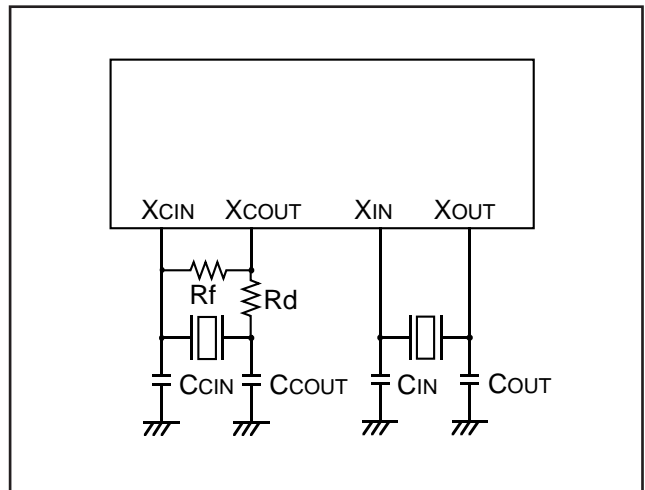


Fig. 40 Ceramic resonator circuit

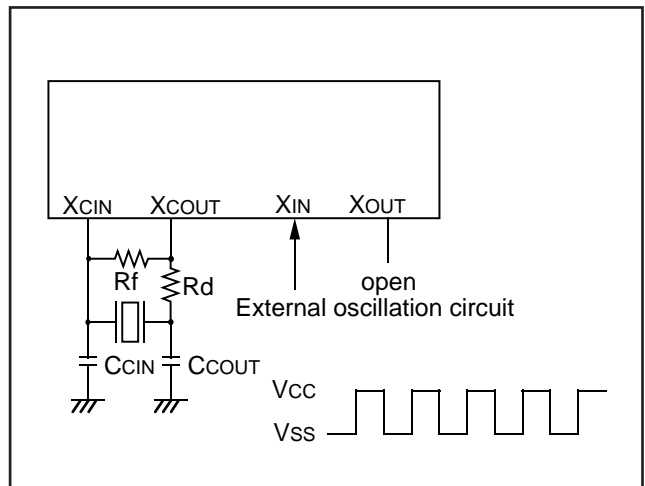


Fig. 41 External clock input circuit

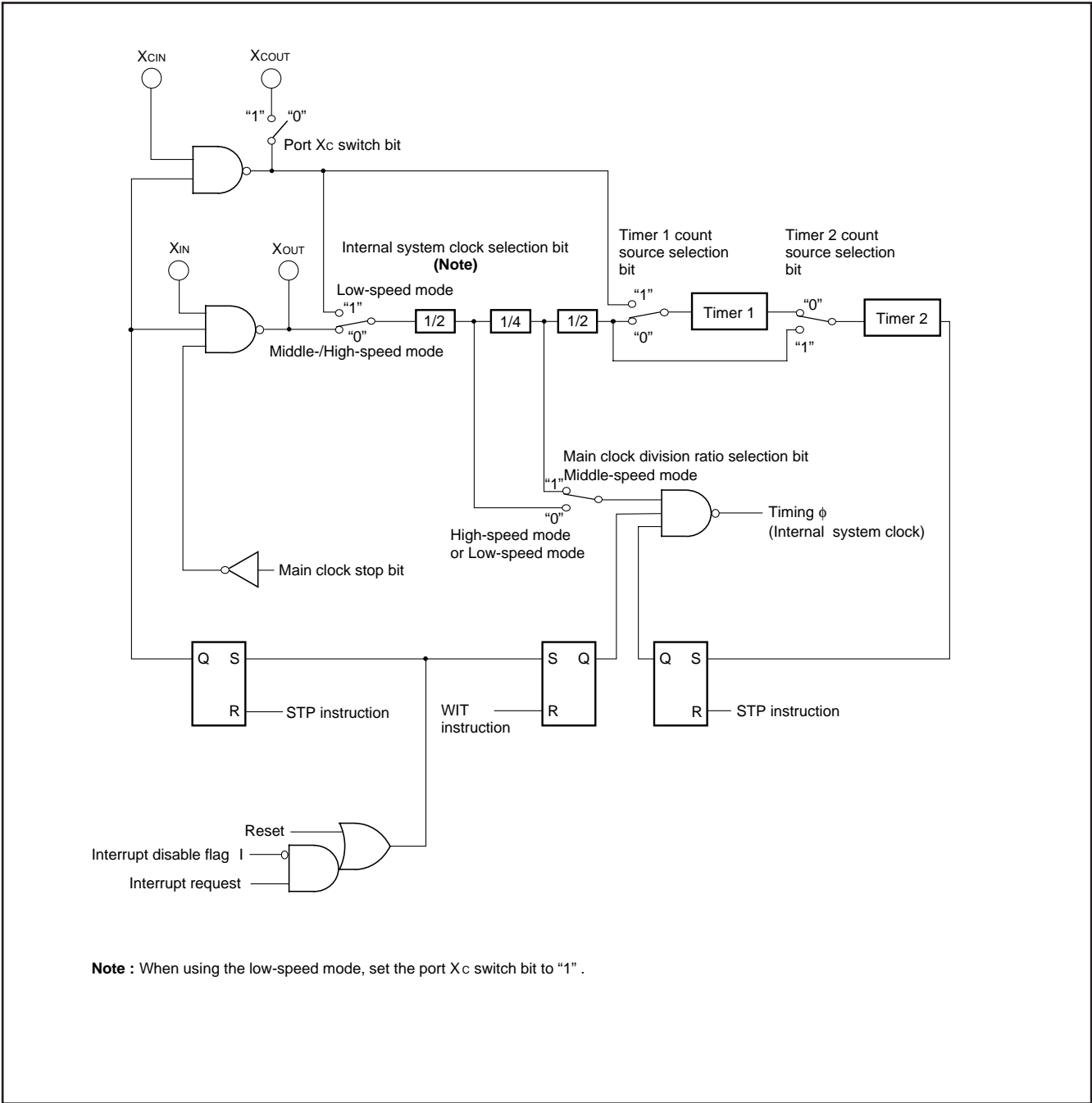
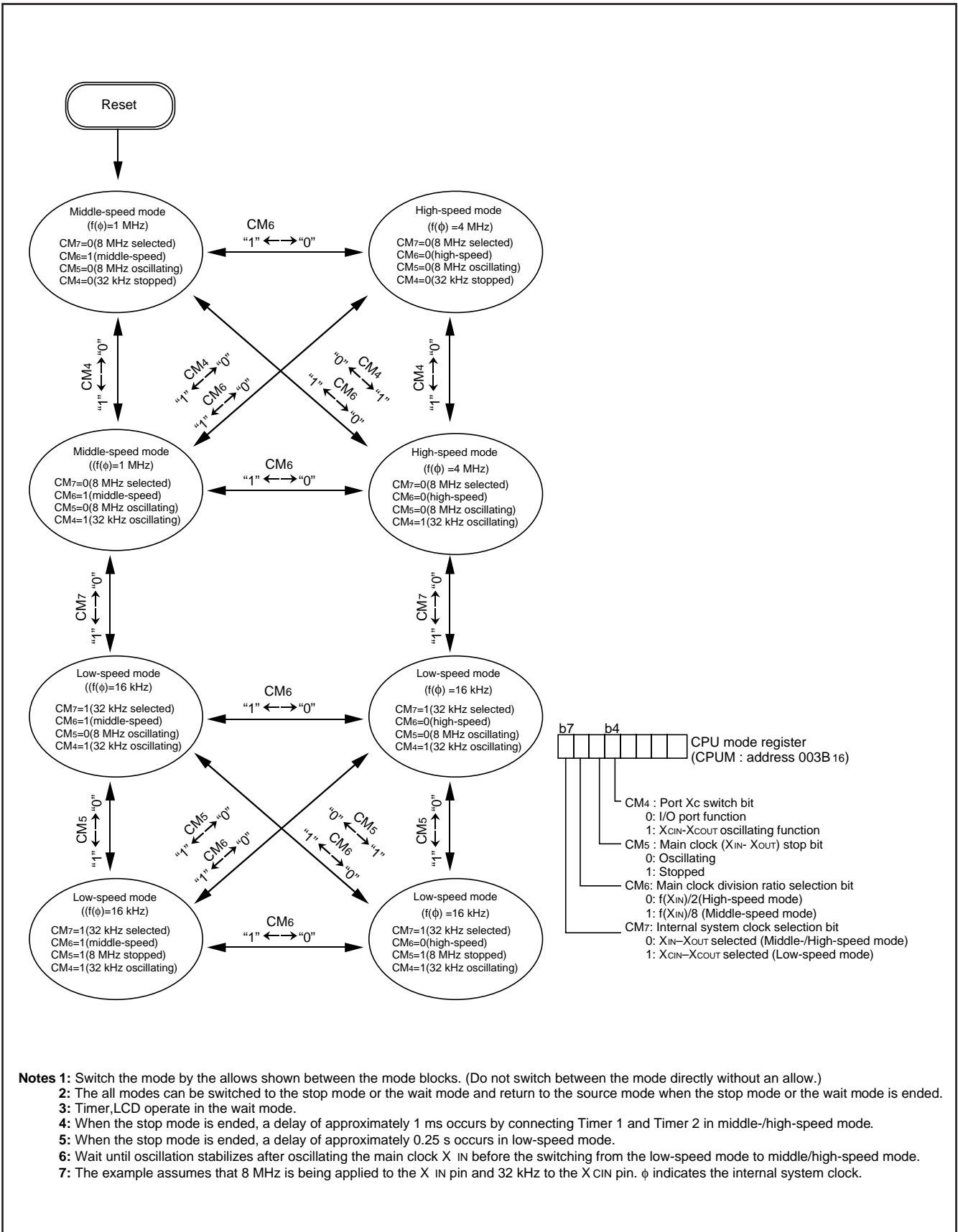


Fig. 42 Clock generating circuit block diagram



- Notes 1:** Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
- 2:** The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
- 3:** Timer, LCD operate in the wait mode.
- 4:** When the stop mode is ended, a delay of approximately 1 ms occurs by connecting Timer 1 and Timer 2 in middle-/high-speed mode.
- 5:** When the stop mode is ended, a delay of approximately 0.25 s occurs in low-speed mode.
- 6:** Wait until oscillation stabilizes after oscillating the main clock X_{IN} before the switching from the low-speed mode to middle/high-speed mode.
- 7:** The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. φ indicates the internal system clock.

Fig. 43 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1," then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

- Using an external clock

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.

- Using an internal clock

When using an internal clock, set the synchronous clock to the internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer and serial I/O automatic transfer.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Therefore, make sure that $f(X_{IN})$ is at least on 500 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal system clock by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal system clock is the same half of the X_{IN} frequency in high-speed mode.

At STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

NOTES ON USE

Notes on Built-in EPROM Version

The P51 pin of the One Time PROM version or the EPROM version functions as the power source input pin of the internal EPROM.

Therefore, this pin is set at low input impedance, thereby being affected easily by noise.

To prevent a malfunction due to noise, insert a resistor (approx. 5 k Ω) in series with the P51 pin.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

DATA REQUIRED FOR ROM WRITING ORDERS

The following are necessary when ordering a ROM writing:

1. ROM Writing Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Table 10 Programming adapter

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 44 is recommended to verify programming.

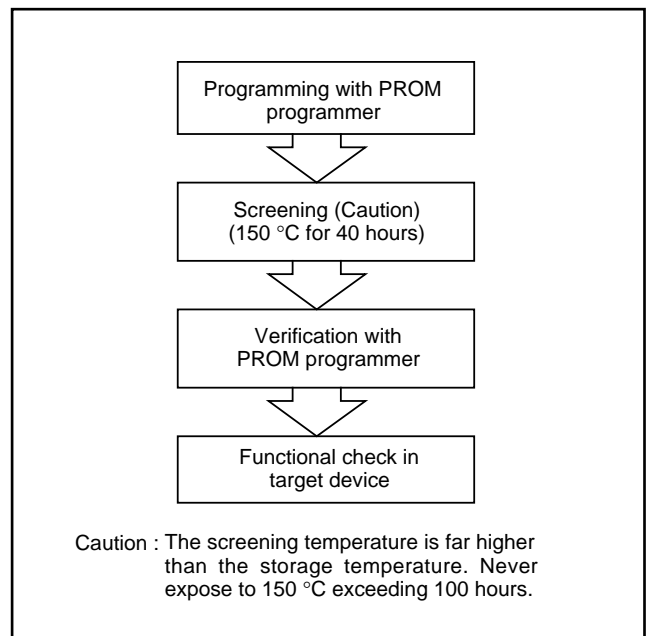


Fig. 44 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Table 11 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage		-0.3 to 7.0	V
VI	Input voltage P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67, P70, P71, P80-P87	All voltages are based on Vss. Output transistors are cut off.	-0.3 to VCC+0.3	V
VI	Input voltage VL1		-0.3 to VL2	V
VI	Input voltage VL2		VL1 to VL3	V
VI	Input voltage VL3		VL2 to VCC+0.3	V
VI	Input voltage RESET, XIN		-0.3 to VCC+0.3	V
VO	Output voltage P00-P07, P10-P17, P20-P27, P30-P37	At output port	-0.3 to VCC+0.3	V
		At segment output	-0.3 to VL3+0.3	V
VO	Output voltage COM0-COM3		-0.3 to VL3+0.3	V
VO	Output voltage P40-P47, P50, P52-P57, P60-P67, P70, P71, P80-P87		-0.3 to VCC+0.3	V
VO	Output voltage XOUT		-0.3 to VCC+0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-40 to 125	°C

Table 12 Recommended operating conditions (Vcc = 2.5 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage	High-speed mode f(XIN) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(XIN) = 8 MHz	2.5	5.0	5.5	V
		Low-speed mode	2.5	5.0	5.5	V
VSS	Power source voltage		0		V	
VREF	A-D converter reference voltage		2.0		VCC	V
AVSS	Analog power source voltage			0		V
VIA	Analog input voltage AN0-AN7		AVSS		VCC	V
VIH	"H" input voltage P00-P07, P10-P17, P20-P27		0.7VCC		VCC	V
VIH	"H" input voltage P40-P47, P50-P57, P60-P67, P70, P71 (CM4 = 0)		0.8VCC		VCC	V
VIH	"H" input voltage P80-P87		0.4VCC		VCC	V
VIH	"H" input voltage RESET		0.8VCC		VCC	V
VIH	"H" input voltage XIN		0.8VCC		VCC	V
VIL	"L" input voltage P00-P07, P10-P17, P20-P27		0		0.3VCC	V
VIL	"L" input voltage P40-P47, P50-P57, P60-P67, P70, P71 (CM4 = 0)		0		0.2VCC	V
VIL	"L" input voltage P80-P87		0		0.16VCC	V
VIL	"L" input voltage RESET		0		0.2VCC	V
VIL	"L" input voltage XIN		0		0.2VCC	V

Table 13 Recommended operating conditions ($V_{CC} = 2.5$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH}(\text{peak})$	"H" total peak output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37 P80–P87, P50			–60	mA
$\Sigma I_{OH}(\text{peak})$	"H" total peak output current (Note 1) P40–P47, P52–P57, P60–P67, P70, P71			–30	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37			40	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P80–P87, P50			80	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P40–P47, P52–P57, P60–P67, P70, P71			40	mA
$\Sigma I_{OH}(\text{avg})$	"H" total average output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37 P80–P87, P50			–30	mA
$\Sigma I_{OH}(\text{avg})$	"H" total average output current (Note 1) P40–P47, P52–P57, P60–P67, P70, P71			–15	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37			20	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P80–P87, P50			40	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P40–P47, P52–P57, P60–P67, P70, P71			20	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P00–P07, P10–P17, P20–P27, P30–P37			–2.0	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P40–P47, P50, P52–P57, P60–P67, P70, P71 P80–P87			–10	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P00–P07, P10–P17, P20–P27, P30–P37			5.0	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P40–P47, P52–P57, P60–P67, P70, P71			10	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P80–P87, P50			30	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P00–P07, P10–P17, P20–P27, P30–P37			–2.0	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P40–P47, P50, P52–P57, P60–P67, P70, P71 P80–P87			–5.0	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P00–P07, P10–P17, P20–P27, P30–P37			2.5	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P40–P47, P52–P57, P60–P67, P70, P71			5.0	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P80–P87, P50			15	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is average value measured over 100 ms.

Table 14 Recommended operating conditions ($V_{CC} = 2.5$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
f(CNTR ₀)	Input frequency (duty cycle 50%)	($4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)			4.0	MHz
f(CNTR ₁)		($V_{CC} \leq 4.0\text{ V}$)			($2 \times V_{CC}$)-4	MHz
f(XIN)	Main clock input oscillation frequency (Note 4)	High-speed mode ($4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)			8.0	MHz
		High-speed mode ($V_{CC} \leq 4.0\text{ V}$)			($4 \times V_{CC}$)-8	MHz
		Middle-speed mode			8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (Notes 4, 5)			32.768	50	kHz

Notes 4: When the oscillation frequency has a duty cycle of 50%.

5: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(XCIN) < f(XIN)/3$.

Table 15 Electrical characteristics (V_{CC} = 4.0 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
VOH	"H" output voltage P00-P07, P10-P17, P20-P27, P30-P37	IOH = -2.0 mA	V _{CC} -2.0			V	
		IOH = -0.6 mA	V _{CC} -1.0			V	
		V _{CC} = 2.5 V					
VOH	"H" output voltage P40-P47, P50, P52-P57, P60-P67, P70, P71, P80-P87	(Note) IOH = -5 mA IOH = -1.25 mA IOH = -1.25 mA V _{CC} = 2.5 V	V _{CC} -2.0			V	
			V _{CC} -0.5			V	
			V _{CC} -1.0			V	
VOL	"L" output voltage P00-P07, P10-P17, P20-P27, P30-P37	IOL = 2.5 mA IOL = 1.25 mA IOL = 1.25 mA V _{CC} = 2.5 V			2.0	V	
					0.5	V	
					1.0	V	
VOL	"L" output voltage P40-P47, P52-P57, P60-P67, P70, P71	(Note) IOL = 5.0 mA IOL = 2.5 mA IOL = 2.5 mA V _{CC} = 2.5 V			2.0	V	
					0.5	V	
					1.0	V	
VOL	"L" output voltage P80-P87, P50	IOL = 15 mA			2.0	V	
VT+~VT-	Hysteresis INT0-INT2, CNTR0, CNTR1, P80-P87			0.5		V	
VT+~VT-	Hysteresis SCLK1, SIN			0.5		V	
VT+~VT-	Hysteresis $\overline{\text{RESET}}$	$\overline{\text{RESET}}$: V _{CC} = 2.5 V - 5.5 V		0.5		V	
IIH	"H" input current P00-P07, P10-P17, P20-P27	VI = V _{CC} Pull-down "off"			5.0	μA	
			V _{CC} = 5.0 V, VI = V _{CC} Pull-down "on"	30	70	140	μA
			V _{CC} = 3.0 V, VI = V _{CC} Pull-down "on"	6.0	25	45	μA
IIH	"H" input current P40-P47, P50-P57, P60-P67, P70, P71, P80-P87	VI = V _{CC}			5.0	μA	
IIH	"H" input current $\overline{\text{RESET}}$	VI = V _{CC}			5.0	μA	
IIH	"H" input current XIN	VI = V _{CC}		4.0		μA	
IIL	"L" input current P00-P07, P10-P17, P20-P27, P51				-5.0	μA	
IIL	"L" input current P40-P47, P50, P52-P57, P60-P67, P70, P71, P80-P87	VI = V _{SS} Pull-up "off"			-5.0	μA	
			V _{CC} = 5.0 V, VI = V _{SS} Pull-up "on"	-30	-70	-140	μA
			V _{CC} = 3.0 V, VI = V _{SS} Pull-up "on"	-6	-25	-45	μA
IIL	"L" input current $\overline{\text{RESET}}$	VI = V _{SS}			-5	μA	
IIL	"L" input current XIN	VI = V _{SS}		-4		μA	

Note: When "1" is set to the port Xc switch bit (bit 4 of address 003B16) of the CPU mode register, the drive ability of Port P70 is different from the value above mentioned.

Table 16 Electrical characteristics ($V_{CC} = 2.5$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped	2.0		5.5	V
I _{CC}	Power source current	High-speed mode, $V_{CC} = 5$ V $f(X_{IN}) = 8$ MHz $f(X_{CIN}) = 32.768$ kHz Output transistors "off", A-D converter in operating		6.4	13	mA
		High-speed mode, $V_{CC} = 5$ V $f(X_{IN}) = 8$ MHz (in WIT state) $f(X_{CIN}) = 32.768$ kHz Output transistors "off", A-D converter stopped		1.6	3.2	mA
		Low-speed mode, $V_{CC} = 3$ V, $T_a \leq 55^\circ\text{C}$ $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32.768$ kHz Output transistors "off"		15	22	μA
		Low-speed mode, $V_{CC} = 3$ V, $T_a = 25^\circ\text{C}$ $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32.768$ kHz (in WIT state) Output transistors "off"		4.5	9.0	μA
		All oscillation stopped (in STP state) Output transistors "off"	$T_a = 25^\circ\text{C}$		0.1	1.0
		$T_a = 85^\circ\text{C}$			10	μA

Table 17 A-D converter characteristics

($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , 4 MHz $\leq f(X_{IN}) \leq 8$ MHz, in middle-speed/high-speed mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	$V_{CC} = V_{REF} = 5.12$ V		± 1	± 2.5	LSB
T_{conv}	Conversion time		61		62	tc(ϕ)
I_{VREF}	Reference input current	$V_{REF} = 5$ V	50	150	200	μA
I_{IA}	Analog port input current			0.5	5.0	μA
RLADDER	Ladder resistor			35		k Ω

Table 18 Timing requirements 1 ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{\text{RESET}})$	Reset input "L" pulse width	2			μs
$t_c(\text{XIN})$	Main clock input cycle time (XIN input)	125			ns
$t_{wH}(\text{XIN})$	Main clock input "H" pulse width	45			ns
$t_{wL}(\text{XIN})$	Main clock input "L" pulse width	40			ns
$t_c(\text{CNTR})$	CNTR0, CNTR1 input cycle time	250			ns
$t_{wH}(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	105			ns
$t_{wL}(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	105			ns
$t_{wH}(\text{INT})$	INT0–INT2 input "H" pulse width	80			ns
$t_{wL}(\text{INT})$	INT0–INT2 input "L" pulse width	80			ns
$t_c(\text{SCLK})$	Serial I/O clock input cycle time	800			ns
$t_{wH}(\text{SCLK})$	Serial I/O clock input "H" pulse width	370			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock input "L" pulse width	370			ns
$t_{su}(\text{SIN-SCLK})$	Serial I/O input setup time	220			ns
$t_h(\text{SCLK-SIN})$	Serial I/O input hold time	100			ns

Table 19 Timing requirements 2 ($V_{CC} = 2.5$ to 4.0 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{\text{RESET}})$	Reset input "L" pulse width	2			μs
$t_c(\text{XIN})$	Main clock input cycle time (XIN input)	125			ns
$t_{wH}(\text{XIN})$	Main clock input "H" pulse width	45			ns
$t_{wL}(\text{XIN})$	Main clock input "L" pulse width	40			ns
$t_c(\text{CNTR})$	CNTR0, CNTR1 input cycle time	$500/(V_{CC}-2)$			ns
$t_{wH}(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	$250/(V_{CC}-2)-20$			ns
$t_{wL}(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	$250/(V_{CC}-2)-20$			ns
$t_{wH}(\text{INT})$	INT0–INT2 input "H" pulse width	230			ns
$t_{wL}(\text{INT})$	INT0–INT2 input "L" pulse width	230			ns
$t_c(\text{SCLK})$	Serial I/O clock input cycle time	2000			ns
$t_{wH}(\text{SCLK})$	Serial I/O clock input "H" pulse width	950			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock input "L" pulse width	950			ns
$t_{su}(\text{SIN-SCLK})$	Serial I/O input setup time	400			ns
$t_h(\text{SCLK-SIN})$	Serial I/O input hold time	200			ns

Table 20 Switching characteristics 1 ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{wH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$t_c(\text{SCLK})/2-30$			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$t_c(\text{SCLK})/2-30$			ns
$t_d(\text{SCLK-SOUT})$	Serial I/O output delay time (Note 1)			140	ns
$t_v(\text{SCLK-SOUT})$	Serial I/O output valid time (Note 1)	-30			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time			30	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time			30	ns
$t_r(\text{CMOS})$	CMOS output rising time (Note 2)		10	30	ns
$t_f(\text{CMOS})$	CMOS output falling time (Note 2)		10	30	ns

Notes 1: When the P-channel output disable bit (bit 7 of address 001916) is "0."
2: The XOUT, XCOUT pins are excluded.

Table 21 Switching characteristics 2 ($V_{CC} = 2.5$ to 4.0 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{wH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$t_c(\text{SCLK})/2-50$			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$t_c(\text{SCLK})/2-50$			ns
$t_d(\text{SCLK-SOUT})$	Serial I/O output delay time (Note 1)			350	ns
$t_v(\text{SCLK-SOUT})$	Serial I/O output valid time (Note 1)	-30			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time			50	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time			50	ns
$t_r(\text{CMOS})$	CMOS output rising time (Note 2)		20	50	ns
$t_f(\text{CMOS})$	CMOS output falling time (Note 2)		20	50	ns

Notes 1: When the P-channel output disable bit (bit 7 of address 001916) is "0."
2: The XOUT, XCOUT pins are excluded.

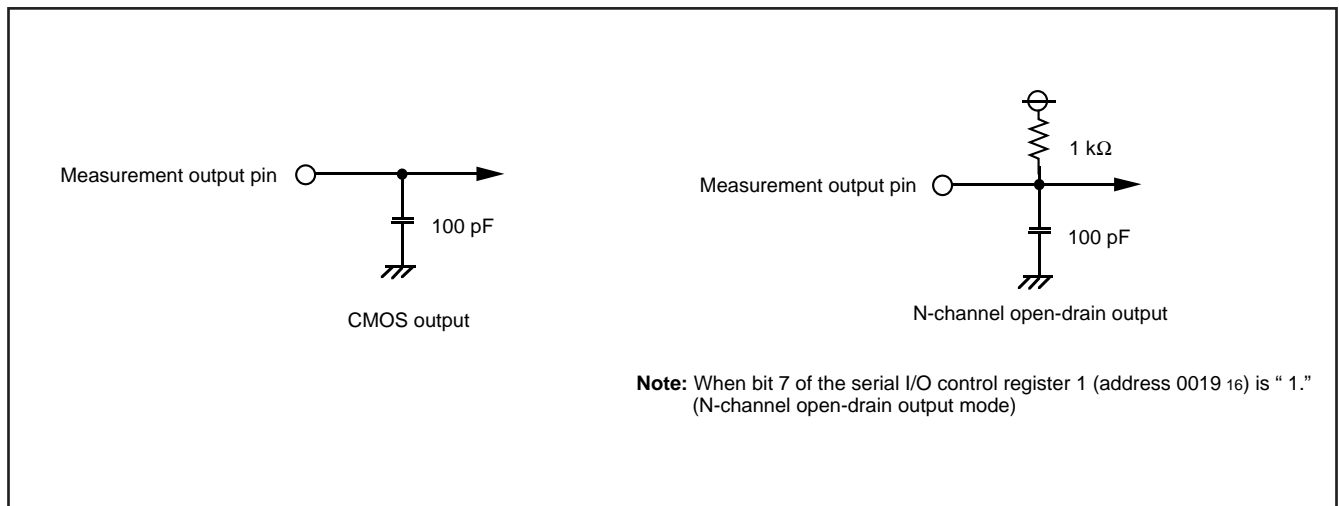


Fig. 45 Circuit for measuring output switching characteristics

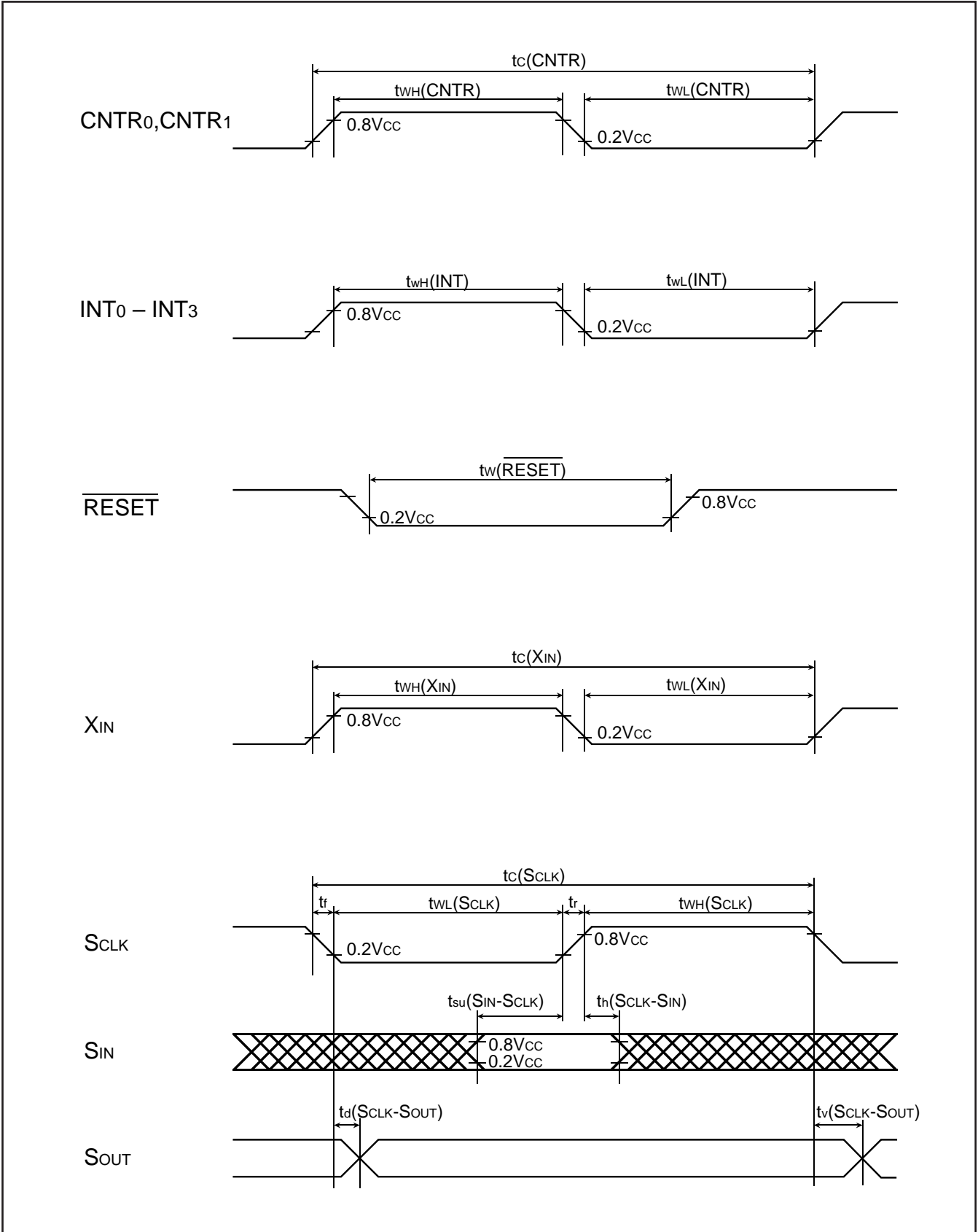


Fig. 46 Timing diagram

GZZ-SH52-95B<85A0>

Mask ROM number	
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**740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C34M6AXXFP
MITSUBISHI ELECTRIC**

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

* 1. Confirmation

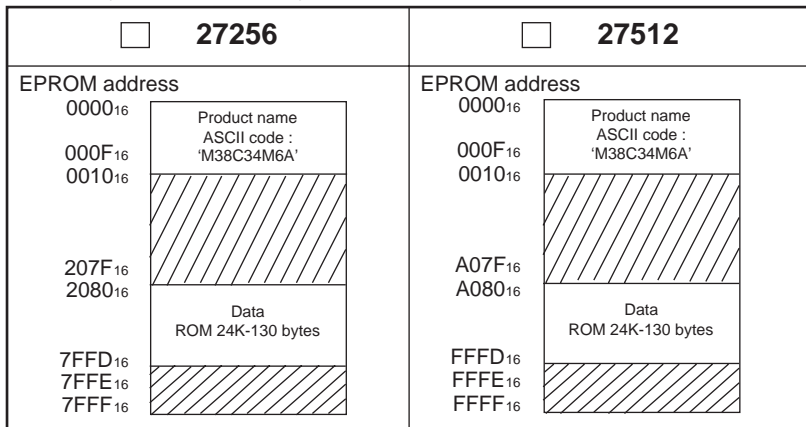
Specify the name of the product being ordered and the type of EPROMs submitted. Three EPROMs are required for each pattern. If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

--	--	--	--

 (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address A080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38C34M6A" must be entered in addresses 0000₁₆ to 0008₁₆. And set data "FF₁₆" in addresses 0009₁₆ to 000F₁₆. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address	Address	Address
0000 ₁₆	'M' = 4D ₁₆	0008 ₁₆
0001 ₁₆	'3' = 33 ₁₆	'A' = 41 ₁₆
0002 ₁₆	'8' = 38 ₁₆	0009 ₁₆
0003 ₁₆	'C' = 43 ₁₆	FF ₁₆
0004 ₁₆	'3' = 33 ₁₆	000A ₁₆
0005 ₁₆	'4' = 34 ₁₆	FF ₁₆
0006 ₁₆	'M' = 4D ₁₆	000B ₁₆
0007 ₁₆	'6' = 36 ₁₆	FF ₁₆
		000C ₁₆
		FF ₁₆
		000D ₁₆
		FF ₁₆
		000E ₁₆
		FF ₁₆
		000F ₁₆
		FF ₁₆

GZZ-SH52-96B<85A0>

Mask ROM number	
-----------------	--

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C34M6MXXFP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

* 1. Confirmation

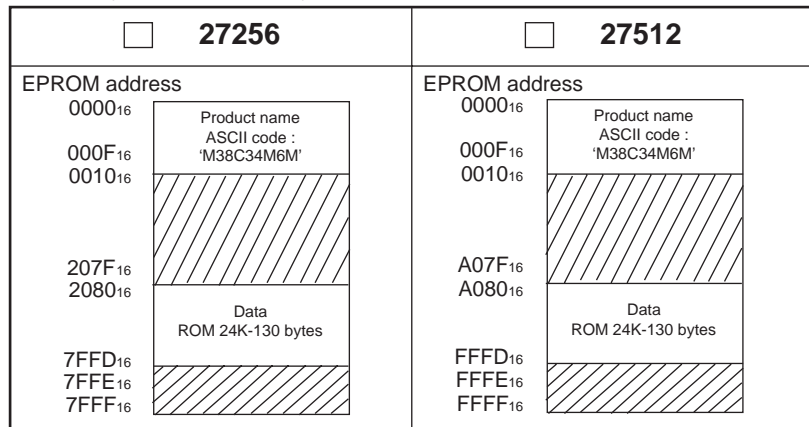
Specify the name of the product being ordered and the type of EPROMs submitted.
 Three EPROMs are required for each pattern.
 If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

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 (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address A080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38C34M6M" must be entered in addresses 0000₁₆ to 0008₁₆. And set data "FF₁₆" in addresses 0009₁₆ to 000F₁₆. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address	Address	Address
0000 ₁₆	'M' = 4D ₁₆	0008 ₁₆
0001 ₁₆	'3' = 33 ₁₆	'M' = 4D ₁₆
0002 ₁₆	'8' = 38 ₁₆	0009 ₁₆
0003 ₁₆	'C' = 43 ₁₆	FF ₁₆
0004 ₁₆	'3' = 33 ₁₆	000A ₁₆
0005 ₁₆	'4' = 34 ₁₆	FF ₁₆
0006 ₁₆	'M' = 4D ₁₆	000B ₁₆
0007 ₁₆	'6' = 36 ₁₆	FF ₁₆
		000C ₁₆
		FF ₁₆
		000D ₁₆
		FF ₁₆
		000E ₁₆
		FF ₁₆
		000F ₁₆
		FF ₁₆

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ROM number	
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740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C37ECAXXFP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

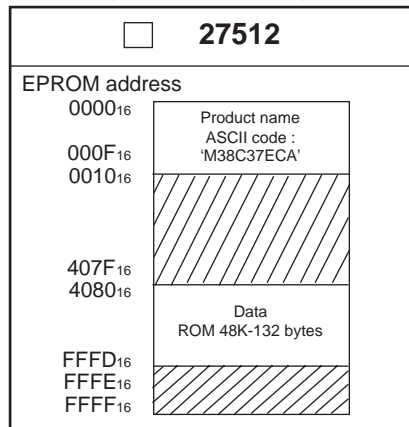
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM programming data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address 4080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38C37ECA" must be entered in addresses 0000₁₆ to 0008₁₆. And set data "FF₁₆" in addresses 0009₁₆ to 000F₁₆. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address

0000 ₁₆	'M' = 4D ₁₆
0001 ₁₆	'3' = 33 ₁₆
0002 ₁₆	'8' = 38 ₁₆
0003 ₁₆	'C' = 43 ₁₆
0004 ₁₆	'3' = 33 ₁₆
0005 ₁₆	'7' = 37 ₁₆
0006 ₁₆	'E' = 45 ₁₆
0007 ₁₆	'C' = 43 ₁₆

Address

0008 ₁₆	'A' = 41 ₁₆
0009 ₁₆	FF ₁₆
000A ₁₆	FF ₁₆
000B ₁₆	FF ₁₆
000C ₁₆	FF ₁₆
000D ₁₆	FF ₁₆
000E ₁₆	FF ₁₆
000F ₁₆	FF ₁₆

GZZ-SH52-97B<85A0>

ROM number	
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**740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C37ECAXXXFP
MITSUBISHI ELECTRIC**

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 0000₁₆ to 0008₁₆ of EPROM.

EPROM type	27512
The pseudo-command	*=Δ\$0000 .BYTEΔ'M38C37ECA'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM will not be processed.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the ROM programming confirmation form.

※ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

- | | |
|---|---|
| <input type="checkbox"/> Ceramic resonator | <input type="checkbox"/> Quartz crystal |
| <input type="checkbox"/> External clock input | <input type="checkbox"/> Other () |

At what frequency?

f(X_{IN}) = MHz

(2) Which function will you use the P7₀/X_{CIN} and P7₀/X_{COU}T pins?

- | | |
|--|---|
| <input type="checkbox"/> Port P7 ₀ and P7 ₁ function | <input type="checkbox"/> X _{CIN} -X _{COU} T function (external resonator) |
|--|---|

※ 4. Comments

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ROM number	
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740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C37ECMXXXFP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

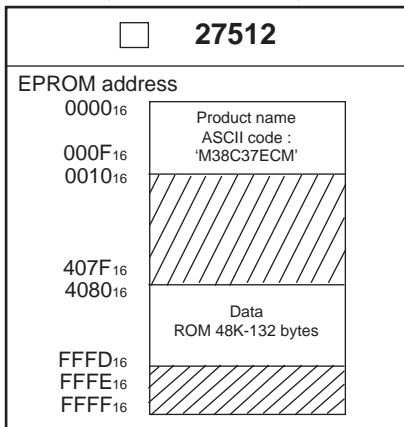
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM programming data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

--	--	--	--

(hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address 4080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38C37ECM" must be entered in addresses 0000₁₆ to 0008₁₆. And set data "FF₁₆" in addresses 0009₁₆ to 000F₁₆. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address

0000 ₁₆	'M' = 4D ₁₆
0001 ₁₆	'3' = 33 ₁₆
0002 ₁₆	'8' = 38 ₁₆
0003 ₁₆	'C' = 43 ₁₆
0004 ₁₆	'3' = 33 ₁₆
0005 ₁₆	'7' = 37 ₁₆
0006 ₁₆	'E' = 45 ₁₆
0007 ₁₆	'C' = 43 ₁₆

Address

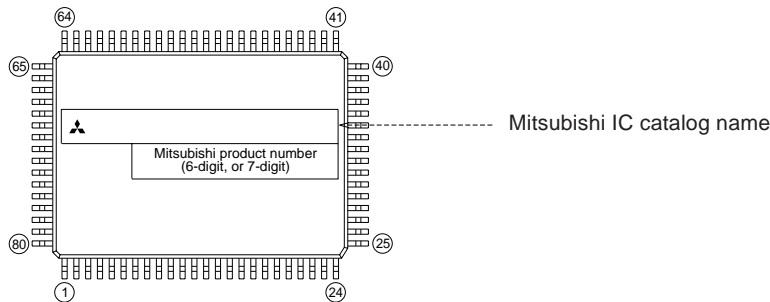
0008 ₁₆	' M ' = 4D ₁₆
0009 ₁₆	FF ₁₆
000A ₁₆	FF ₁₆
000B ₁₆	FF ₁₆
000C ₁₆	FF ₁₆
000D ₁₆	FF ₁₆
000E ₁₆	FF ₁₆
000F ₁₆	FF ₁₆

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

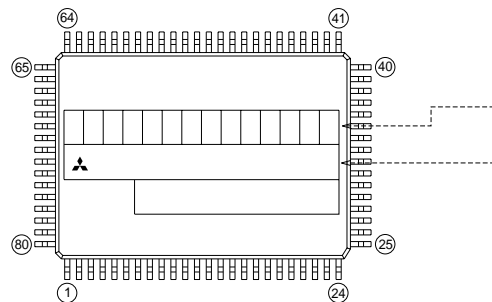
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



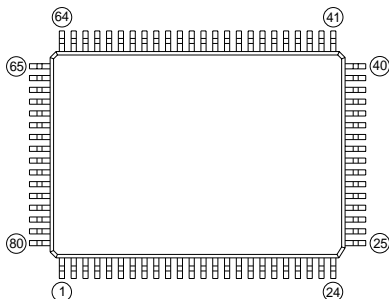
B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number
 Note : The fonts and size of characters are standard Mitsubishi type.
 Mitsubishi IC catalog name
 Notes 1 : The mark field should be written right aligned.
 2 : The fonts and size of characters are standard Mitsubishi type.
 3 : Customer's parts number can be up to 14 alphanumeric characters for capital letters, hyphens, commas, periods and so on.
 4 : If the Mitsubishi logo ▲ is not required, check the box below.

▲ Mitsubishi logo is not required

C. Special Mark Required



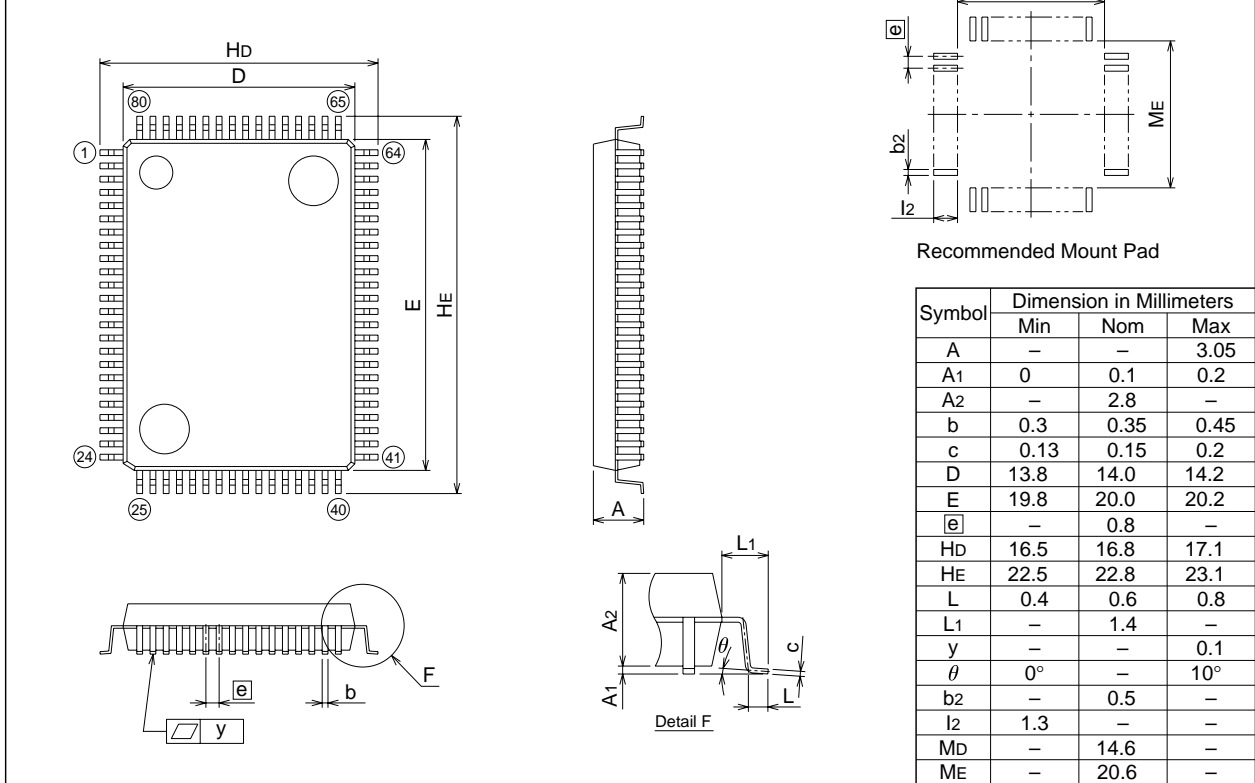
Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.
 Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.
 2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.
 For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

80P6N-A

Plastic 80pin 14x20mm body QFP

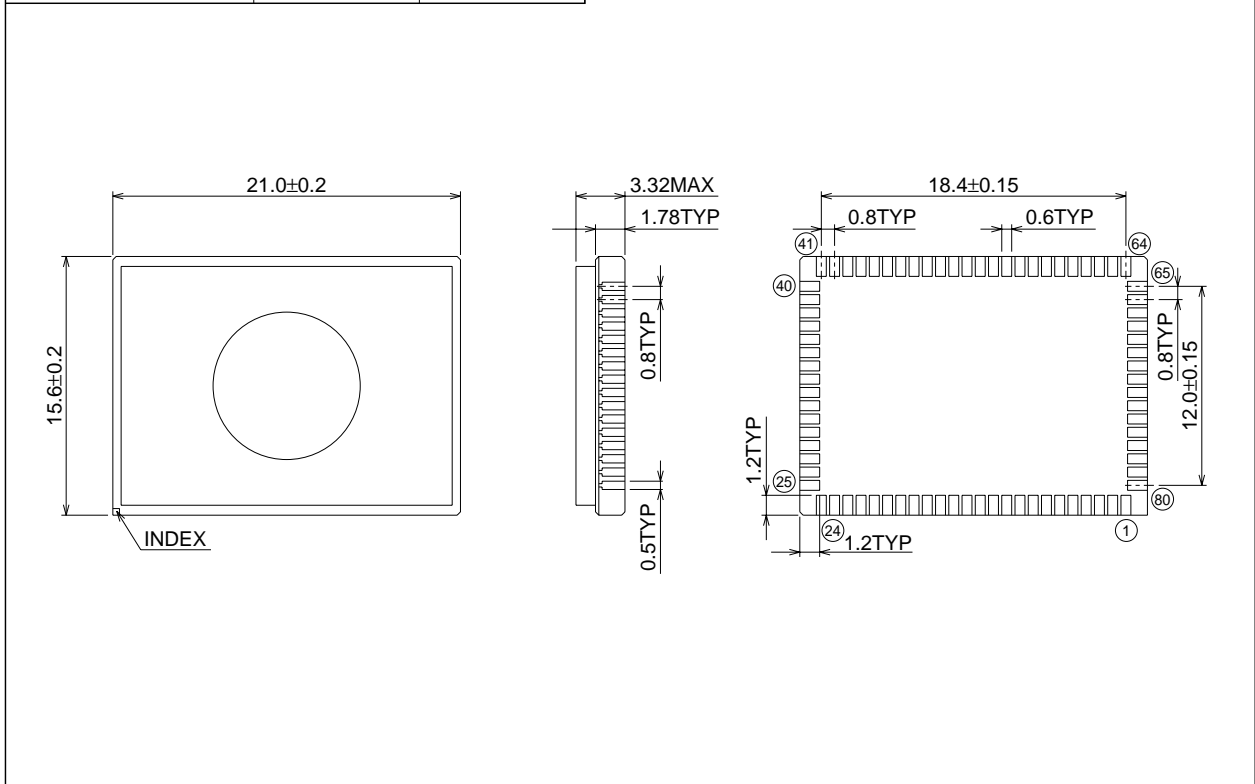
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	-	1.58	Alloy 42



80D0

Glass seal 80pin QFN

EIAJ Package Code	JEDEC Code	Weight(g)
-	-	-



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REVISION DESCRIPTION LIST

38C3 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980602