



# LA75503V

## Adjustment Free VIF/SIF Signal Processing IC for PAL TV/VCR

### Overview

The LA75503V is an adjustment free VIF/SIF signal processing IC for PAL TV/VCR.

It supports 38 MHz, 38.9 MHz, and 39.5 MHz as the IF frequencies, as well as PAL sound multi-system (M/N, B/G, I, D/K), and contains an on-chip sound carrier trap and sound carrier BPF. To adjust the VCO circuit, AFT circuit, and sound filter, 4-MHz external crystal or 4-MHz external signal is needed.

### Functions

- VIF amplifier
- VCO adjustment free PLL detection circuit
- Digital AFT circuit
- RF AGC
- Buzz canceller
- Equalizer amplifier
- Internal sound carrier BPF
- Internal sound carrier trap
- PLL-FM detector
- Reference oscillation circuit

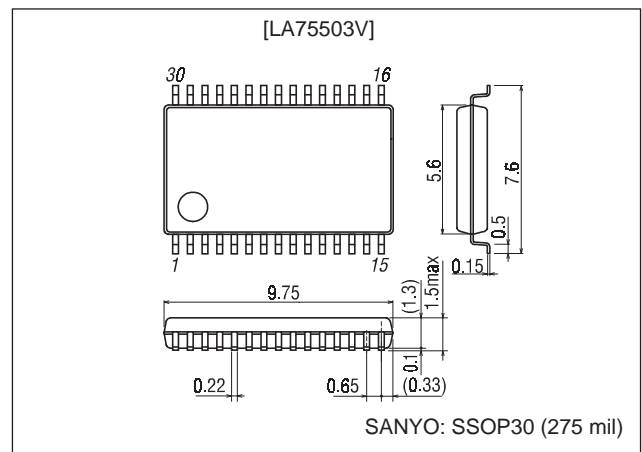
### Features

- Internal VCO adjustment free circuit eliminating need for VCO coil adjustments.
- Internal sound carrier BPF and sound carrier trap enable easy configuration of PAL sound multi-system at low cost.
- Considerably reduces the number of required peripheral parts.
- Use of digital AFT eliminates problem of AFT tolerance.
- Package: SSOP30 (275 mil)

### Package Dimensions

unit: mm

#### 3191A-SSOP30 (275 mil)



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## Specifications

### Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		7	V
Circuit voltage	V16		V <sub>CC</sub>	V
	V18		V <sub>CC</sub>	V
Circuit current	I30		-1	mA
	I17		+0.5	mA
	I6		-10	mA
	I4		-3	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C (*Mounted on a printed circuit board)	550	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

Note: \* Circuit board dimensions: 65 × 72 × 1.6 mm<sup>3</sup>, material: paper phenol.

### Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V <sub>CC</sub>		5	V
Operating voltage range	V <sub>CC</sub> op		4.5 to 5.5	V

### Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 5.0 V, fp = 38.9 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[VIF Block ]						
Circuit current	I17			64.0	73.6	mA
Maximum RF AGC voltage	V14H	Collector load 30 kΩ VC2 = 9 V	8.5	9	—	V
Minimum RF AGC voltage	V14L			0.3	0.7	V
Input sensitivity	V <sub>i</sub>		33	39	45	dBμV
AGC range	GR		58			dB
Maximum allowable input	V <sub>imax</sub>		92	97		dBμV
No-signal video output voltage	V4		3.3	3.6	3.9	V
Synchronizing signal tip voltage	V4tip		1.0	1.3	1.6	V
Video output level	V <sub>O</sub>		1.7	2.0	2.3	V <sub>pp</sub>
Video signal-to-noise ratio	S/N	B/G	48	52		dB
C-S beating	IC-S	P/S = 10 dB	26	32	38	dB
Differential gain	DG	V <sub>in</sub> = 80 dBμ		3	10	%
Differential phase	DP			2	10	deg
Black noise threshold voltage	VBTH			0.7		V
Black noise clamp voltage	VBCL			1.8		V
VIF input resistance	R <sub>i</sub>			2.5	3.0	kΩ
VIF input capacitance	C <sub>i</sub>			3	6	PF
Maximum AFT voltage	V13H		4.3	4.7	5.0	V
Minimum AFT voltage	V13L		0	0.2	0.7	V
AFT tolerance 1	d <sub>fa1</sub>	f = 38.9 MHz		±35	±70	kHz
AFT tolerance 2	d <sub>fa2</sub>	f = 38.0 MHz		±35	±70	kHz
AFT tolerance 3	d <sub>fa3</sub>	f = 39.5 MHz		±35	±70	kHz
AFT detection sensitivity	S <sub>f</sub>	RL = 100 kΩ/100 kΩ	40	80	120	mV/kHz
AFT dead zone	f <sub>da</sub>			30	60	kHz
APC pull-in range (U)	f <sub>pu</sub>		1.5	2.0		MHz
APC pull-in range (L)	f <sub>pl</sub>		1.5	2.0		MHz
VCO maximum frequency range (U)	d <sub>fu</sub>		1.5	2.0		MHz
VCO maximum frequency range (L)	d <sub>fl</sub>		1.5	2.0		MHz
VCO control sensitivity	β		2.0	4.0	8.0	kHz/mV

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
N trap1 (4.75 MHz)	NT1	wrt 1 MHz	-30	-35		dB
N trap2 (5.25 MHz)	NT2	wrt 1 MHz	-19	-24		dB
BG trap1 (5.75 MHz)	BT1	wrt 1 MHz	-27	-32		dB
BG trap2 (6.1 MHz)	BT2	wrt 1 MHz	-20	-25		dB
BG trap3 (5.85 MHz)	BT3	wrt 1 MHz	-27	-32		dB
I trap1 (6.25 MHz)	IT1	wrt 1 MHz	-25	-30		dB
I trap2 (6.8 MHz)	IT2	wrt 1 MHz	-15	-20		dB
DK trap1 (6.75 MHz)	DT1	wrt 1 MHz	-25	-30		dB
Group delay 1 NTSC (3.0 MHz)	NGD1	wrt 1 MHz	10	40	70	ns
Group delay 1-1 NTSC (3.5 MHz)	NGD1-1	wrt 1 MHz	70	120	170	ns
Group delay 2 BG (4 MHz)	BGD2	wrt 1 MHz	30	60	90	ns
Group delay 2-1 BG (4.4 MHz)	BGD2-1	wrt 1 MHz	100	150	200	ns
Group delay 3 I (4 MHz)	IGD3	wrt 1 MHz	0	30	60	ns
Group delay 3-1 I (4.4 MHz)	IGD3-1	wrt 1 MHz	30	60	90	ns
Group delay 4 DK (4 MHz)	DGD4	wrt 1 MHz	0	15	30	ns
Group delay 4-1 DK (4.4 MHz)	DGD4-1	wrt 1 MHz	0	30	60	ns
[1st SIF Block]						
Conversion gain	Vg	fp = 5.5 MHz, Vi = 500μV	26	32	38	dB
SIF carrier output level	So	Vi = 10 mV		100		mVrms
First SIF maximum input	Simax	So ±2 dB		106		dBμV
First SIF input resistance	Ris			5.0	6.0	kΩ
First SIF input capacitance	Cis			3	6	pF
[SIF Block]						
Limiting sensitivity	Vi(lim)	fp = 5.5 MHz, ΔF = ±30 kHz at 400 Hz	46	52	58	dBμV
FM detector output voltage	Vo(FM)		560	700	850	mVrms
AM rejection ratio	AMR	AM = 30% at 400 Hz	50	60		dB
Total harmonic distortion	THD	f = 5.5 MHz, ΔF = ±30 kHz		0.3	1.0	%
FM detector output S/N	S/N(FM)		55	60		dB
BPF 3-dB bandwidth	BW			±100		kHz
PAL de-emphasis	Pdeem	fm = 3 kHz		-3		dB
NTSC de-emphasis	Ndeem	fm = 2 kHz		-3		dB
PAL/NT audio voltage gain difference	GD			6		dB
[Others]						
4-MHz level (during external input)	X4MIN	Terminated	86			dBμ
SIF system SW threshold voltage	V10, V11			1.4		V
IF system SW threshold resistance	V12				270	kΩ
Split/inter SW	V16			0.5		V

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### System Switching

- SIF system switch

The SIF system is switched by setting pins A (pin 13) and B (pin 14) to GND or OPEN.

A	B	B/G	I	D/K	M/N	FM DET LEVEL	De-emphasis
GND	GND				O	6 dB	75 $\mu$ s
GND	OPEN			O		0 dB	50 $\mu$ s
OPEN	GND		O			0 dB	50 $\mu$ s
OPEN	OPEN	O				0 dB	50 $\mu$ s

Note: "O" indicates that the system is selected.

- IF system switch

38.9 MHz is selected as the IF frequency by leaving pin 15 (crystal oscillation) open. 38 MHz is selected by adding 220 k $\Omega$  between pin 15 and GND. This device can also select 39.5 MHz operation by adding a 220 k $\Omega$  resistor between pin 15 and V<sub>CC</sub>.

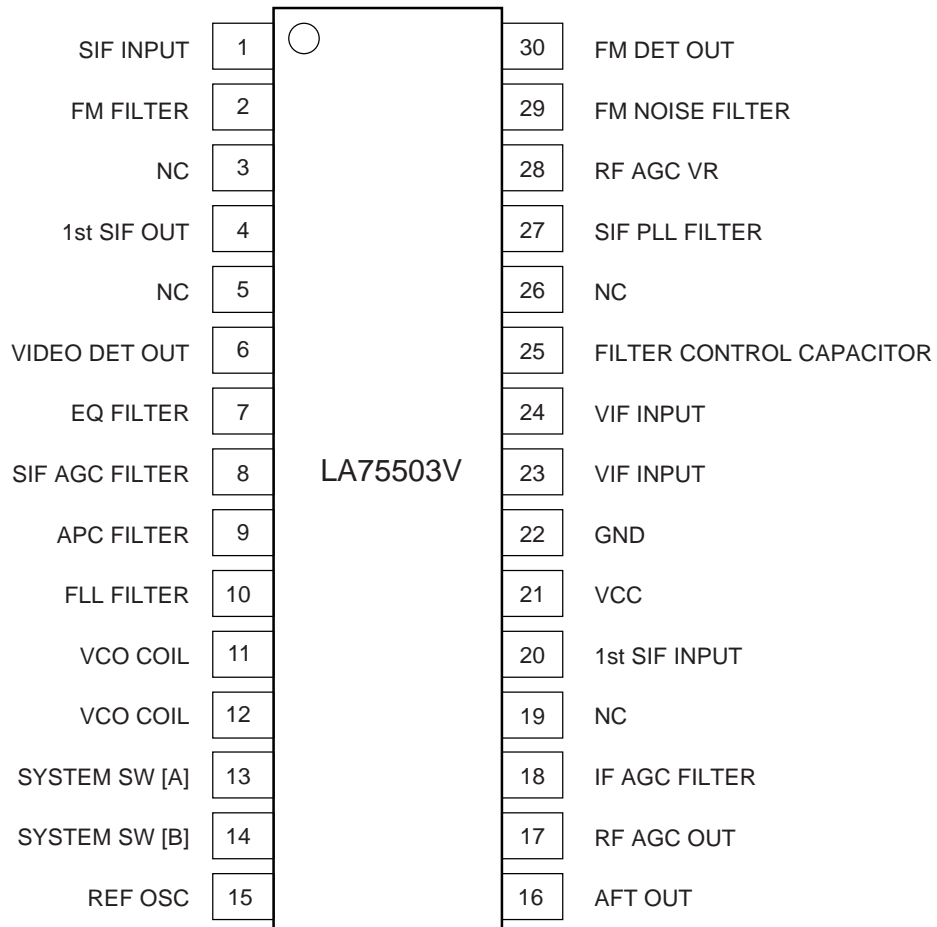
- Split/inter carrier switch

Inter carrier is selected by setting the first SIF input (pin 20) to GND.

### Sound Trap

The trapping point of the sound trap is set approximately 250 kHz above the SIF center frequency of each mode to improve the video S/N. Therefore, design using split specifications is preferable.

### Pin Assignment

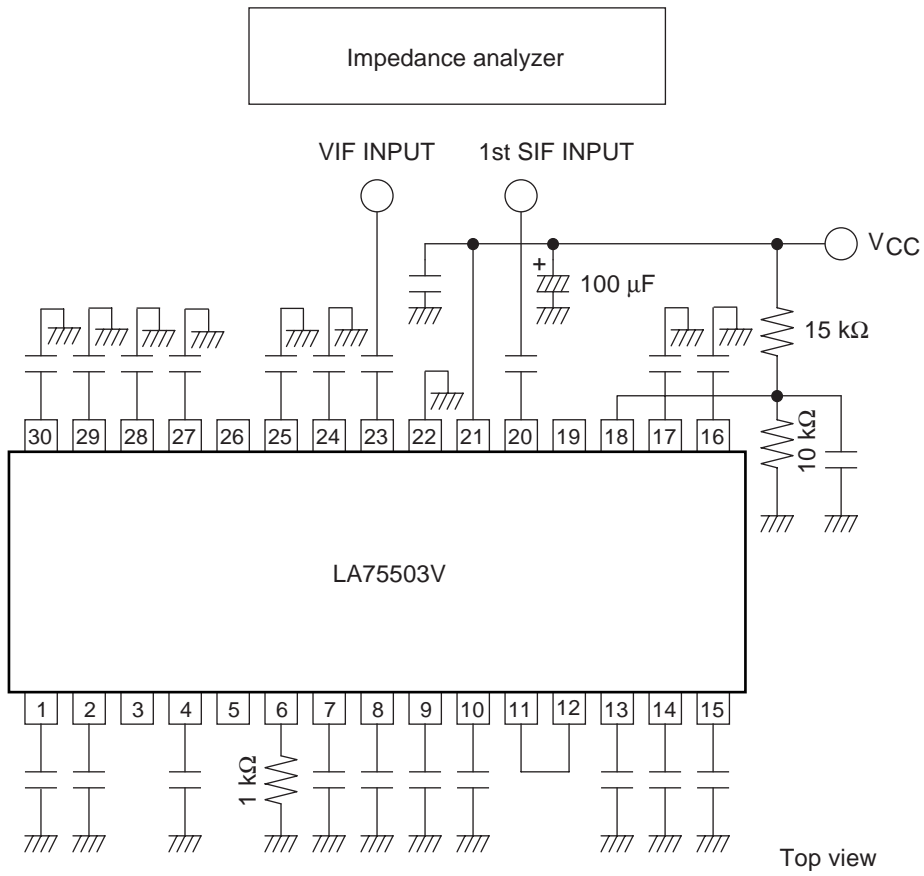


Top view

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## Test Circuit

Input Impedance Measuring Circuit (VIF, First SIF input impedance)



\*: 0.01  $\mu$ F in case of unspecified capacitor

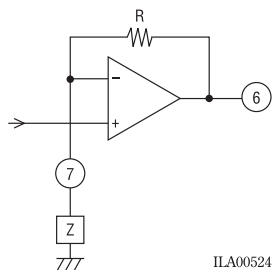
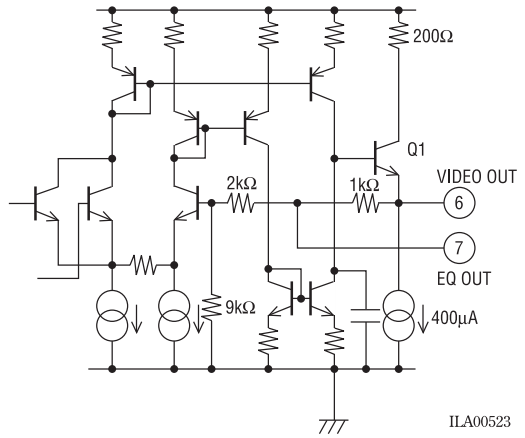
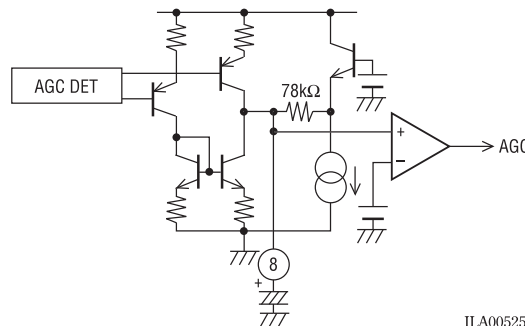
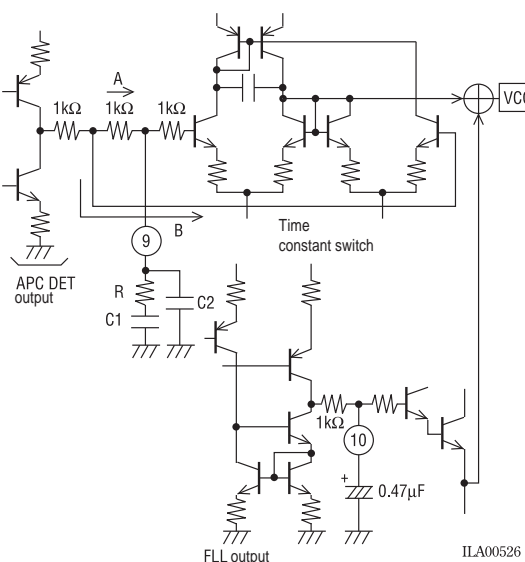
Pin Functions

Pin No.	Pin	Pin Function	Internal Circuit
1	SIF INPUT	Inputs the SIF signal from the first SIF output. Set the input level to 90 dBμV or lower because of the dynamic range of the internal filter.	<p style="text-align: right;">ILA00519</p>
2	FM FILTER	This is the FM feedback filter pin. It is composed of a C and R filters. 1 μF is normally used as the capacitance. If the capacitance is a low value, the audio output level is small at low frequencies. Moreover, the audio output level can be made smaller by increasing the resistance connected in series. Use a resistance of 3 kΩ or higher.	<p style="text-align: right;">ILA00520</p>
3	NC	Not connected	
4	1st SIF OUT	This is the first SIF output. In case of inter carrier, the chroma carrier is bigger than split carrier applications, so that it is recommended to connect a filter externally.  Filter example <p style="text-align: right;">ILA00522</p>	<p style="text-align: right;">ILA00521</p>

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Pin No.	Pin	Pin Function	Internal Circuit
5	NC	Not connected	
6 7	VIDEO-OUT EQ-OUT	<p>Pin 6 is the video output pin.</p> <p>The EQ amplifier can be thought of as shown below.</p>  <p style="text-align: center;">ILA00524</p> <p>Therefore, the peak gain of the EQ amplifier is determined by <math>A_v = 1 + R/Z</math>.</p> <p>However, note that the LA75503V being an IC with <math>V_{CC} = 5\text{ V}</math>, setting too large an amplitude causes distortion in the <math>V_{CC}</math> side. Use so that the white level is 4 V or less.</p>	 <p style="text-align: right;">ILA00523</p>
8	SIF AGC FILTER	<p>Pin 8 is the SIF AGC filter pin.</p> <p>Use this pin with a capacitance between 0.01 <math>\mu\text{F}</math> and 0.1 <math>\mu\text{F}</math>.</p>	 <p style="text-align: right;">ILA00525</p>
9 10	APC FILTER FLL FILTER	<p>Pin 9 is the PLL detector APC filter pin.</p> <p>Normally the following are used:</p> <p><math>R = 330\ \Omega</math></p> <p><math>C1 = 0.47\ \mu\text{F}</math> to <math>1\ \mu\text{F}</math></p> <p><math>C2 = 100\ \text{pF}</math></p> <p><math>C1 = 1\ \mu\text{F}</math> is effective for the overmodulation characteristics.</p> <p>When the PLL is locked, the signal passes via the path marked A in the figure, and when PLL is unlocked and in weak signal, the signal passes via the path marked B in the figure. The PLL loop gain can thus be switched in this manner.</p> <p>Pin 10 is a VCO automatic control FLL filter pin.</p> <p>Since it operates always on a small current, using a larger capacitance results in a slower response.</p> <p>Normally, a capacitance between 0.47 <math>\mu\text{F}</math> and 1 <math>\mu\text{F}</math> is used.</p> <p>Moreover, the control range for this pin is between about 3 V to 4.7 V. Since this range is determined when adjusting the VCO tank circuit, set the design center of L and C of VCO so that the voltage of pin 10 is 3.6 V.</p>	 <p style="text-align: right;">ILA00526</p>

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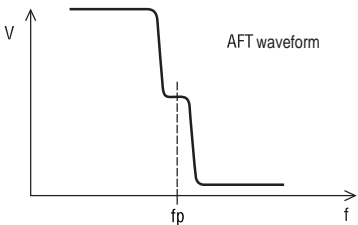
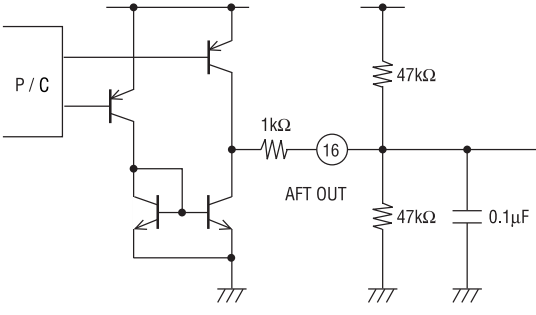
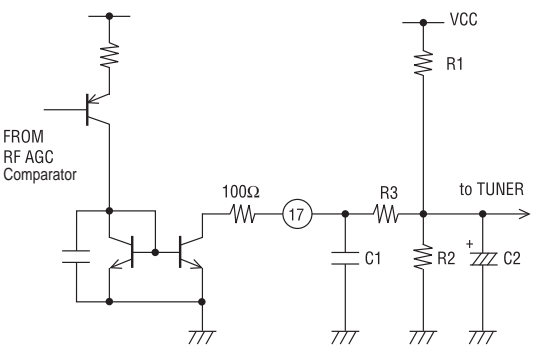
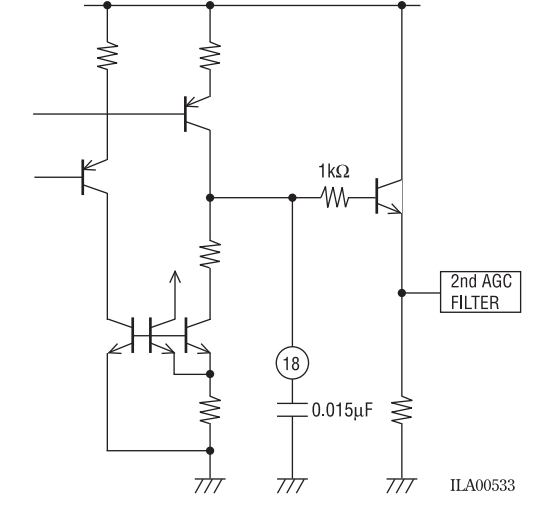
Pin No.	Pin	Pin Function	Internal Circuit
11 12	VCO COIL	<p>This is the VCO tank circuit for the PLL detector. Use a tuning capacitance of 24 pF. Use L and C specifications that are accurate to <math>\pm 2\%</math>. Also, design the L and C values so that the voltage of pin 10 is 3.6 V when PLL is locked while using the IF center frequency.</p>	<p style="text-align: right;">ILA00527</p>
13 14	SYSTEM SW	<p>This is the system switch pin. The transistor turns ON when the pin voltage from the circuit becomes approx. 1.4 V.</p>	<p style="text-align: right;">ILA00528</p>
15	REF OSC	<p>This pin can be used both as the crystal resonator pin and IF switch. The 38-MHz mode is selected by inserting 220 kΩ between pin 15 and GND, the 38.9 MHz mode by leaving the pin open, and the 39.5-MHz mode by inserting 220 kΩ between pin 15 and V<sub>CC</sub>. 4-MHz input is possible from this pin. In the case of 4-MHz external input, input 86 dBμ or more.</p>	<p style="text-align: right;">ILA00529</p>

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Pin No.	Pin	Pin Function	Internal Circuit
16	AFT OUT	<p>Pin 16 is the AFT output pin.</p> <p>Use external resistors of 47 kΩ and a filter capacitance 0.1 μF.</p> <p>The AFT circuit generates the AFT voltage by comparing the signal obtained by dividing the 4-MHz reference frequency with the signal obtained by dividing VCO.</p> <p>Since it uses a digital phase comparator, a dead zone exists in the AFT center.</p>  <p>ILA00531</p>	 <p>ILA00530</p>
17	RF AGC OUT	<p>Pin 17 is the RF AGC output.</p> <p>RF AGC max is determined by R1 and R2.</p> <p>RF AGC min is determined by R3 and R4.</p> <p>Capacitor C1 prevents oscillation and capacitor C2 is the RF AGC filter.</p> <p>Normally 30 kΩ is used for R1, but if the tuner's F/E transistor is GaAS, the gate's impedance is lower, so use approx. 10 kΩ.</p>	 <p>ILA00532</p>
18	IF AGC FILTER	<p>Pin 18 is the IF AGC filter pin.</p> <p>Normally, 0.01 μF to 0.02 μF polyester film capacitor is used.</p> <p>Determine the impedance based on H-SAG and AGC speed.</p>	 <p>ILA00533</p>
19	NC	Not connected	

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Pin No.	Pin	Pin Function	Internal Circuit
20	1st SIF INPUT	<p>Pin 20 can be used both as the First SIF IN and inter/split switch pins.</p> <p>In the case of inter carrier, connect pin 20 to GND.</p> <p>When a sound saw filter is added, the matching loss can be decreased by inserting L to neutralize the IC input capacitance and saw filter output capacitance.</p>	<p style="text-align: right;">ILA00534</p>
21	V <sub>CC</sub>	Connect the decoupling capacitor as close as possible.	
22	GND		
23 24	VIF INPUT	<p>Pins 23 and 24 are VIF input pins.</p> <p>To reduce the loss of signal through a saw filter, input registers are set to 2 kΩ.</p> <p>VIF amplifier has three capacitive coupling amplifiers, direct connection from a saw filter is available.</p>	<p style="text-align: right;">ILA00536</p>

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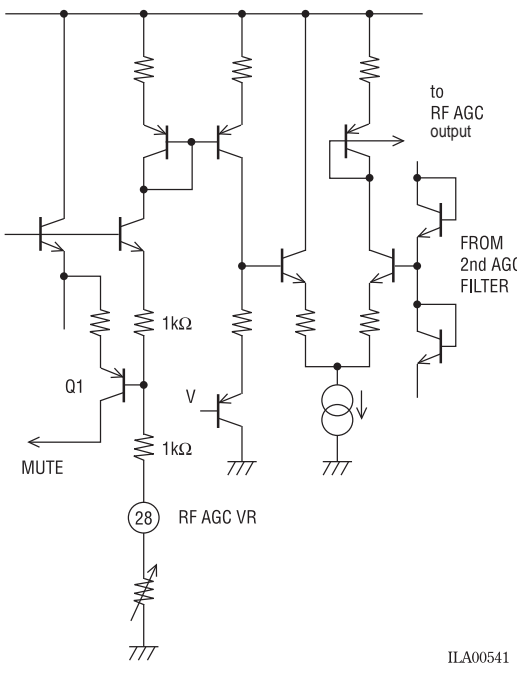
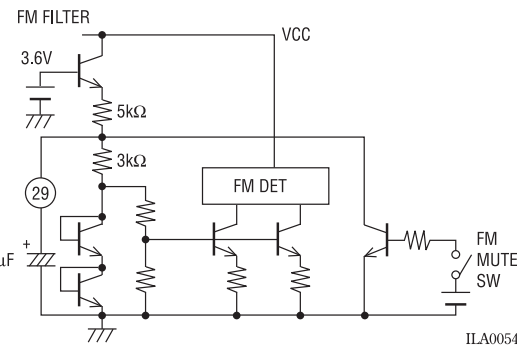
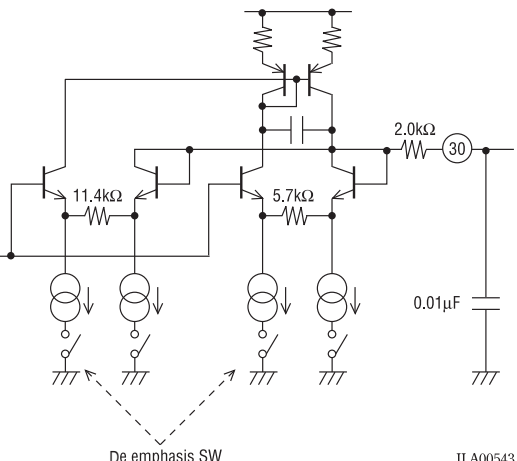
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Pin No.	Pin	Pin Function	Internal Circuit
25	FILTER CONTROL CAPACITOR	<p>Internal filters (i.e. sound carrier BPF and sound carrier trap) are tuned using the capacitor connected to pin 25.</p> <p>A value between 0.47 <math>\mu\text{F}</math> and 1 <math>\mu\text{F}</math> is considered desirable taking video S/N, and AM and PM noise into consideration.</p>	<p>The diagram shows a multi-stage transistor circuit. A capacitor is connected to pin 25, labeled 'FIL CONT'. The circuit includes several transistors, resistors, and a reference voltage 'Vref'. An output is labeled 'to FILTER CONTROL'. The diagram is identified as ILA00538.</p>
26	NC	Not connected	
27	SIF PLL FILTER	<p>Pin 27 is the SIF PLL filter pin.</p> <p>Normally use the following values.</p> <p>R: 3 k<math>\Omega</math></p> <p>C1: 0.01 <math>\mu\text{F}</math></p> <p>C2: 1000 pF</p> <p>The graph plots 'level' on the vertical axis against frequency 'f' on the horizontal axis. Two curves are shown: a wider, lower curve labeled 'Large R value' and a narrower, higher curve labeled 'Small R value'. The diagram is identified as ILA00540.</p> <p>A large R value (6 k<math>\Omega</math> or lower) results in high-pass FM detection output noise. A smaller R value results in low-pass noise.</p>	<p>The diagram shows a complex transistor circuit for the SIF PLL filter. It includes several transistors, resistors, and two capacitors, C1 and C2, connected to pin 27. The output is connected to a block labeled 'SIF VCO'. The diagram is identified as ILA00539.</p>

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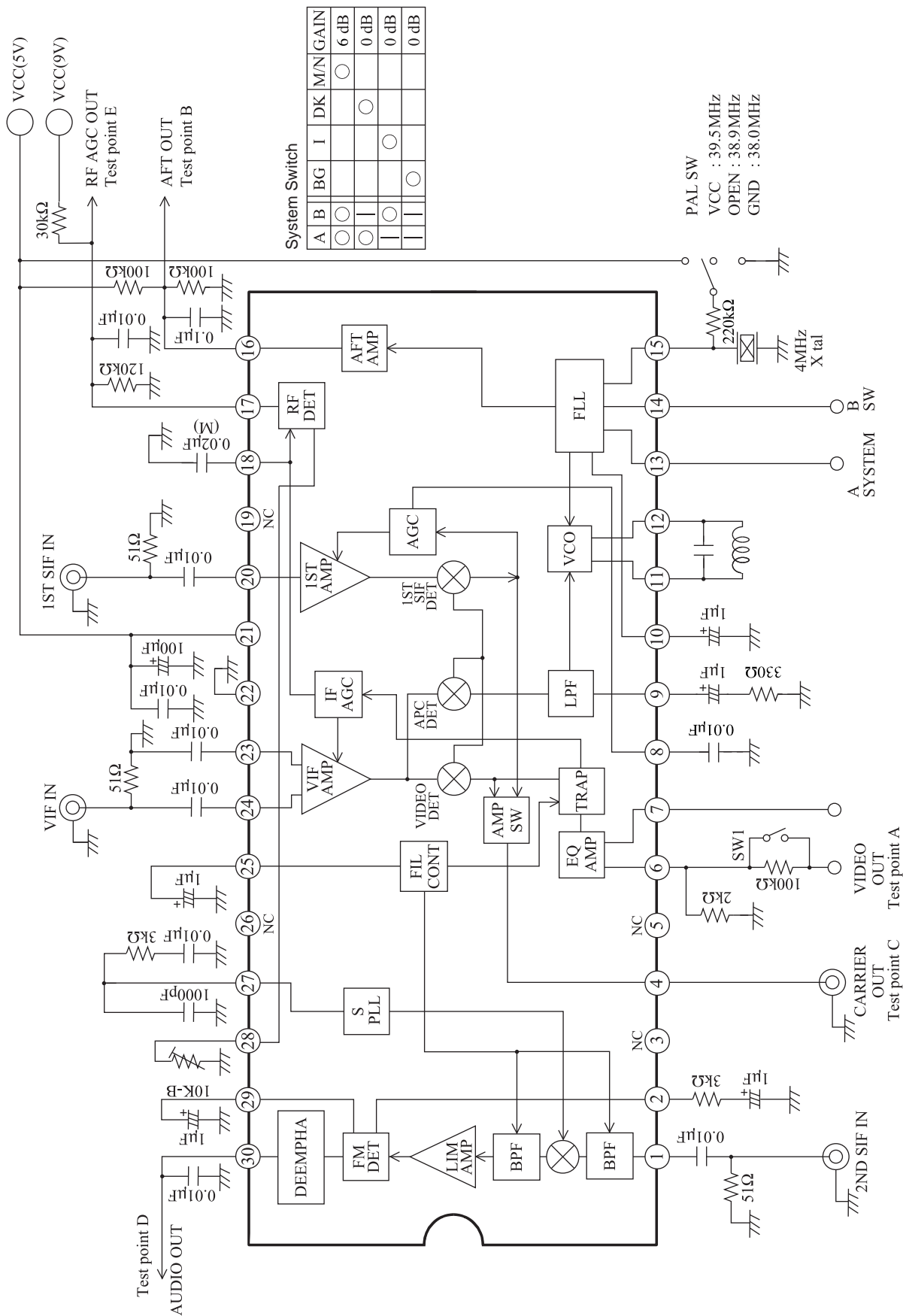
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Pin No.	Pin	Pin Function	Internal Circuit
28	RF AGC VR	<p>Pin 28 is the RF AGC VR pin.</p> <p>When this pin is connected to GND, no signal is appeared on pin 6 and pin 30.</p>	 <p style="text-align: right;">ILA00541</p>
29	FM FILTER	<p>Pin 29 is the FM filter pin.</p> <p>Use a capacitance between 0.01 μF and 1 μF.</p>	 <p style="text-align: right;">ILA00542</p>
30	FM DET OUT	<p>Pin 30 is the FM output pin.</p> <p>The built-in differential amplifier determines and switches the de-emphasis resistance value.</p> <p>PAL: <math>5\text{ k} \times 0.01\text{ }\mu\text{F}</math></p> <p>NT: <math>7.5\text{ k} \times 0.01\text{ }\mu\text{F}</math></p>	 <p style="text-align: right;">ILA00543</p>



Test Circuit



System Switch		I	DK	M/N	GAIN
A	B	○	○	○	6 dB
○	○	○	○	○	0 dB
○	○	○	○	○	0 dB
○	○	○	○	○	0 dB

PAL SW  
 VCC : 39.5MHz  
 OPEN : 38.9MHz  
 GND : 38.0MHz

Top view [IC]

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