CX74017

RF Transceiver for Single, Dual, or Tri-Band GSM/GPRS Applications

Conexant's CX74017 transceiver is a highly integrated device for use in multi-band, Global System for Mobile communications® (GSM®) applications or General Packet Radio Service (GPRS) applications. The device requires a minimal number of external components to complete a GSM radio subsystem.

The device's receiver uses a direct down-conversion architecture that eliminates the need for Intermediate Frequency (IF) components. The receiver consists of integrated Low Noise Amplifiers (LNAs), a quadrature demodulator, tunable receiver baseband filters, and a DC offset correction sequencer.

In the transmit path, the device consists of an In-phase and Quadrature (I/Q) modulator within a frequency translation loop designed to perform frequency up-conversion with high output spectral purity. This loop also contains a phase-frequency detector, a charge pump, a mixer, and buffers for the required isolation between RF output, Local Oscillator (LO), and IF ports. The transmitter also includes the entire transmit Voltage Controlled Oscillator (VCO) structure with no external tank required.

The CX74017 also features an integrated, fully programmable, fractional-N synthesizer suitable for GPRS multi-slot operation. With the exception of the loop filter, the frequency synthesizer function is completely on-chip.

The CX74017 device package and pin configuration are shown in Figure 1. A functional block diagram is shown in Figure 2. The signal pin assignments and functional pin descriptions are provided in Table 1.

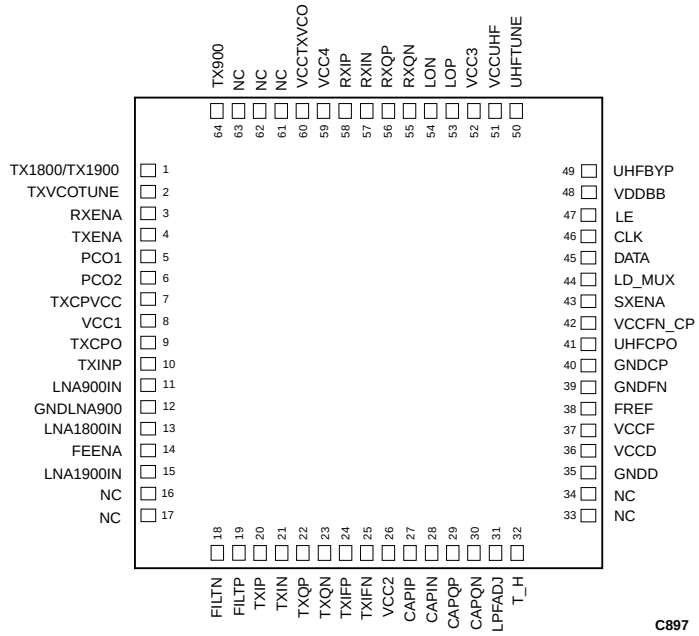

Figure 1. CX74017 Pinout – 64-Pin LGA (Top View)

Features

- Direct down-conversion receiver eliminates the external image reject/IF filters
- Integrated triple band LNAs with three separate inputs
- 18 dB of RF gain range and 100 dB of baseband gain range
- Gain selectable in 2 dB steps
- Integrated receive baseband filters with tunable bandwidth
- Integrated DC offset correction sequencer
- Reduced filtering requirements with translation loop transmit architecture
- Integrated transmit VCOs
- Wide RF range for dual/ triple band operation
- Single integrated, fully programmable fractional-N synthesizer suitable for multi-slot GPRS operation
- Fully integrated UHF VCO
- Separate enable lines for power management transmit, receive, and synthesizer modes
- Supply voltage down to 2.7 V
- Low external component count
- Optional bypass of baseband filtering for use with high dynamic range Analog/Digital Converters (ADCs) for current savings
- Interfaces to low dynamic range ADC
- No digital post-processing required
- 64-pin Land Grid Array (LGA) 9x9mm package

Applications

- GSM single, dual, or tri-band handsets with multislot capability
- GPRS handsets and modules

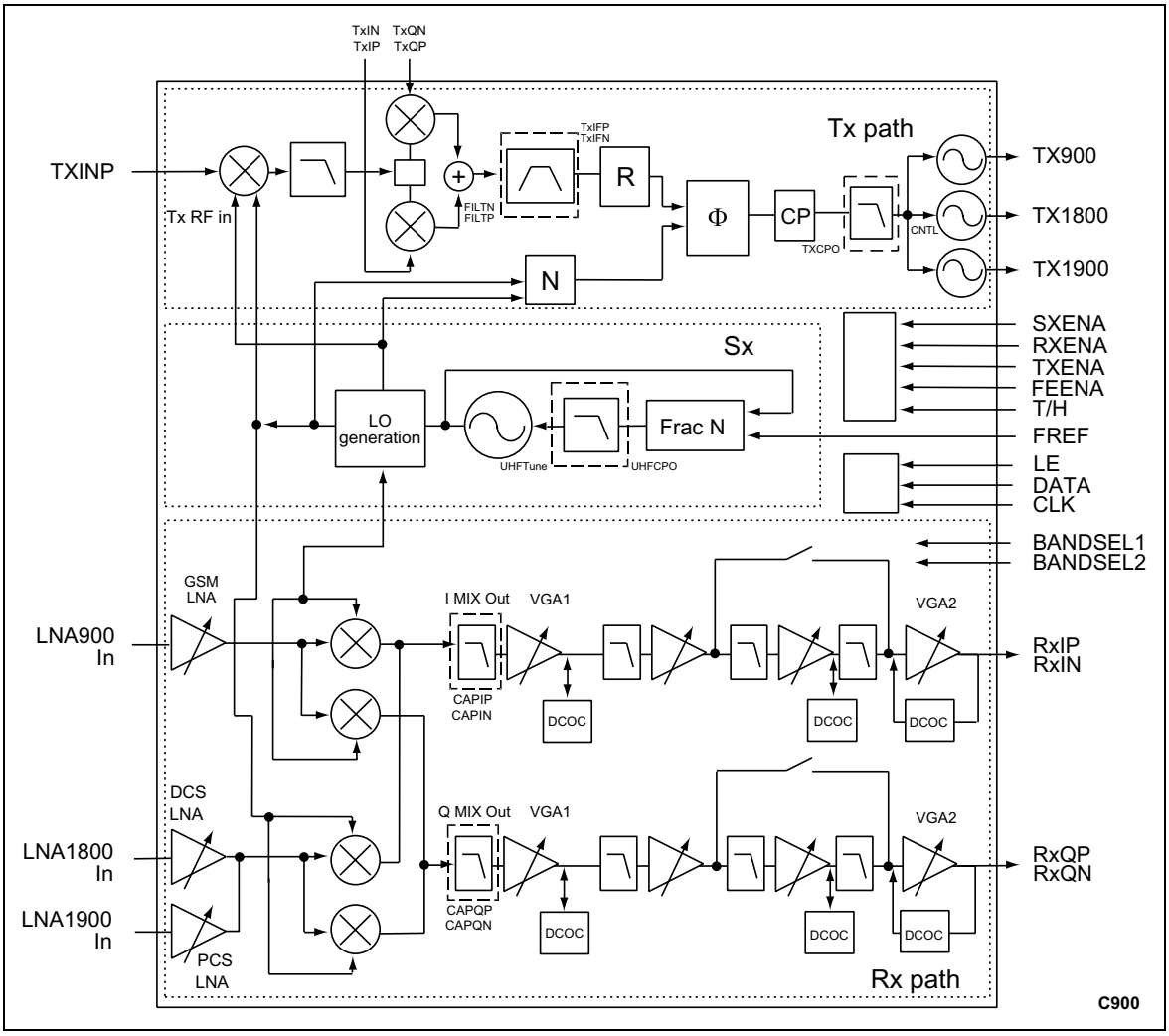

Figure 2. CX74017 Transceiver Block Diagram

Technical Description

The CX74017 transceiver contains a receive path, a transmit path, and a synthesizer section as shown in Figure 2. The receive path consists of a triple band integrated LNA, quadrature demodulator section that performs direct down conversion, and baseband amplifier circuitry with I/Q outputs and three stages of DC offset correction. The transmit path consists of a vector modulator within a translation loop for frequency up-conversion. The fully integrated on-chip oscillator locked in an integrated fractional-N synthesizer loop comprises the synthesizer section. Each section of the CX74017 is separately enabled via the enable signals TXENA, RXENA, and SXENA.

To control different modes of operation, a serial 24-bit word (bits S0 to S23) is written to the on-chip register. This 24-bit word is programmed using the 3-wire input signals CLK, DATA, and LE. To ensure that the data stays latched, the CX74017 must continue to be supplied with voltage although none of the sections needs to be enabled. A separate power supply pin is provided for the digital sections that allow power supply operation compatible with modern digital baseband devices.

Receive Path

The receive path of the CX74017 consists of an RF section and a baseband section. The RF section includes a programmable gain LNA and quadrature demodulator for each band. The baseband I/Q paths are made up of cascaded amplifier and low pass filter sections. An off-chip capacitor and three fixed poles of on-chip filtering provide rejection of strong in- and out-of-band blockers. A tunable, four-pole filter provides rejection of the adjacent channel blockers. Incorporated within the fixed pole filters are two switchable gain stages of 18 dB and 12 dB gain steps, respectively. Incorporated into the four- pole tunable filter is another programmable gain amplifier with a gain range from -2 to +32 dB, selectable in 2 dB steps. The output of the final filter feeds a rail-to-rail amplifier with a gain range from 0 to 30 dB, selectable in 6 dB steps.

Table 1. CX74017 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	TX1800/TX1900	DCS and PCS transmit VCO output (NC)	33	NC	No connect
2	TXVCOTUNE	Transmit VCO control input	34	NC	No connect
3	RXENA	Receiver enable input	35	GNDD	Synthesizer digital ground
4	TXENA	Transmitter enable input	36	VCCD	Synthesizer digital supply
5	PCO1	Bi-directional control	37	VCCF	Synthesizer analog supply
6	PCO2	Bi-directional control	38	FREF	Crystal reference input
7	TXCPVCC	Transmit charge pump supply	39	GNDFN	Synthesizer analog ground
8	VCC1	LNA/transmit charge pump supply (LNA supply)	40	GNDCP	Synthesizer charge pump ground
9	TXCPO	Translation loop charge pump output	41	UHFCPO	Synthesizer charge pump output
10	TXINP	Translation loop feedback input	42	VCCFN_CP	Synthesizer charge pump supply
11	LNA900IN	EGSM LNA input	43	SXENA	Synthesizer enable input
12	GNDLNA900	EGSM LNA emitter ground	44	LD_MUX	Synthesizer test output
13	LNA1800IN	DCS LNA input	45	DATA	Data
14	FEENA	Bi-directional front end enable input/output	46	CLK	Clock
15	LNA1900IN	PCS LNA input	47	LE	Latch enable
16	NC	No connect	48	VDDBB	Digital CMOS supply
17	NC	No connect	49	UHFBYP	Bypass capacitor for UHF VCO (NC)
18	FILTN	TX IF output negative	50	UHFTUNE	UHF VCO control input (NC)
19	FILTP	TX IF output positive	51	VCCUHF	UHF VCO supply
20	TXIP	TX I baseband input positive	52	VCC3	LO chain supply
21	TXIN	TX I baseband input negative	53	LOP	External LO input/internal LO monitor positive
22	TXQP	TX Q baseband input positive	54	LON	External LO input/internal LO monitor negative
23	TXQN	TX Q baseband input negative	55	RXQN	Receiver output Q negative
24	TXIFP	TX IF filter output positive	56	RXQP	Receiver output Q positive
25	TXINN	TX IF filter output negative	57	RXIN	Receiver output I negative
26	VCC2	Mixer/baseband supply	58	RXIP	Receiver output I positive
27	CAPIP	Capacitor filter I positive	59	VCC4	Baseband supply
28	CAPIN	Capacitor filter I negative	60	VCCTXVCO	Transmit VCO supply (NC)
29	CAPQP	Capacitor filter Q positive	61	NC	No connect
30	CAPQN	Capacitor filter Q negative	62	NC	No connect
31	LPFADJ	LPF corner resistor	63	NC	No connect
32	T_H	Track and hold initiate	64	TX900	EGSM transmit VCO

The receiver architecture intrinsically defeats DC offsets generated through LO and blocker self-mixing.

Random input referred offsets generated in the CX74017 must be calibrated out. Three calibration loops are required to ensure that DC offsets do not overload the baseband chain at any point. After compensation, the correction voltages are held in capacitors for the duration of the receive slot(s). Internal, on-chip timing is provided to generate the track and hold signals for these calibration loops. The timing for these signals is relative to the T_H signal.

The timing diagram for the calibration sequence for one DC offset correction in reference to the receive slot is shown in Figure 3. First the CX74017 receiver is turned on (RXENA is set high). After time T1, the track and hold signal, T_H, places the DC compensation circuitry in the track mode for time T2. Then, there is a settling time, T3, before the front end is turned on (FEENA is set high). The front end must be turned on for time T4 before the receive slot begins.

For more flexibility with baseband interfaces, the four-pole filter, its associated Variable Gain Amplifier (VGA), and DC offset correction can be bypassed and turned off for current savings.

To minimize the post-PA filtering requirements, and any additional post-PA losses, the transmit path consists of a vector modulator within a frequency translation loop. The translation

loop consists of a Phase Frequency Detector (PFD) and charge pump, a mixer (with an operating range of 800 MHz to 2 GHz), an in-loop modulator, and two transmit VCOs. As shown in Figure 2, the loop functions as a Phase-Locked Loop (PLL) with a mixer and modulator in the feedback path. The on-chip Low-Pass Filter (LPF) following the mixer attenuates the unwanted sideband as well as harmonics. The two on-chip transmit VCOs are designed to meet EGSM, DCS, and PCS requirements.

Synthesizer Section

The CX74017 includes a fully integrated UHF VCO with an on-chip LC tank.

A single fractional-N synthesizer can phase lock the local oscillator used in both the transmit and the receive path to a precision frequency reference source. Fractional-N operation offers low phase noise and fast settling times, allowing for multiple slot applications such as GPRS. The frequency stepping function of the CX74017, with a 1 Hz accuracy, allows triple band operation in both transmit and receive bands without the requirement of a large VCO tuning range using only a single integrated on-chip UHF VCO.

Control Interface

The transceiver and synthesizer are controlled by a three-wire interface. The receiver gain control, as well as the division ratios and charge pump currents in the synthesizer and transmitter, can be programmed using 24-bit words. The transmitter, receiver, and synthesizer can be enabled separately.

Electrical and Mechanical Specifications

The absolute maximum ratings of the CX74017 are provided in Table 2. The recommended operating conditions are specified in Table 3. Table 4 provides the power consumption of the CX74017 in various operational modes. Electrical specifications are provided in Tables 5, 6, 7 and 8. Table 9 contains the band selection truth table. Table 10 and Table 11 show the function settings of the control bits in the serial interface. Figure 4 depicts a summarized description of each programming word for quick reference. The three-wire serial interface timing diagram is shown in Figure 5. Figure 6 shows the 64-pin CX74017 LGA package dimensions.

Electrostatic Discharge

The CX74017 contains Class 1 devices. The following Electrostatic Discharge (ESD) precautions are recommended:

- Protective outer garments
- Handle device in ESD safeguarded work area
- Transport device in ESD shielded containers
- Monitor and test all ESD protection equipment
- Treat the CX74017 as extremely sensitive to ESD

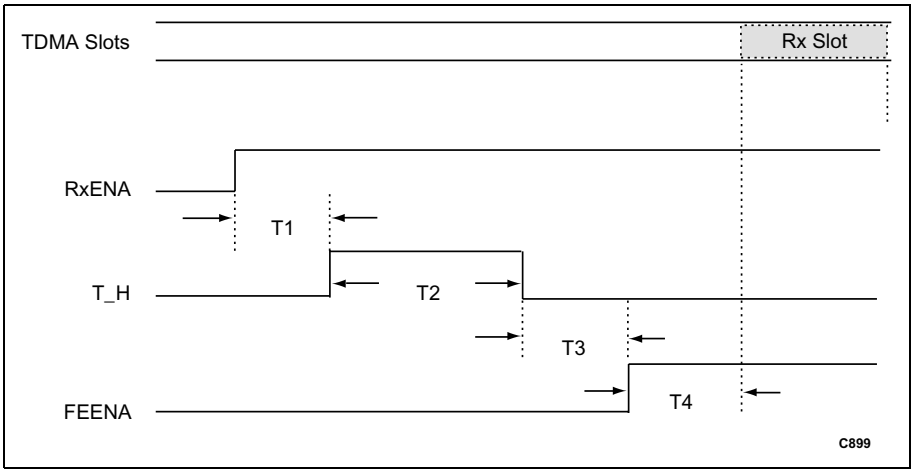

Figure 3. CX74017 Sample and Hold Timing Diagram

Table 2. CX74017 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply voltage (VCC)		3.6	V
Ambient operating temperature range	–40	+85	°C
Storage temperature range	–50	+125	°C
Input voltage range	GND	VCC	V
Maximum power dissipation		600	mW

NOTE: stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.

Table 3. CX74017 Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Power supply	2.7	3.0	3.6	V
Operating junction temperature	–40		+100	°C
Operating ambient temperature	–40		+85	°C

Table 4. Power Consumption Specifications
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Total supply current:	I_{CC}					
Rx mode, GSM		RXENA=SXENA=H		45		mA
Tx mode (no TIC VCO), GSM		TXENA=SXENA=H		45		mA
Synthesizer mode, GSM		SXENA=H		15		mA
TIC VCO, GSM				40		mA
Rx mode, DCS/PCS		RXENA=SXENA=H		55		mA
Tx mode, DCS/PCS		TXENA=SXENA=H		50		mA
Synthesizer mode, DCS/PCS		SXENA=H		20		mA
TIC VCO, DCS/PCS				40		mA
Sleep mode		@ VCC = 3.6 V RXENA=TXENA= SXENA=L		20		µA

Table 5. CX74017 Electrical Specifications – Receiver (1 of 4)
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
LNA: EGSM						
Input impedance	Z_{IN}	With external match		50		Ω
Input operating frequency	Band 1	EGSM Rx band	925		960	MHz
LNA Gain	G_{LNA}	High Gain Mode		15		dB
		Lowest Gain Mode		–3		dB
Voltage variation versus frequency		Over band 1		***** TBD *****		dB
Noise Figure	NF_{MIN}	High gain mode		2		dB
	NF_{MAX}	Low gain mode		9		dB
	NF_{BLOC}	With –25 dBm input blocker @ 10 MHz offset		3.5		dB
Input 1 dB compression point	IP1dB			–20		dBm

Table 5. CX74017 Electrical Specifications – Receiver (2 of 4)
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Mixer/LPF: EGSM						
Input IP2	IIP2	Referred to LNA input	65			dBm
Mixer voltage gain	G_{MIX}	High Gain		40		dB
		Low Gain		22		dB
Noise Figure	NF	High Gain		13		dB
		Low Gain		23		dB
Input 1 dB compression point	IP1dB	In-band (high gain)		–46		dBV
		In-band (low gain)		–26		dBV
		@ 3 MHz		–15		dBV
Output 1 dB compression point	OP1dB			–6		dBV
Blocker rejection		@ 3 MHz offset		–40		dB
		@ 1.6 MHz offset		–30		dB
		@ 600 kHz offset		–16		dB
		@ 400 kHz offset		–8		dB
I/Q amplitude imbalance					1	dB
I/Q phase imbalance			–3		3	degrees
Combined LNA/mixer NF	NF_{MIN}	High gain mode		3		dB
	NF_{MAX}	Low gain mode		26		dB
	NF_{BLOC}	With –25 dBm input blocker @ 10 MHz offset		4.5		dB
Combined input 1 dB compression point	IP1dB	In-band (high gain)			–45	dBm
		In-band (low gain)			–22	dBm
		@ 3 MHz			–23	dBm
LNA: DCS						
Input impedance	Z_{IN}	With external match		50		Ω
Input operating frequency	Band 2	DCS/PCS Rx band	1805		1990	MHz
LNA gain	G_{LNA}	High gain mode		15		dB
		Lowest gain mode		–3		dB
Voltage variation versus frequency		Over band 1		***** TBD *****		dB
Noise Figure	NF_{MIN}	High gain mode		3		dB
	NF_{MAX}	Low gain mode		10		dB
	NF_{BLOC}	With –28 dBm input blocker @ 10 MHz offset		4.5		dB
Input 1 dB compression point	IP1dB			–22		dBm
LNA: PCS						
Input impedance	Z_{IN}	With external match		50		Ω
Input operating frequency	Band 2	DCS/PCS Rx band	1805		1990	MHz
LNA gain	G_{LNA}	High gain mode		15		dB
		Lowest gain mode		–3		dB
Voltage variation versus frequency		Over band 1		***** TBD *****		dB
Noise Figure	NF_{MIN}	High gain mode		3		dB
	NF_{MAX}	Low gain mode		10		dB
	NF_{BLOC}	With –28 dBm input blocker @ 10 MHz offset		4.5		dB

Table 5. CX74017 Electrical Specifications – Receiver (3 of 4)
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
LNA: PCS (continued)						
Noise Figure	NF_{MIN}	High gain mode		3		dB
	NF_{MAX}	Low gain mode		10		dB
	NF_{BLOC}	With –28 dBm input blocker @ 10 MHz offset		4.5		dB
Input 1 dB compression point	IP1dB			–22		dBm
Mixer/LPF: DCS/PCS						
Input IP2	IIP2	Referred to LNA input	55			dBm
Mixer voltage gain	Gmix	High gain		40		dB
		Low gain		22		dB
Noise Figure	NF	High gain		15		dB
		Low gain		25		dB
Input 1 dB comp point	IP1dB	In-band (high gain)		–46		dBV
		In-band (low gain)		–26		dBV
		@ 3 MHz		–15		dBV
Output 1 dB compression point	OP1dB			–6		dBV
Blocker rejection		@ 3 MHz offset		–40		dB
		@ 1.6 MHz offset		–30		dB
		@ 600 kHz offset		–16		dB
		@ 400 kHz offset		–8		dB
I/Q Amplitude imbalance					1	dB
I/Q Phase imbalance			–3		3	degrees
Combined LNA/mixer NF	NF_{MIN}	Highest gain mode		4.2		dB
	NF_{MAX}	Lowest gain mode		28		dB
	NF_{BLOC}	With –28 dBm input blocker @ 10 MHz offset		5.7		dB
Combined input 1dB compression point	IP1dB	In-band (high gain)		–45		dBm
		In-band (low gain)		–22		dBm
		@ 3 MHz		–23		dBm
First Active LPF						
Gain	A_V	High gain		10		dB
		Low gain		–2		dB
Corner frequency	F_C			300		kHz
Output 1 dB compression point	OP1dB	High gain		–6		dBV
		Low gain		4		dBV
Rejection		@ 400 kHz		–6		dB
		@ 600 kHz		–13		dB
		@ 1.6 MHz		–30		dB
		@ 3 MHz		–42		dB
Group delay		Combined with mixer		2		µs
Group delay variation		Combined with mixer		50		ns
Voltage gain temperature coefficient				***** TBD *****		dB/°C

Table 5. CX74017 Electrical Specifications – Receiver (4 of 4)
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Second Active LPF						
Gain: Highest gain Lowest gain	A_V			 40 0		 dB dB
Gain step	dA_V			2		dB
Gain step accuracy			–0.5		0.5	dB
Input 1 dB compression point	IP1dB			–6		dBV
Corner frequency (programmable)	F_C		50		150	kHz
Corner frequency variation	dF_C	Without calibration With calibration	–15 –7		+15 +7	% %
Rejection (F_C=105 kHz)		@200 kHz @400 kHz @600 kHz		–11 –34 –48		dB dB dB
Group delay		F_C=105 kHz, (DC to 100 kHz)		3		µs
Group delay variation		F_C=105 kHz, (DC to 100 kHz)		300		ns
Second VGA						
Voltage gain: Highest gain Lowest gain Gain step	A_V			 30 0 6		 dB dB dB
Differential output amplitude		A_V = 30 dB A_V = 0 dB			2.5 0.1	V V
Output common mode voltage				1.35		V
Output offset voltage		With DC offset correction			±5	mV
Output impedance	Z_{OUT}			200		Ω

Table 6. CX74017 Electrical Specifications – Transmitter (1 of 2)
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
I/Q Modulator						
Differential input impedance	Z_{IN}			20		kΩ
Input signal level		Differential		1		Vp-p
Input common mode voltage range	V_{CM}		0.85	1.35	VCC – 1.3	V
Input offset voltage	V_{OS}				5	mV
Input frequency 3 dB bandwidth				3		MHz
Input common mode rejection ratio		F_{IN} = 100 kHz F_{IN} = 1 MHz		75 55		dB
Output operating frequency	F_{OUT}		70		110	MHz
Output impedance	Z_{OUT}	Per side		400		Ω
Output voltage	V_{OUT}		–20	–15		dBV
Output noise power	N_O	@ 10 MHz offset @ 1.8 MHz offset		–132 –130	–128 –126	dBc/Hz dBc/Hz
LO feedthrough				–45	–40	dBc
Sideband suppression			38	45		dB

Table 6. CX74017 Electrical Specifications – Transmitter (2 of 2)
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
I/Q Modulator (continued)						
Spurious		Modulation 2nd order		–70	–40	dBc
		Modulation 3rd order		–60	–55	dBc
Translational Loop						
Transmit frequency (input from VCO)	f_{TX}		800		2000	MHz
IF frequency	f_{IF}		70		110	MHz
Transmit input power	P_{IN}	With external 50 Ω termination	–13	–10	–7	dBm
Transmit input impedance	Z_{IN}			300// 0.3		Ω// pF
Transmitter output phase noise	N_O	@ 400 kHz offset			–118	dBc/Hz
		@ 1.8 MHz offset			–124	dBc/Hz
Translational Loop (continued)						
Charge pump output current: high impedance source/sink	I_{OUT}	CP = state 4		±2.0		mA
		CP = state 3		±1.5		mA
		CP = state 2		±.1.0		mA
		CP = state 1		±0.5		mA
Device turn-on and lock time (with respect to enable input)				30	100	µs
N divide ratio range			9		12	
R divide ratio			1		2	
EGSM Translation Loop VCO						
Frequency range	F_{RNG}		880		915	MHz
Power output	P_{OUT}		8	10	12	dBm
Phase noise	N_{PH}	At 10 MHz offset		–153	–150	dBc/Hz
		At 20 MHz offset		–165	–162	dBc/Hz
DCS Translation Loop VCO						
Frequency range	F_{RNG}		1710		1785	MHz
Power output	P_{OUT}		6	8	10	dBm
Phase noise	N_{PH}	At 20 MHz offset		–154	–152	dBc/Hz
PCS Translation Loop VCO						
Frequency range	F_{RNG}		1850		1910	MHz
Power output	P_{OUT}		6	8	10	dBm
Phase noise	N_{PH}	At 20 MHz offset		–154	–152	dBc/Hz

Table 7. CX74017 Electrical Specifications – Three-Wire Interface
(T_A=25° C, VCC = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Data to clock setup time (see Figure 5)	t_{CS}		50			ns
Data to clock hold time (see Figure 5)	t_{CH}		10			ns
Clock pulse width High (see Figure 5)	t_{CWH}		50			ns
Clock pulse width Low (see Figure 5)	t_{CWL}		50			ns
Clock to load enable setup time see (Figure 5)	t_{ES}		50			ns
Load enable pulse width (see Figure 5)	t_{EW}		50			ns
LE falling edge to clock rising edge (see Figure 5)	t_{EFC}		50			ns
RXENA setup time			50			ns
TXENA setup time			50			ns
SXENA setup time			50			ns
FEENA setup time			50			ns
Power supply range	VCC		2.7		3.6	V
Operating temperature range	T_A		–40	25	85	°C

Table 8. CX74017 Electrical Specifications – Synthesizer (1 of 2)
(T_A=25° C, VCCB = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Operating input frequency		RF	100		100	MHz
Reference input frequency			10	13	20	MHz
Phase detector frequency		RF		13		MHz
Input sensitivity		RF	–15			dBm
Reference oscillator sensitivity			0.5		VDD	V_{PEAK}
In-band phase noise		RF		–90		dBc/Hz
Spurious tones		RF		–75		dBc
Charge pump output current (can be programmed in four steps)		RF, V_{CP} = VDD/2 RF, V_{CP} = VDD/2 RF, V_{CP} = VDD/2 RF, V_{CP} = VDD/2		100 200 300 400		µA µA µA µA
Charge pump leakage current		0.5 < V_{CP} < VDD – 0.5		0.1		nA
Charge pump sink versus source mismatch		V_{CP} = VDD/2		5		%
Charge pump current versus voltage/temperature		0.5 < V_{CP} < VDD – 0.5		10		%
GSM LO						
Operating frequency	F_{VCO}		880		960	
Tuning voltage range			0.3		VCC – 0.5	
Tuning sensitivity	K_{VCO}			20		
Phase noise		@ 10 MHz offset @ 3 MHz offset @ 400 kHz offset		–144 –142 –125		

Table 8. CX74017 Electrical Specifications – Synthesizer (2 of 2)
(T_A=25° C, VCCB = 2.7 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
DCS/PCS LO						
Operating frequency	F_{VCO}		1710		1990	
Tuning voltage range			0.3		VCC – 0.5	
Tuning sensitivity	K_{VCO}			20		
Phase noise		@ 10 MHz offset @ 3 MHz offset @ 400 kHz offset		–138 –136 –119		

Table 9. CX74017 Operation Band Selection Logic

BANDSEL1	BANDSEL2	Band of Operation
0	0	GSM900
0	1	GSM900
1	0	DCS1800
1	1	PCS1900

Table 10. Control And Output States (1 of 2)

Symbol	Function	Description
EN	Program mode enable bits [1:0]	Logic 11 enables program mode
LNA	Gain [2]	Logic 1 selects the high gain mode of the LNA
MIX	[3]	Logic 1 selects the high gain mode of the RX mixer
LPF1	[4]	Logic 1 selects the high gain mode of the active LPF
VGA2	V2 gain steps [7:5]	s5 to s7 program the V2 gain in 6 dB increments: Logic 000 sets gain to 30 dB Logic 001 sets gain to 24 dB Logic 010 sets gain to 18 dB Logic 011 sets gain to 12 dB Logic 100 sets gain to 6 dB Logic 101 sets gain to 0 dB
AUX	[8]	Logic 1 activates 6 dB auxiliary gain
VGA1	V1 gain steps [11:9]	S9 to s11 program the V1 gain in 6 dB increments: Logic 000 sets gain to 30 dB Logic 001 sets gain to 24 dB Logic 010 sets gain to 18 dB Logic 011 sets gain to 12 dB Logic 100 sets gain to 6 dB Logic 101 sets gain to 0 dB
VGA1	V1 fine tune[13:12]	S12 and s13 program V1 in 2 dB increments: Logic 00 sets gain to 0 dB Logic 01 sets gain to 2 dB Logic 10 sets gain to 4 dB

Table 10. Control And Output States (2 of 2)

Symbol	Function	Description
TXCP	Tx charge pump bits[15:14]	Two bit translation loop charge pump setting: Logic 00 sets TXCP to 0.5 mA Logic 01 sets TXCP to 1.0 mA Logic 10 sets TXCP to 1.5 mA Logic 11 sets TXCP to 2.0 mA
TXN	N divider [17:16]	These two bits set N divider ratio: Logic 00 sets N to 9 Logic 01 sets N to 10 Logic 10 sets N to 11 Logic 11 sets N to 12
TXR	R divider [18]	Set the R divider ratio selection: Logic 0 sets R to 1 Logic 1 sets R to 2.
TXPOL	CP polarity [19]	One bit CP polarity selection: Logic 0 sets POL to Normal Logic 1 sets POL to Inverted
RSVD	Reserved [20]	Reserved bit
RSVD	Reserved [21]	Reserved bit
RSVD	Reserved [22]	Reserved bit
RSVD	Reserved [23]	Reserved bit

Table 11. Serial Interface Description for Fractional-N Sx

Symbol	Function	Description
D0	Address bit [0]	Logic 0 enables three-wire programming for synthesizer
D1	Address bit [1]	Logic 0 enables PLL programming and logic 1 enables fractional-modulo programming
EN	Enable mode [2]	Logic 0 enables synthesizer
EF	Integer mode [3]	Logic 0 sets the integer-N mode and logic 1 sets the fractional-N mode
SP	Phase detector output polarity [4]	Logic 0 sets the phase detector output for negative VCO gain and logic 1 sets it for positive VCO gain
SC	Charge-pump output current [6:5]	Charge pump current selection: (logic 00 sets 100 μA, 01 = 200 μA, 10 = 300 μA, 11 = 400 μA)
LD	Test mode [8:7]	Logic 00 multiplexes N divider output to LD output Logic 01 multiplexes R divider output to LD output Logic 10 multiplexes lock detect output to LD output
N	Main divider [19:9]	Sets 11-bit main divider ratio with minimum division ratio of 64
R	Reference divider [23:20]	Sets 4-bit reference divider ratio with minimum division ratio of 1
FN	Fractional-N modulo [23:2]	Sets fractional-N modulo up to 2^{22} (= 4,194,300) modulo

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RSVD	1	RSVD		TXCP Polarity Select	TXR Divider Ratio Select	TXN Divider Radio Select		TXCP Current Select		VGA1 Fine Gain Select		VGA1 Coarse Gain Select			Aux Gain Select	VGA2 Gain Select			Active LPF1 Gain Select	Mixer Gain Select	LNA Gain Select	1	1

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R DIVIDER				N DIVIDER											LD		SC		SP	EF	EN	0	0
Reserved for Fractional-N Programming																						1	0

Figure 4. Programming Word Summary

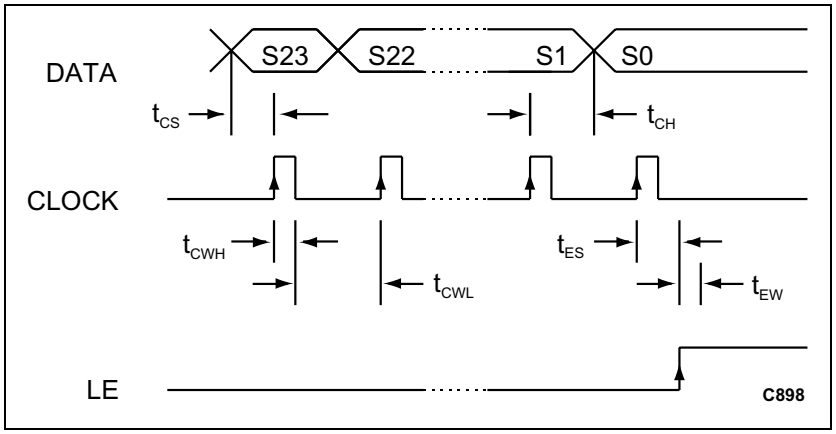

Figure 5. Serial Data Input Timing Diagram For Transceiver

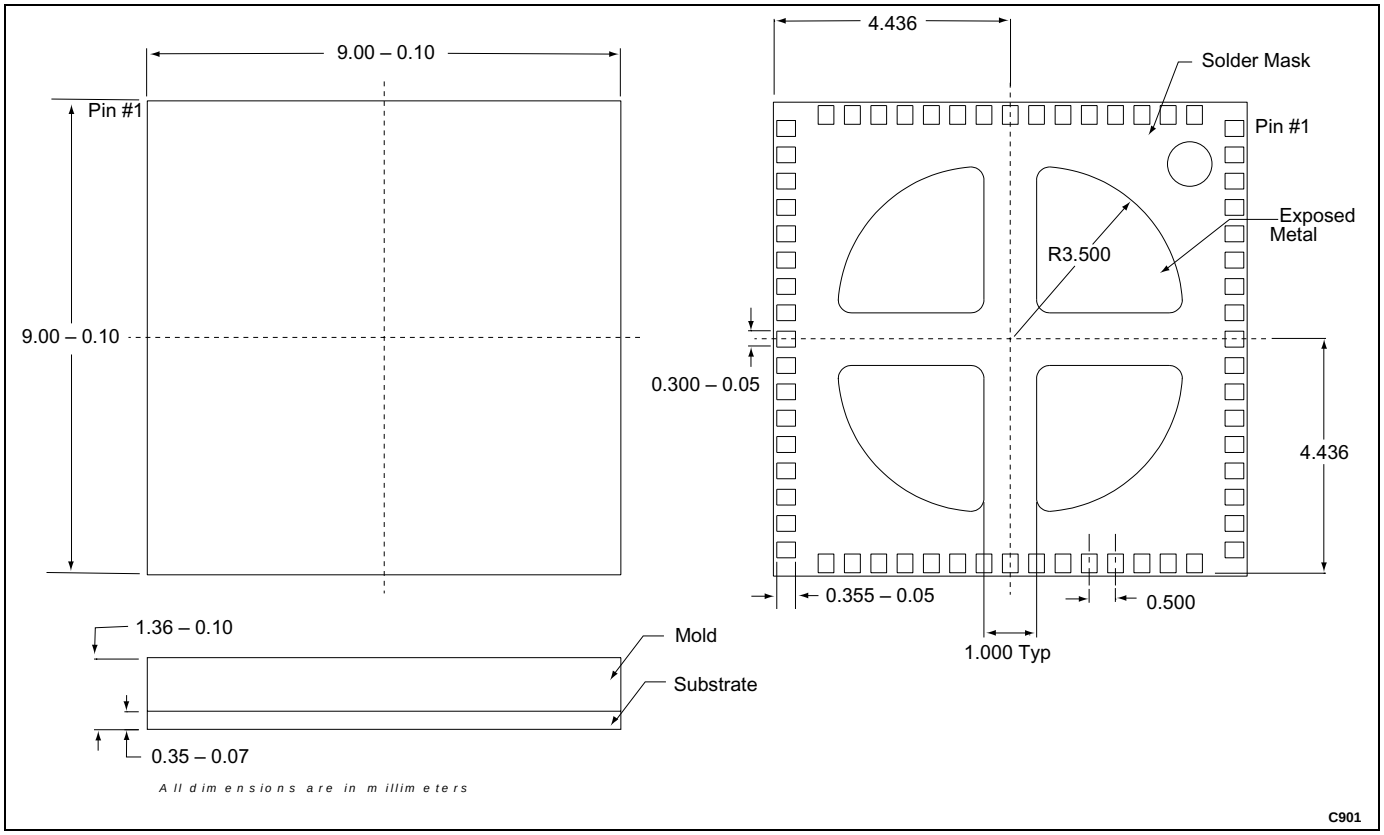

Figure 6. CX74017 64-Pin LGA Package Dimension Drawing

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
CX74017		

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