

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

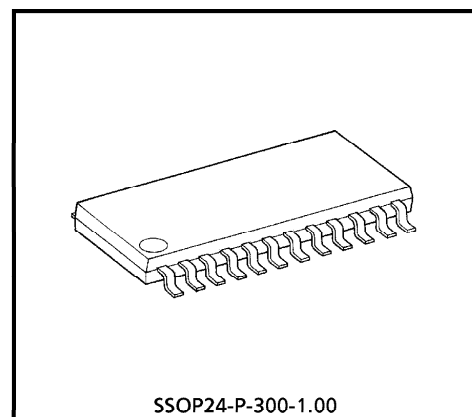
TD62C853F, TD62C854F

8BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER / LATCH DRIVERS

The TD62C853F and TD62C854F are monolithic circuits designed to be used together with Bi-CMOS integrated circuits. The devices consist of a 8 bit shift register, 8 bit latches, and 8 output circuits.

FEATURES

- 8 bit serial-in parallel-out shift register / latch driver (Bi-CMOS process)
- Maximum output sustaining voltage ; 50 V
- Maximum output current ;
 TD62C853F 200 mA / ch (Low saturation type)
 TD62C854F 500 mA / ch (darlington type)

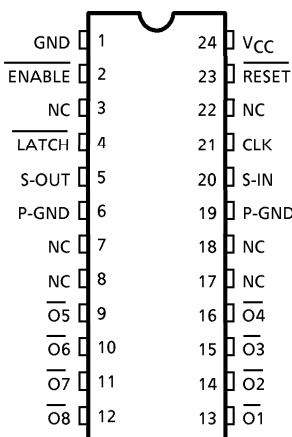


Weight : 0.32 g (Typ.)

- CMOS compatible inputs
- Package ; SSOP24-P-300-1.00

(Note) S-OUT pin is sensitive against Latch-up. (Latch-up performance is under 30mA)

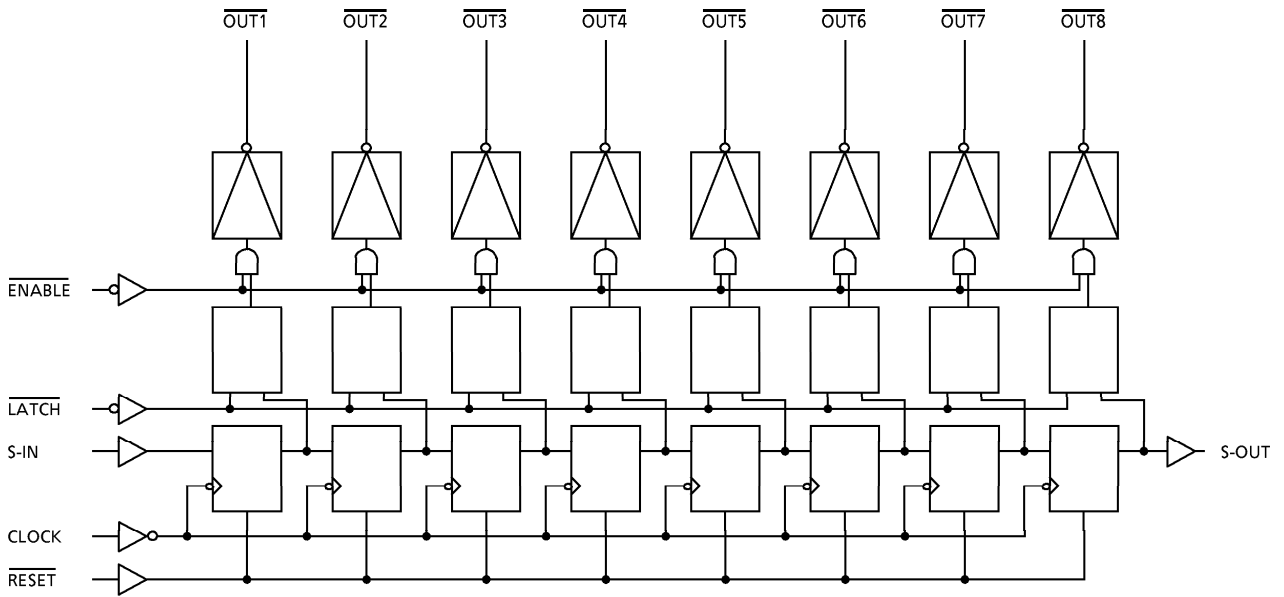
PIN CONNECTION (TOP VIEW)



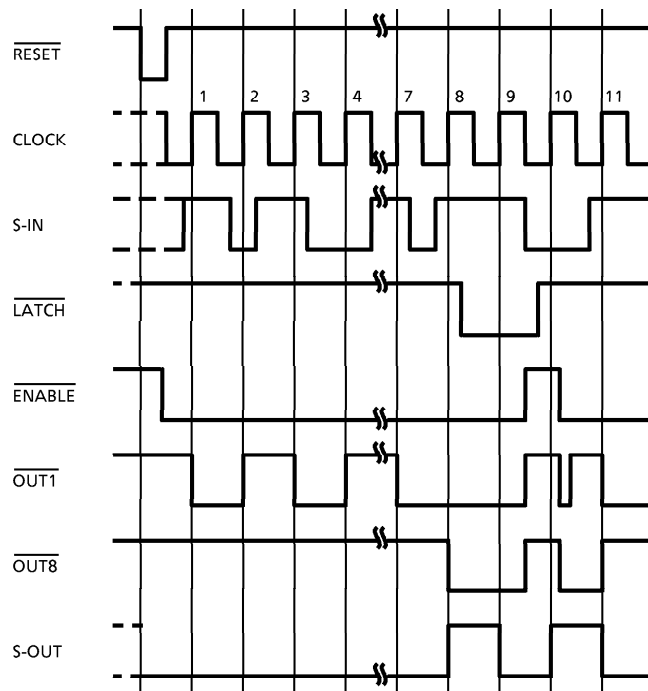
980910EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

BLOCK DIAGRAM

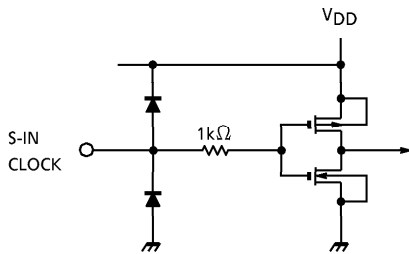


TIMING DIAGRAM

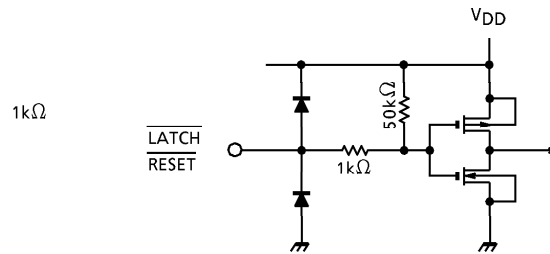


EQUIVALENT CIRCUITS OF INPUTS AND OUTPUTS

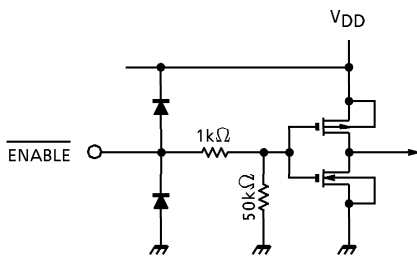
S-IN, CLOCK terminal equivalent circuit



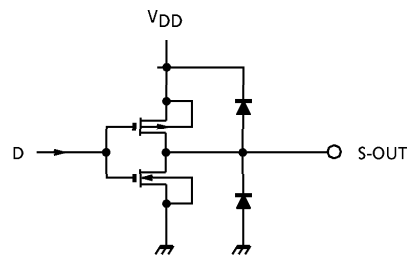
$\overline{\text{LATCH}}$, $\overline{\text{RESET}}$ terminal equivalent circuit



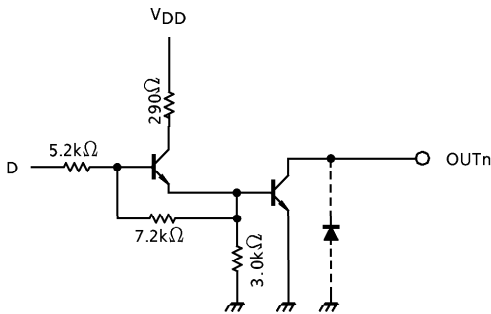
$\overline{\text{ENABLE}}$ terminal equivalent circuit



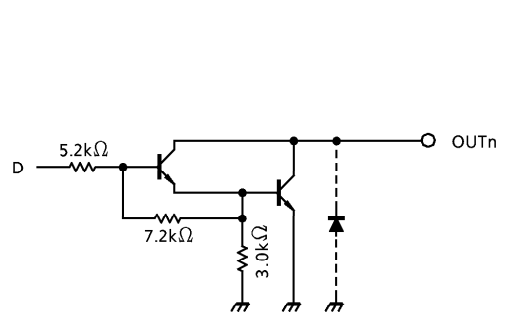
S-OUT terminal equivalent circuit



Output terminal equivalent circuit (TD62C853F)



Output terminal equivalent circuit (TD62C854F)



(Note) The output parasitic diode cannot be used as clamp diode.

TRUTH TABLE

CK	\bar{E}	\bar{R}	$\overline{\text{LATCH}}$	S-IN	OUT		S-OUT
					O1	$\overline{O_n}$	
	L	H	H	L	OFF	$\overline{O_n-1}$	Q7
	L	H	H	H	ON	$\overline{O_n-1}$	Q7
	L	H	L	(*)	NC	NC	Q7
	H	H	(*)	(*)	OFF	NC	Q7
	(*)	(*)	(*)	(*)	NC	NC	Q7
(*)	(*)	L	H	(*)	OFF	OFF	L
(*)	H		L	(*)	NC	NC	L

CK = CLOCK
 \bar{E} = ENABLE
 \bar{R} = RESET
 $\overline{\text{LATCH}}$ = LATCH
 S-IN = SERIAL IN
 OUT = PARALLEL OUT
 S-OUT = SERIAL OUT

(*) = DON'T CARE
 NC = NO CHANGE
 L = LOW LEVEL
 H = HIGH LEVEL

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	- 0.3~7.0	V
Output Sustaining Voltage	V _{CE (SUS)}	- 0.5~50	V
Output Current	TD62C853F	200	mA / ch
	TD62C854F	500	
Input Voltage	V _{IN}	~0.4~V _{DD} + 0.3	V
Power Dissipation	P _D	780 (*)	mW
Operating Temperature	T _{opr}	- 40~85	°C
Storage Temperature	T _{stg}	- 55~150	°C

(*) On PCB (50×50×1.6 mm Cu 30% Glass Epoxy PCB)
 Ambient temperature delated above 25°C in the proportion of 6.6 mW/°C

RECOMMENDED OPERATING CONDITIONS (Ta = -40~85°C)

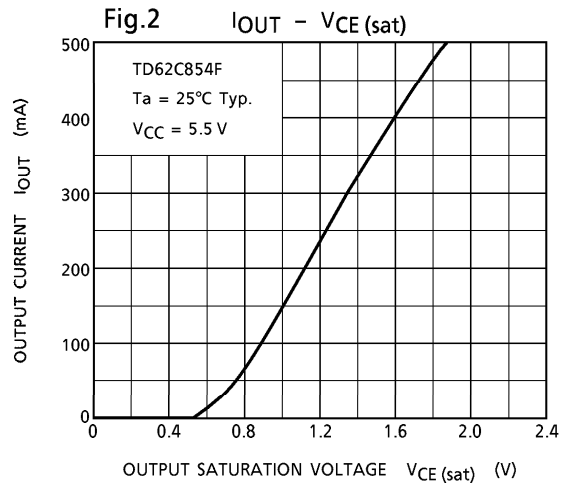
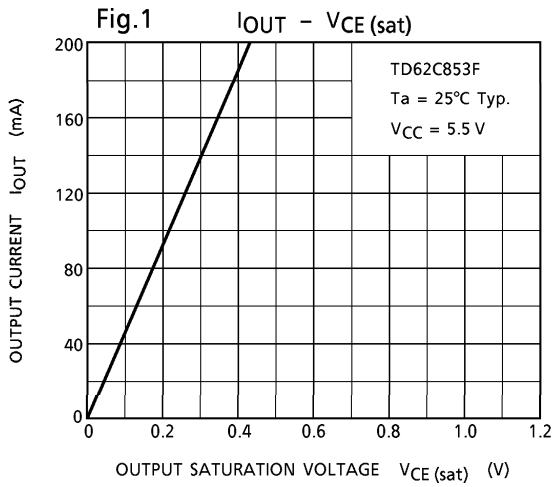
CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage		V _{DD}	—	4.5	5.0	5.5	V
Input Voltage		V _{IN}	—	0	—	V _{DD}	V
Output Current ("H" Level)	S-OUT	I _{OH}	Ta = 25°C	—	—	-0.4	mA
Output Voltage ("H" Level)	$\overline{O_n}$	V _{OH}	—	0	—	50	V
Output Current ("L" Level)	S-OUT	I _{OL}	—	—	—	0.4	mA / ch
	TD62C853F		DC 1 circuit, Ta = 25°C	0	—	160	
			8 circuits on T _{pw} = 25 ms Ta = 85°C V _{DD} = 5.5 V	Duty = 10%	0	—	
	Duty = 40%			0	—	55	
	TD62C854F		DC 1 circuit, Ta = 25°C	0	—	360	
			8 circuits on T _{pw} = 25 ms Ta = 85°C V _{DD} = 5.5 V	Duty = 10%	0	—	
Duty = 50%	0	—		170			
Clock Frequency		f _{CLOCK}	—	1.5	—	—	MHz
Clock Pulse Width		f _w CLOCK	—	0.33	—	—	μs
Data Set Up Time		t _{setup}	—	100	—	—	ns
Data Hold Time		t _{hold}	—	100	—	—	ns

ELECTRICAL CHARACTERISTICS (Ta = -40~85°C)

CHARACTERISTIC		SYM-BOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT			
Input Voltage	"H" Level	V _{IH}	—	—	0.7 V _{DD}	—	—	V			
	"L" Level	V _{IL}	—	—	—	—	0.3 V _{DD}				
Input Current	"H" Level	I _{IH}	—	ENABLE, V _{DD} = 5.5 V V _{IH} = V _{DD}	28	55	110	μA			
	"L" Level	I _{IL}	—	LATCH, RESET V _{DD} = 5.5 V, V _{IL} = GND	-55	-110	-275				
		I _{IN}	—	CLOCK, S-IN V _{IN} = V _{CC} or GND	—	—	±1.0				
Output Voltage	"H" Level	S-OUT	V _{OH}	—	V _{DD} = 4.5 V I _{OH} = -10 μA	3.9	4.1	—	V		
	"L" Level	S-OUT On	V _{OL}	—	V _{DD} = 4.5 V	I _{OL} = 0.8 mA	—	0.2	0.4	V	
						I _{OL} = 100 mA	—	0.29	0.50		
						I _{OL} = 160 mA	—	0.39	0.65		
						I _{OL} = 250 mA	—	1.24	1.90		
					I _{OL} = 400 mA	—	1.54	2.30			
Output Current	"H" Level	On	I _{OH}	—	V _{DD} = 5.5 V, V _{OH} = 50.0 V	—	—	100	μA		
Operating Supply Current			I _{DD1}	—	V _{DD} = 5.5 V Ta = 25°C	ENABLE = "H"	—	130	200	mA	
			I _{DD2}			f _{CLK} = 1 MHz Output open DATA = 1 / 2 f _{CLK}	—	2.0	5.0		
			TD62C853F TD62C854F			I _{DD3}	1 circuit on f _{CLK} = 1 MHz	—	35		40
							ENABLE = "L"	—	1.0		1.4

SWITCHING CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC			SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time	Low-to-High	CK-S-OUT	t_{pLH}	—	$V_{DD} = 5.0\text{ V}, V_{IH} = 5.0\text{ V}$ $V_{IL} = 0\text{ V}, \text{Duty} = 50\%$ $R_L = \begin{cases} 300\ \Omega \text{ (TD62C853F)} \\ 120\ \Omega \text{ (TD62C854F)} \end{cases}$	—	0.40	0.65	μs
		$\overline{\text{CK}}\text{-}\overline{\text{On}}$				—	1.80	3.00	
		$\overline{\text{L}}\text{-}\overline{\text{On}}$				—	2.10	3.50	
		$\overline{\text{R}}\text{-}\overline{\text{On}}$				—	1.50	2.50	
		$\overline{\text{E}}\text{-}\overline{\text{On}}$				—	1.50	2.50	
	High-to-Low	CK-S-OUT	t_{pHL}	—		—	0.33	0.55	
		$\overline{\text{CK}}\text{-}\overline{\text{On}}$				—	0.41	0.70	
		$\overline{\text{L}}\text{-}\overline{\text{On}}$				—	0.30	0.50	
		R-S-OUT				—	0.25	0.42	
		$\overline{\text{E}}\text{-}\overline{\text{On}}$				—	0.21	0.35	
Maximum Clock Frequency			f_{MAX}	—	1.5	2.0	—	MHz	
Minimum Pulse Width	CLOCK	t_{wCK}	—	—	250	330	ns		
	$\overline{\text{LATCH}}$	t_{wL}		—	116	160			
	$\overline{\text{RESET}}$	t_{wR}		—	107	140			
Data Set Up Time			t_{setup}	—	—	30	60	ns	
Data Hold Time			t_{hold}	—	—	14	40	ns	
Maximum Clock Rise Time			t_r	—	—	70	—	ns	
Maximum Clock Fall Time			t_f	—	—	70	—		



TD62C853F each characteristic data and reference graph

Output current I_{OUT} vs lighting rate DUTY,
 Condition: 1~8 circuit operation, $V_{DD} = 5.5\text{ V}$

Fig.3 DUTY - I_{OUT} ($T_{opr} = 85^\circ\text{C}$)

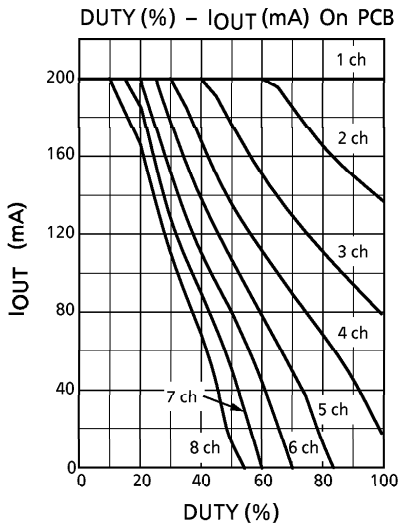


Fig.4 DUTY - I_{OUT} ($T_{opr} = 55^\circ\text{C}$)

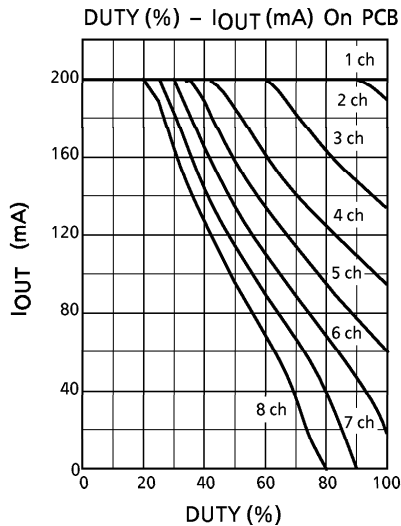
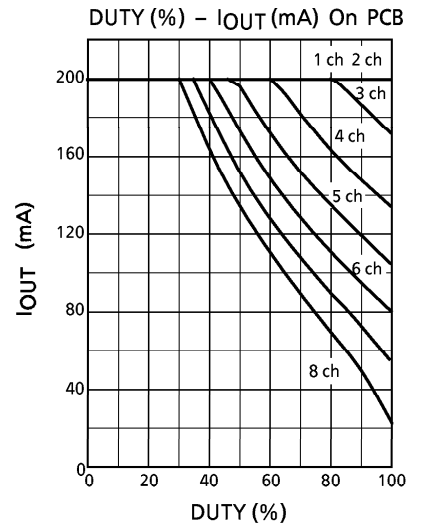


Fig.5 DUTY - I_{OUT} ($T_{opr} = 25^\circ\text{C}$)



TD62C854F each characteristic data and reference graph

Output current I_{OUT} vs lighting rate DUTY,
 Condition: 1~8 circuit operation, $V_{DD} = 5.5V$

Fig.6 DUTY - I_{OUT} (Topr = 85°C)

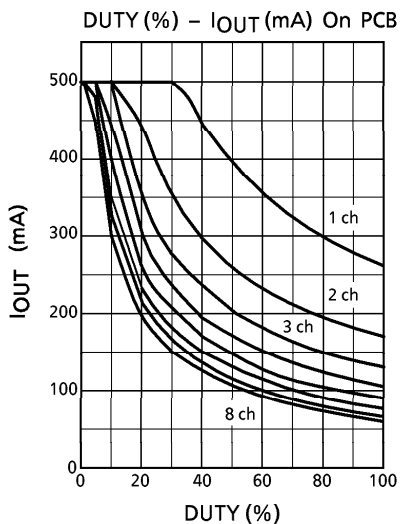


Fig.7 DUTY - I_{OUT} (Topr = 55°C)

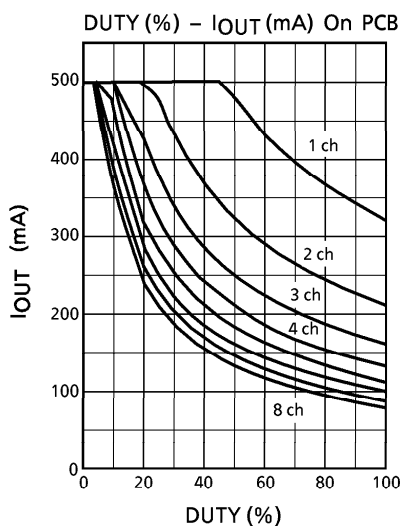
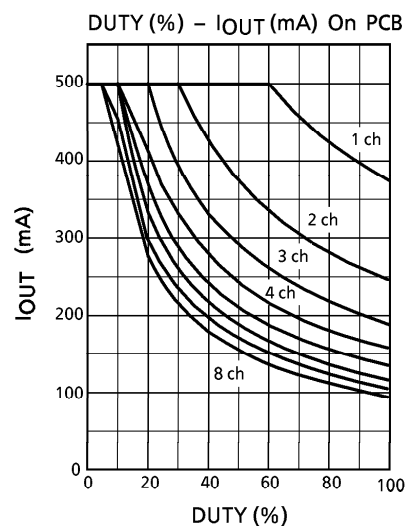
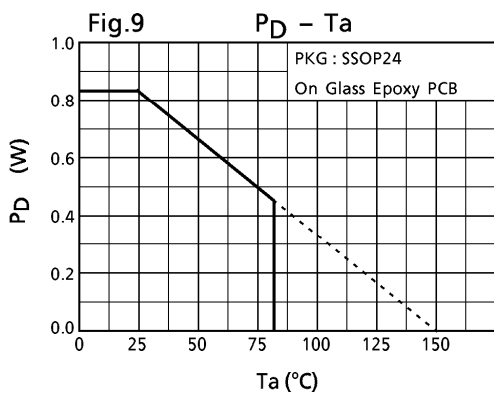


Fig.8 DUTY - I_{OUT} (Topr = 25°C)

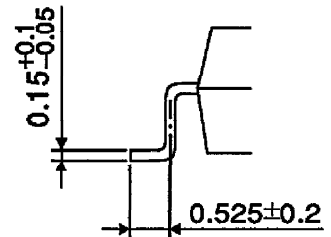
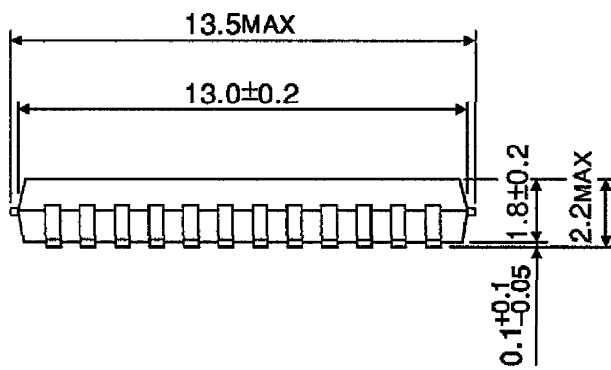
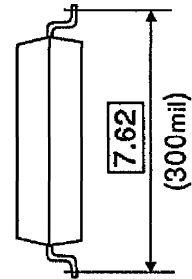
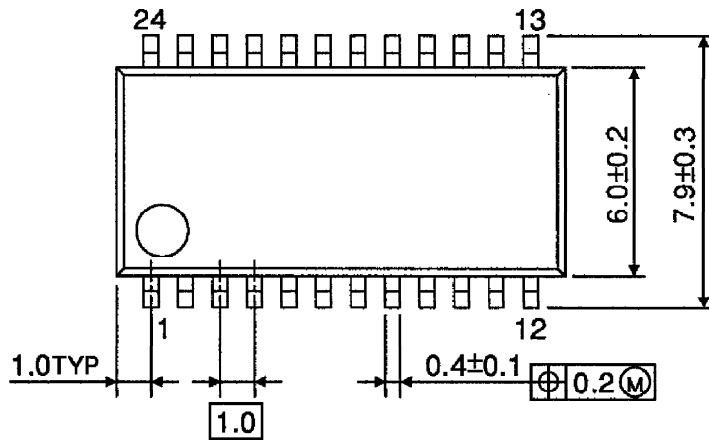


SSOP24 Power dissipation



PACKAGE DIMENSIONS
SSOP24-P-300-1.00

Unit: mm



Weight: 0.32 g (Typ.)