OKI semiconductor

MSM5298

DOT MATRIX LCD 68 DOT COMMON DRIVER

GENERAL DESCRIPTION

The OKI MSM5298GS is a dot matrix LCD's common driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 68-bit bidirectional shift register, 68-bit level shifter and 68-bit 4-level driver.

This LSI has 68 output pins to be connected to the LCD. By connecting more than two MSM5298GSs in series, this LSI is applicable to a wide LCD panel.

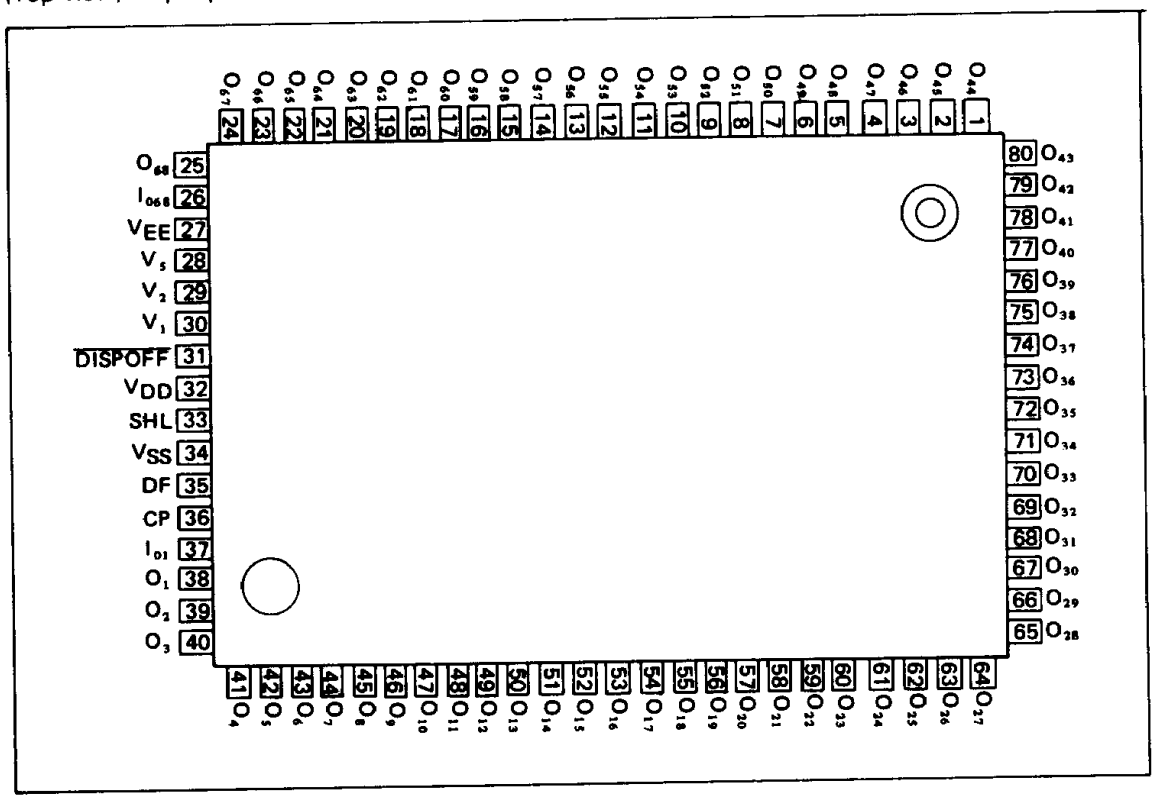
This LSI can drive a variety of LCD because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

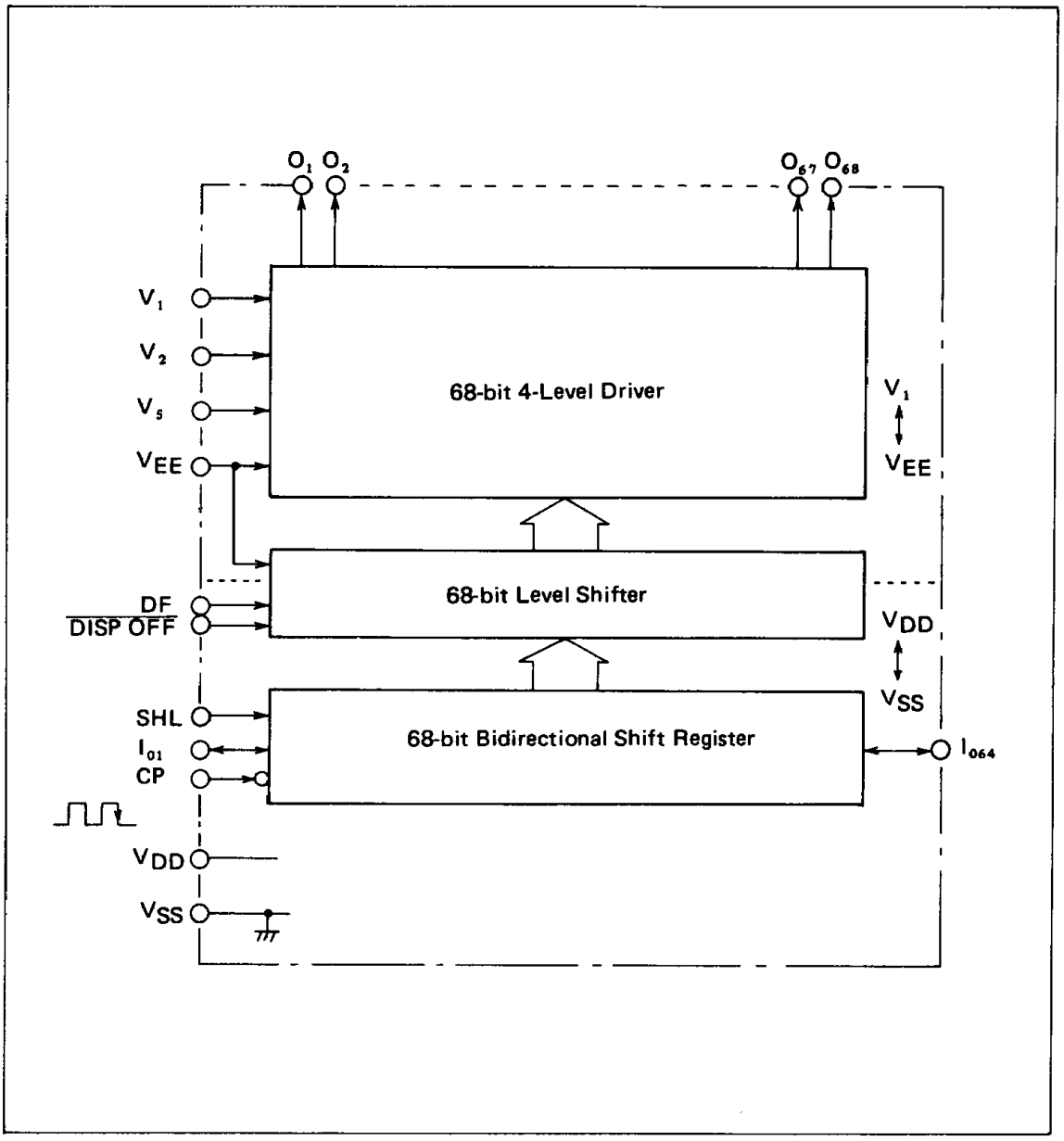
- Supply voltage: 4.5V ~ 5.5V
- LCD driving voltage: 8 ~ 26 V
- Applicable LCD duty: 1/64 ~ 1/256
  Three chips of the MSM5298GS are required to drive 1/200 duty LCD.
- Bias voltage can be supplied externally.
- 80 pin plastic QFP (QFP80-P-1420-K)
- 80 pin -VI plastic QFP (QFP80-P-1420-VIK)

PIN CONFIGURATION (TOP VIEW)

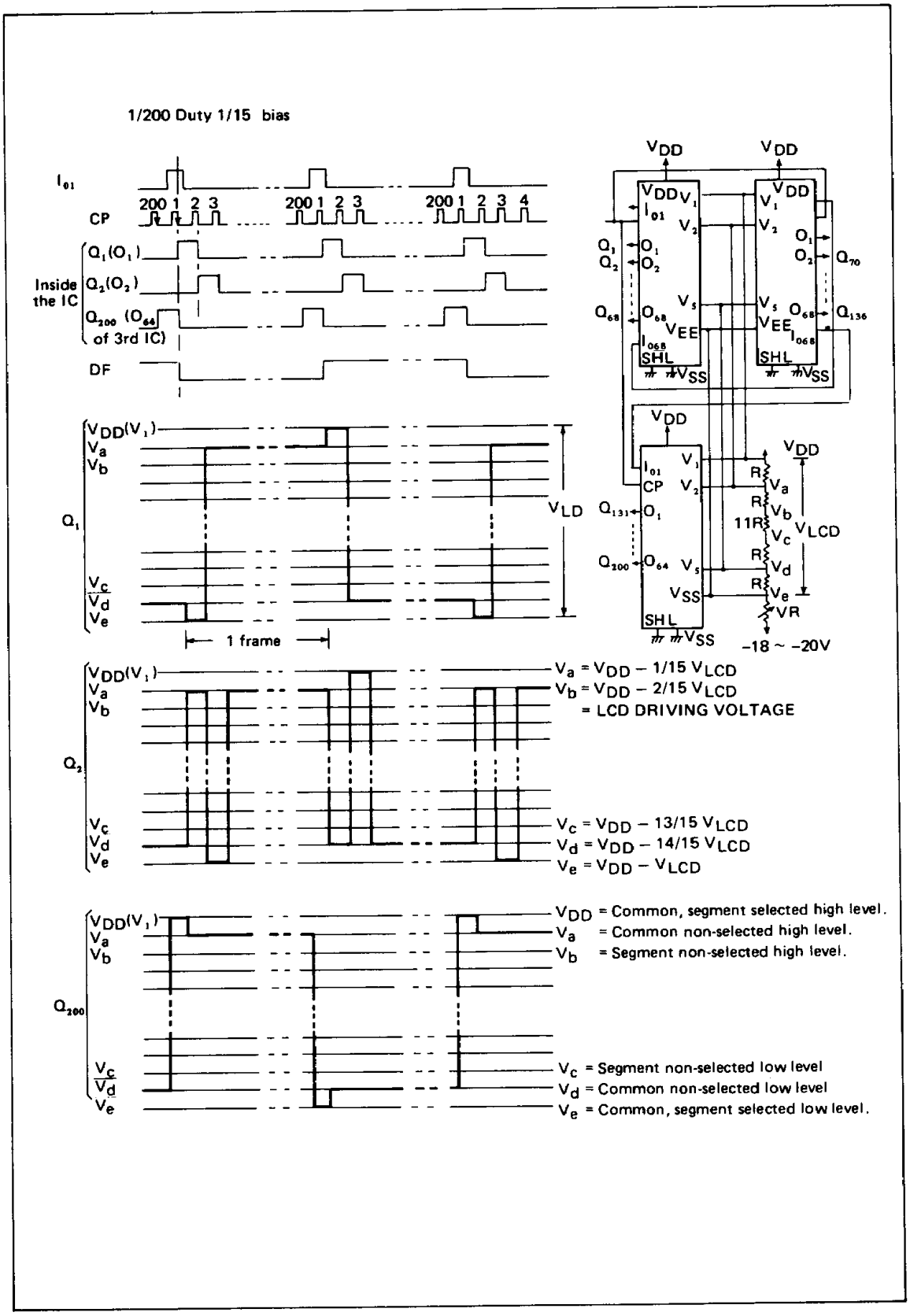
(Top view) 80 pin plastic QFP



BLOCK DIAGRAM



TIMING CHART

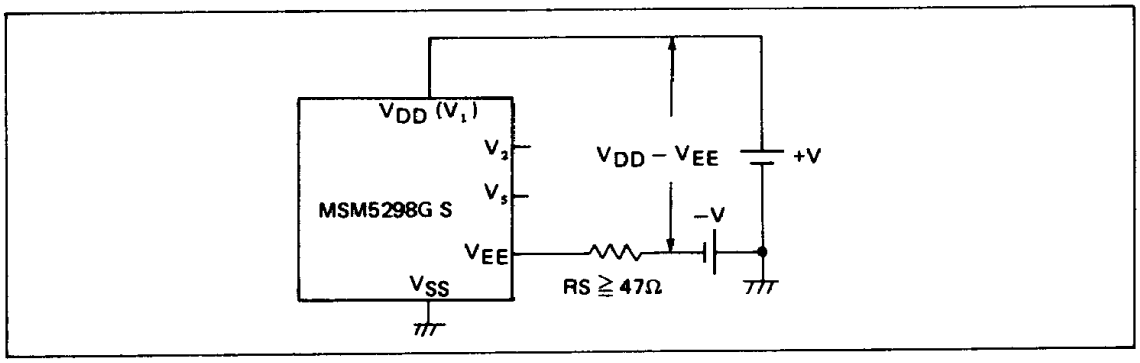


ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	Ta = 25°C	−0.3 ~ 6	V
Supply voltage (2)	$V_{DD}-V_{EE}$ *1	Ta = 25°C	0 ~ 27	V
	$V_{DD}-V_{EE}$ *1 *2	Ta = 25°C	0 ~ 30	V
Input voltage	V_1	Ta = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$

*2 In case of connecting Resister (RS ≧ 47 Ω) at V_{EE} pin

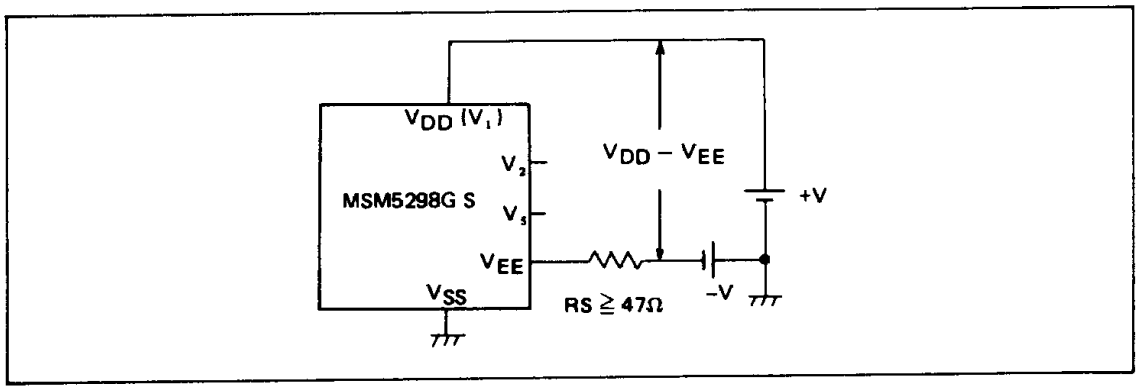


OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	—	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD}-V_{EE}$ *1	—	8 ~ 26	V
	$V_{DD}-V_{EE}$ *1 *2	—	8 ~ 28	V
Operating temperature	T_{OP}	—	−20 ~ +85	°C

*1 $V_1 > V_2 > V_5$, V_{EE}, $V_1 \leqq V_{DD}$

*2 In case of connecting Resister (RS ≧ 47 Ω) at V_{EE} pin



DC CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = −20 ~ +85°C CL = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH} *1	–	0.8V_{DD}	–	–	V
"L" Input voltage	V_{IL} *1	–	–	–	0.2V_{DD}	V
"H" Input current	I_{IH} *1	V_{IH}=V_{DD} V_{DD} =5.5V	–	–	1	μA
"L" Input current	I_{IL} *1	V_{IH} =0V V_{DD} =5.5V	–	–	−1	μA
"H" output voltage	V_{OH} *2	I_O =−0.4 mA V_{DD} =4.5V	V_{DD} −0.4	–	–	V
"L" output voltage	V_{OL} *2	I_O=0.4mA V_{DD} =4.5V	–	–	0.4	V
ON Resistance	R_{ON}	$V_{DD}-V_{EE}$ =23V, V_{DD}=4.5V $\lvert V_N-V_O\rvert$=0.25V *3	–	0.75	1.5	kΩ
Power consumption	I_{DD}	CP = 14KHz V_{DD} =5.5V $V_{DD}-V_{EE}$ =23V No load	–	–	100	μA
Input capacitance	C_I	f = 1MHz	–	5	–	pF

*1 Applicable to CP, I_{01}, I_{068}, SHL, DF, $\overline{\text{DISP OFF}}$ terminals.

*2 Applicable to I_{01}, and I_{068} terminals.

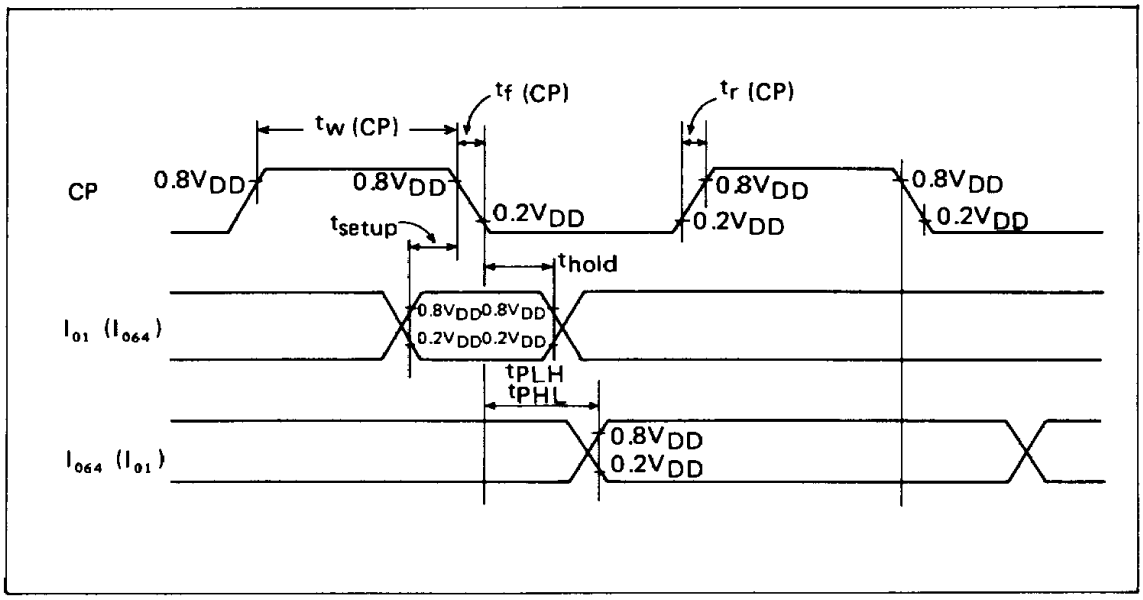
*3 $VN = V_{DD} \sim V_{EE}$, $V_2 = \frac{1}{15}(V_{DD} - V_{EE})$, $V_5 = \frac{14}{15}(V_{DD} - V_{EE})$, $V_{DD} = V_1$

*4 Applicable to $O_1 \sim O_{68}$ terminals.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = -20 ~ +85°C CL = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH} t_{PHL}	–	–	–	250	ns
Max. clock frequency	f CP	–	1	–	–	MHz
Clock pulse width	t_W (CP)	–	125	–	–	ns
DATA SET UP TIME I_{01} (I_{064}) → CP	$t_{set\ up}$	–	100	–	–	ns
DATA HOLD TIME I_{01} ($_{064}$) → CP	t_{hold}	–	100	–	–	ns
Clock pulse Rising/ Falling time	t_r (CP) t_f (CP)	–	–	–	50	ns



TRUTH TABLE

DF	Latched data level	$\overline{DISPOFF}$	Display data output level (O_1 ~ O_{68})
L	L	H	V_2
L	H	H	V_{EE}
H	L	H	V_5
H	H	H	V_1
X	X	L	V_1

PIN DISCRIPTION

• I_{01}, I_{68}, SHL

I_{01} and I_{068} are 68-bit bidirectional shift register input/output pins. The shifting direction is selected by the SHL pin. Refer to the table below.

SHL	Shifting direction	I_{01}/I_{068}	Input/ output	Pin description
L	$O_1 \rightarrow O_{68}$	I_{01}	Input	The scanning data from the LCD controller LSI is input from I_{01} synchronized with the clock pulse. *1
		I_{068}	Output	Shift regiser contents output pin. The data which was input from I_{01} in output from IO_{68} with 68 bit's delay, synchronized with the clock pulse. Refer to the application circuit.
H	$O_{68} \rightarrow O_1$	I_{068}	Input	The scanning data from the LCD controller LSI is input from I_{068} synchronized with the clock pulse. *1.
		I_{01}	Output	Shift register contents output pin. The data which was input from I_{068} in output from I_{01} with 68 bit's delay, synchronized with the clock pulse. Refer to the application circuit.

*1. The combination of the scanning data, I_{01} or I_{068}, and the LCD driving output, $O_1 \sim O_{68}$, in shown in the table below.

I_{01}, I_{068}	LCD driving output
"H"	Selected level (V_1, V_{EE})
"L"	Non-selected level (V_2, V_5)

• CP

Clock pulse input pin for 68-bit bidirectional shift register. The data is shifted to 68-bit level shifter at the falling edge of clock pulse.

• DF

Alternate signal input pin for LCD driving. Normal frame inversion signal is input.

• V_{DD}, V_{SS}

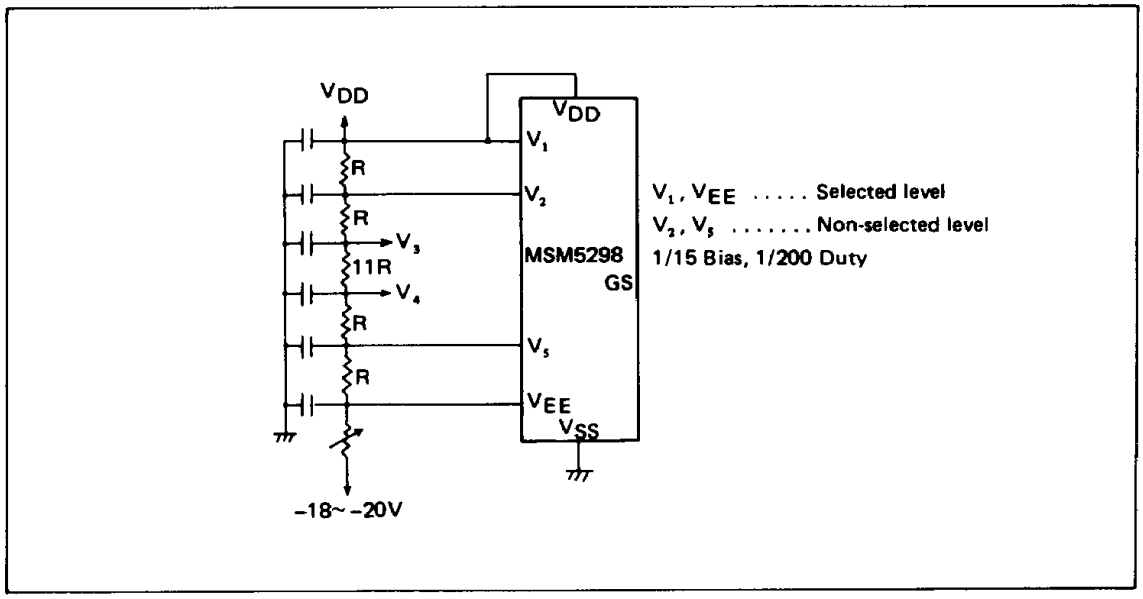
Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V. V_{SS} in a ground pin. (V_{SS} = 0V).

• $\overline{\text{DISP OFF}}$

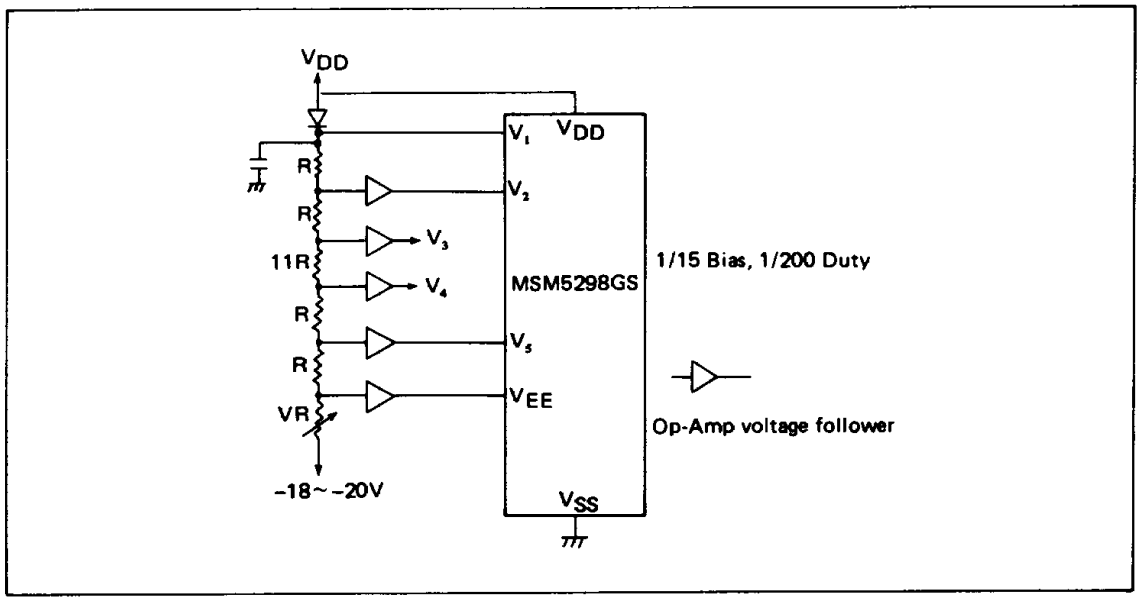
Control input pin for display data output level ($O_1 \sim O_{68}$). V_1 level is output from $O_1 \sim O_{68}$ pin during "L" level input. Refer to TRUTH TABLE.
LCD becomes non-visual by V_1 level output from every output of segment drivers and every output of common drivers.

• V_1, V_2, V_5, V_{EE}

Bias supply voltage pins to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source.
The below figure shows the case when bias voltage is divided by the resistance.
V_1 is not necessarily connected to V_{DD}.



The below figure shows the case when bias voltage is supplied by the OP-Amps.
By using OP-Amps, the bias voltage becomes low impedance and the power consumption of LCD module becomes low.



• $O_1 \sim O_{68}$

Display data output pins which correspond to 68-bit shift register contents. One of V_1, V_2, V_5 and V_{EE} is selected as a display driving voltage source according to the conbination of the latched data level and DF signal. (Refer to the truth table.)

APPLICATION CIRCUIT