

# MC74VHC1GT126

## Noninverting Buffer / CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74VHC1GT126 is a single gate noninverting 3-state buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC1GT126 requires the 3-state control input ( $\overline{OE}$ ) to be set Low to place the output into the high impedance state.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT126 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT126 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed:  $t_{PD} = 3.5$  ns (Typ) at  $V_{CC} = 5$  V
- Low Power Dissipation:  $I_{CC} = 1$   $\mu$ A (Max) at  $T_A = 25^\circ\text{C}$
- TTL-Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- CMOS-Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC}$  @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 62; Equivalent Gates = 16

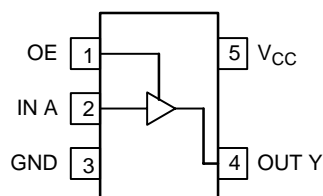


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol



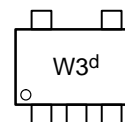
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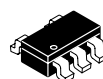
### MARKING DIAGRAMS



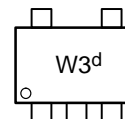
SC-88A / SOT-353/SC-70  
DF SUFFIX  
CASE 419A



Pin 1  
d = Date Code



TSOP-5/SOT-23/SC-59  
DT SUFFIX  
CASE 483



Pin 1  
d = Date Code

### PIN ASSIGNMENT

Pin	Function
1	OE
2	IN A
3	GND
4	OUT Y
5	$V_{CC}$

### FUNCTION TABLE

A Input	OE Input	Y Output
L	H	L
H	H	H
X	L	Z

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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## MAXIMUM RATINGS (Note 1)

Symbol	Characteristics	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>OUT</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current V <sub>OUT</sub> < GND; V <sub>OUT</sub> > V <sub>CC</sub>	+20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	+25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND	+50	mA
P <sub>D</sub>	Power Dissipation in Still Air SC-88A, TSOP-5	200	mW
θ <sub>JA</sub>	Thermal Resistance SC-88A, TSOP-5	333	°C/W
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 s	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I <sub>Latch-Up</sub>	Latch-Up Performance Above V <sub>CC</sub> and Below GND at 125°C (Note 5)	±500	mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	3.0	5.5	V
V <sub>IN</sub>	DC Input Voltage	0.0	5.5	V
V <sub>OUT</sub>	DC Output Voltage	0.0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time V <sub>CC</sub> = 5.0 V ± 0.5 V	0	20	ns/V

## Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

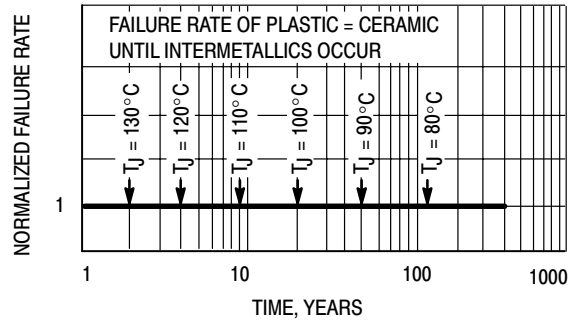


Figure 3. Failure Rate vs. Time Junction Temperature

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		-55 ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		3.0	1.4			1.4		1.4		V
			4.5	2.0		2.0		2.0			
			5.5	2.0		2.0		2.0			
V <sub>IL</sub>	Maximum Low-Level Input Voltage		3.0			0.53		0.53		0.53	V
			4.5			0.8		0.8		0.8	
			5.5			0.8		0.8		0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 4 mA I <sub>OH</sub> = - 8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1.0		20		40	μA
I <sub>CCT</sub>	Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V Other Input: V <sub>CC</sub> or GND	5.5			1.35		1.50		1.65	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5			± 0.25		± 2.5		± 2.5	μA

## AC ELECTRICAL CHARACTERISTICS Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		-55 ≤ T <sub>A</sub> ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to Y (Figures 3 and 5)	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0		12.0 16.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5		8.5 10.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Output Enable Time, OE to Y (Figures 4 and 5)	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15pF R <sub>L</sub> = R <sub>I</sub> = 500 Ω C <sub>L</sub> = 50pF		5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0		11.5 15.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15pF R <sub>L</sub> = R <sub>I</sub> = 500 Ω C <sub>L</sub> = 50pF		3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0		7.5 9.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Output Disable Time, OE to Y (Figures 4 and 5)	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15pF R <sub>L</sub> = R <sub>I</sub> = 500 Ω C <sub>L</sub> = 50pF		6.5 8.0	9.7 13.2	1.0 1.0	11.5 15.0		14.5 18.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15pF R <sub>L</sub> = R <sub>I</sub> = 500 Ω C <sub>L</sub> = 50pF		4.8 7.0	6.8 8.8	1.0 1.0	8.0 10.0		10.0 12.0	
C <sub>in</sub>	Maximum Input Capacitance			4	10		10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High Impedance State)			6						pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	<b>Typical @ 25°C, V<sub>CC</sub> = 5.0 V</b>								pF
		14								

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per buffer). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

# MC74VHC1GT126

## SWITCHING WAVEFORMS

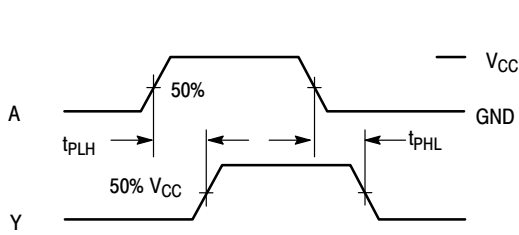


Figure 4. Switching Waveforms

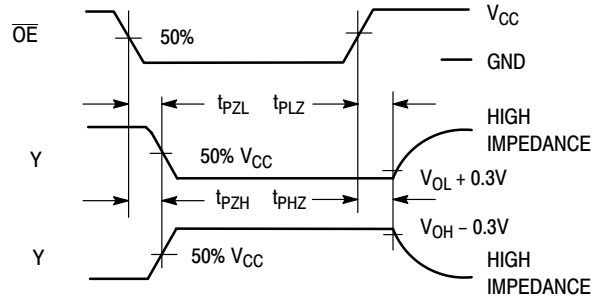
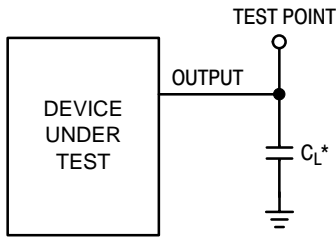
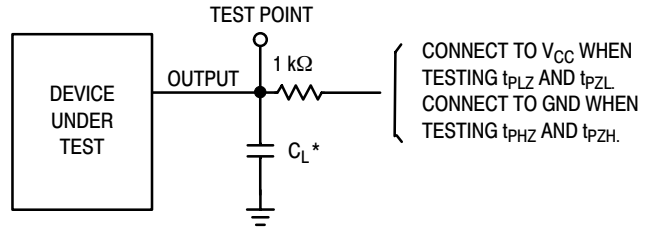


Figure 5.



\*Includes all probe and jig capacitance

Figure 6. Test Circuit



\*Includes all probe and jig capacitance

Figure 7. Test Circuit

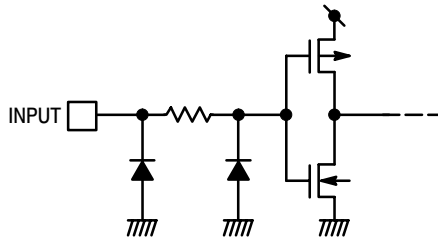


Figure 8. Input Equivalent Circuit

## DEVICE ORDERING INFORMATION

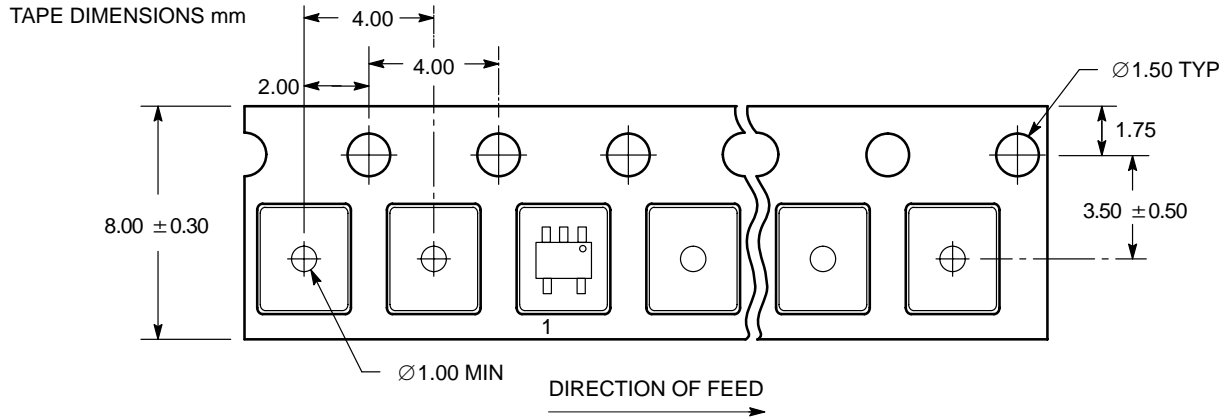
Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size†
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT126DF1	MC	74	VHC1G	T126	DF	1	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT126DF2	MC	74	VHC1G	T126	DF	2	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT126DT1	MC	74	VHC1G	T126	DT	1	TSOP5 / SOT-23 / SC-59	178 mm (7") 3000 Unit

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

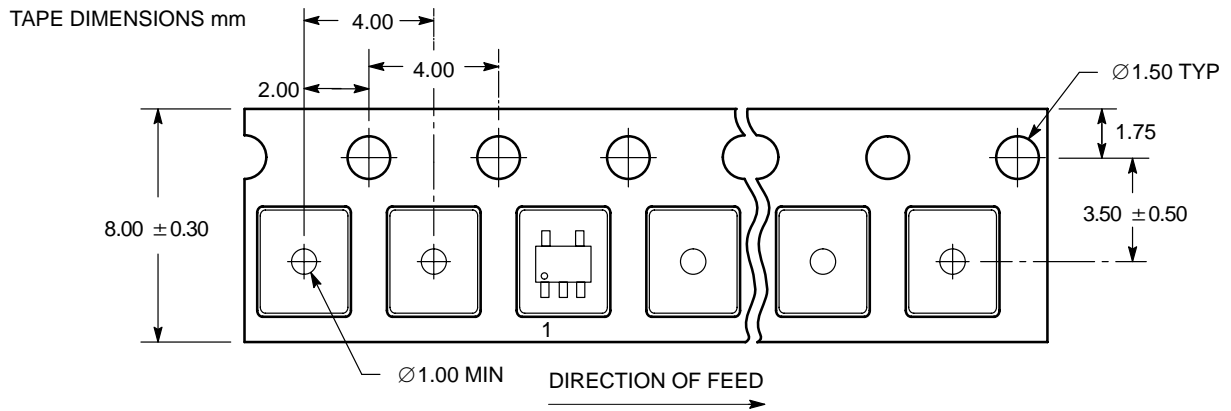
# MC74VHC1GT126



**Figure 9. Tape Ends for Finished Goods**



**Figure 10. SC-70-5/SC-88A/SOT-353 DF1 Reel Configuration/Orientation**



**Figure 11. SC-70/SC-88A/SOT-353 DF2 and SOT23-5/TSOP-5/SC59-5 DT1 Reel Configuration/Orientation**

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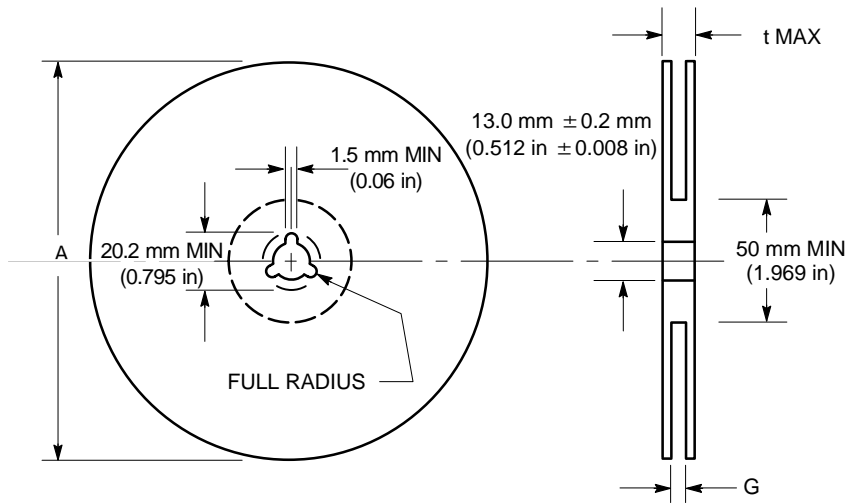


Figure 12. Reel Dimensions

## REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	1, 2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

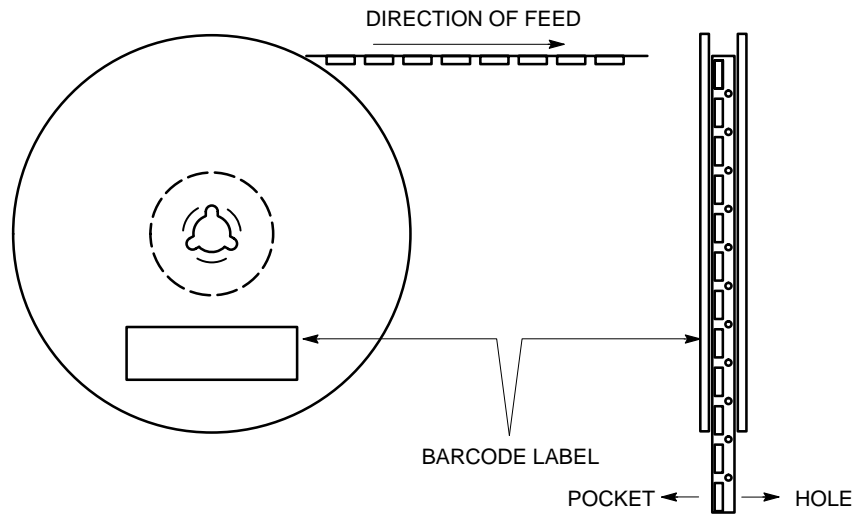
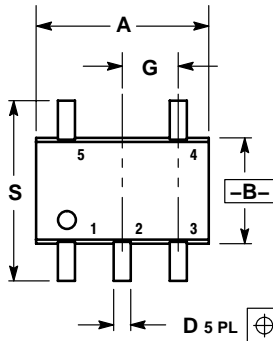


Figure 13. Reel Winding Direction

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## PACKAGE DIMENSIONS

**SC70-5/SC-88A/SOT-353**  
**DF SUFFIX**  
**5-LEAD PACKAGE**  
**CASE 419A-02**  
**ISSUE G**

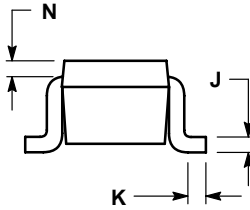


$\text{D } 5 \text{ PL } \text{ } \oplus \text{ } 0.2 \text{ (0.008) } \text{ } \text{M} \text{ } \text{B } \text{ } \text{M}$

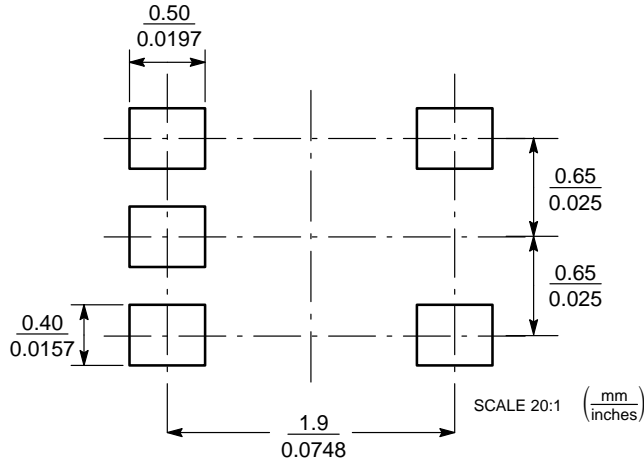
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



### SOLDERING FOOTPRINT\*



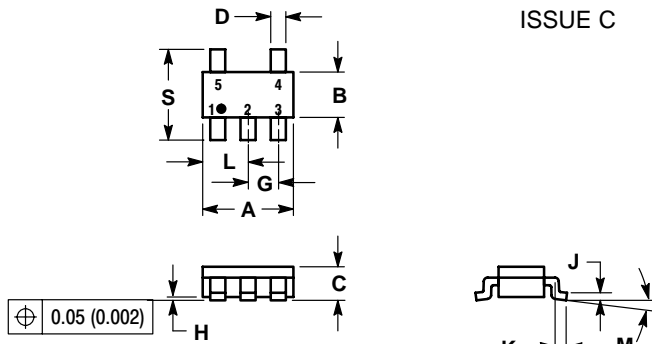
**Figure 14. SC-88A/SC70-5/SOT-353**

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

SOT23-5/TSOP-5/SC59-5  
DT SUFFIX  
5-LEAD PACKAGE  
CASE 483-01  
ISSUE C



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

### SOLDERING FOOTPRINT\*

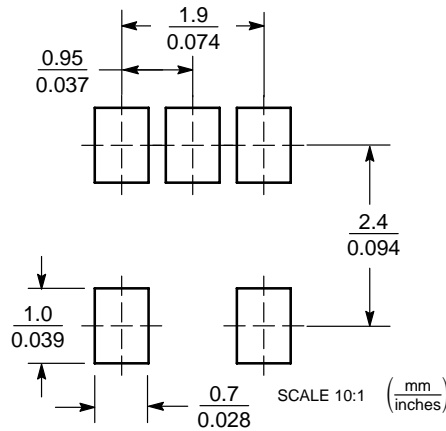



Figure 15. THIN SOT23-5/TSOP-5/SC59-5

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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