

4M × 4-Bit Dynamic RAM 2k & 4k Refresh (Fast Page Mode)

HYB 5116400BJ-50/-60
HYB 5117400BJ-50/-60
HYB 3116400BJ/BT-50/-60
HYB 3117400BJ-50/-60

Advanced Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast Page Mode operation
- Performance:

| | | -50 | -60 | |
|-----------|------------------------------|-----|-----|----|
| t_{RAC} | \overline{RAS} access time | 50 | 60 | ns |
| t_{CAC} | \overline{CAS} access time | 13 | 15 | ns |
| t_{AA} | Access time from address | 25 | 30 | ns |
| t_{RC} | Read/Write cycle time | 84 | 104 | ns |
| t_{PC} | Fast page mode cycle time | 35 | 40 | ns |

- Power Dissipation, Refresh & Addressing:

| | HYB 5116400 | | HYB 3116400 | | HYB 5117400 | | HYB 3117400 | | |
|--------------|---------------------|-----|---------------|-----|---------------------|-----|---------------|-----|----|
| | -50 | -60 | -50 | -60 | -50 | -60 | -50 | -60 | |
| Power Supply | 5 V ± 10% | | 3.3 V ± 0.3 V | | 5 V ± 10% | | 3.3 V ± 0.3 V | | |
| Addressing | 12/10 | | 12/10 | | 11/11 | | 11/11 | | |
| Refresh | 4096 cycles / 64 ms | | | | 2048 cycles / 32 ms | | | | |
| Active | 275 | 220 | 180 | 144 | 440 | 385 | 288 | 252 | mW |
| TTL Standby | 11 | | 7.2 | | 11 | | 7.2 | | mW |
| CMOS Standby | 5.5 | | 3.6 | | 5.5 | | 3.6 | | mW |

- Read, write, read-modify-write, \overline{CAS} -before- \overline{RAS} refresh, \overline{RAS} -only refresh, hidden refresh and test mode
- All inputs, outputs and clocks fully TTL (5 V versions) and LV-TTL (3.3 V version)-compatible
- Plastic Package: P-SOJ-26/24-1 300 mil
P-TSOPII-26/24-1 300 mil

The HYB 5(3)116(7)400 are 16 MBit dynamic RAMs based on die revisions "G" & "F" and organized as 4 194 304 words by 4-bits. The HYB 5(3)116(7)400BJ/BT utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5(3)116(7)400 to be packaged in a standard SOJ-26/24 and TSOPII-26/24 plastic package with 300 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment.

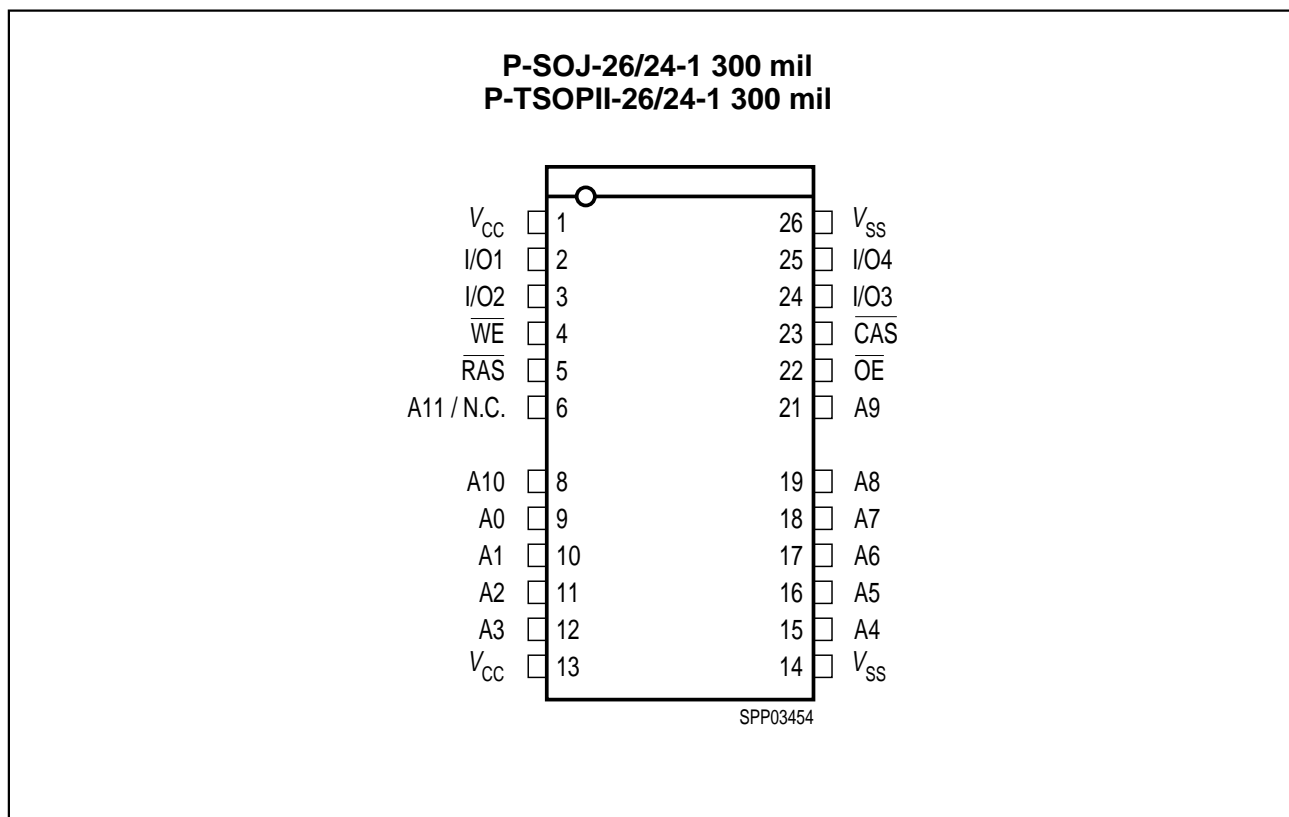
Ordering Information

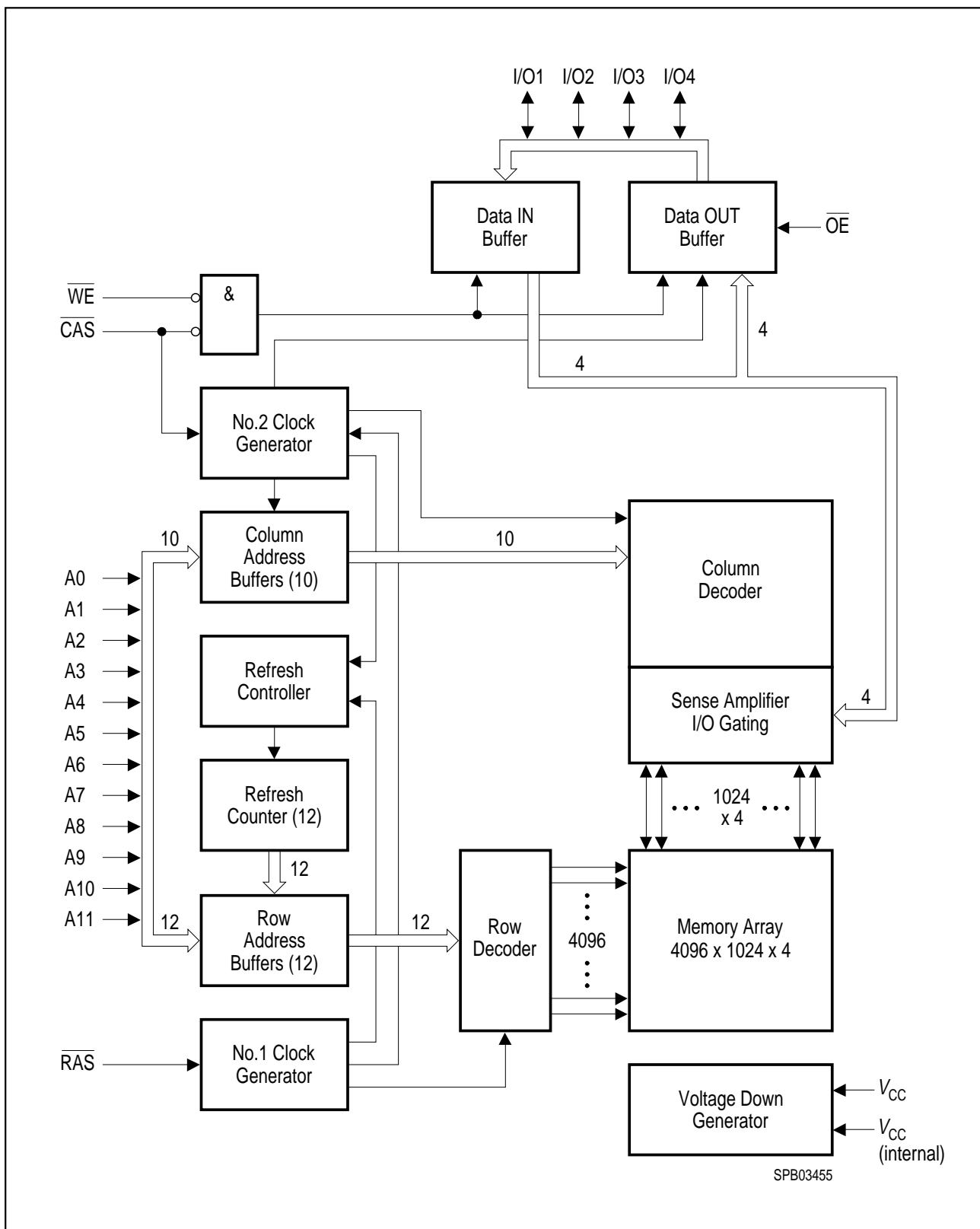
| Type | Ordering Code | Package | Descriptions |
|----------------------------|---------------|--------------------------|----------------------|
| 2k-Refresh Versions | | | |
| HYB 5117400BJ-50 | Q67100-Q1086 | P-SOJ-26/24-1 300 mil | 5 V 50 ns FPM-DRAM |
| HYB 5117400BJ-60 | Q67100-Q1087 | P-SOJ-26/24-1 300 mil | 5 V 60 ns FPM-DRAM |
| HYB 3117400BJ-50 | on request | P-SOJ-26/24-1 300 mil | 3.3 V 50 ns FPM-DRAM |
| HYB 3117400BJ-60 | on request | P-SOJ-26/24-1 300 mil | 3.3 V 60 ns FPM-DRAM |
| 4k-Refresh Versions | | | |
| HYB 5116400BJ-50 | Q67100-Q1049 | P-SOJ-26/24-1 300 mil | 5 V 50 ns FPM-DRAM |
| HYB 5116400BJ-60 | Q67100-Q1050 | P-SOJ-26/24-1 300 mil | 5 V 60 ns FPM-DRAM |
| HYB 3116400BJ-50 | on request | P-SOJ-26/24-1 300 mil | 3.3 V 50 ns FPM-DRAM |
| HYB 3116400BJ-60 | on request | P-SOJ-26/24-1 300 mil | 3.3 V 60 ns FPM-DRAM |
| HYB 3116400BT-50 | on request | P-TSOPII-26/24-1 300 mil | 3.3 V 50 ns FPM-DRAM |
| HYB 3116400BT-60 | on request | P-TSOPII-26/24-1 300 mil | 3.3 V 60 ns FPM-DRAM |

Pin Names

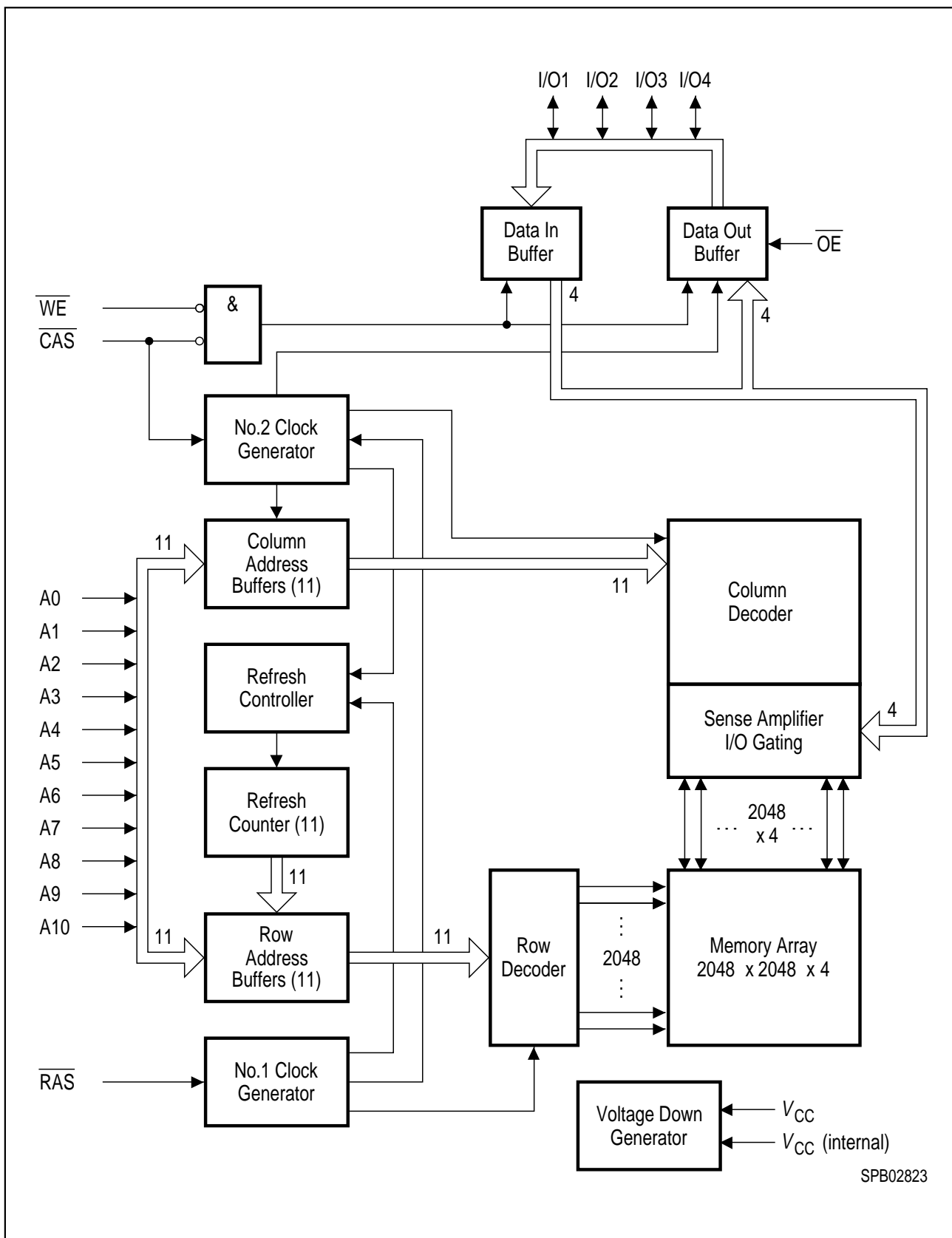
| | HYB 5(3)116400 4k-Refresh | HYB 5(3)117400 2k-Refresh |
|-----------------------|------------------------------|------------------------------|
| Row Address Inputs | A0 - A11 | A0 - A10 |
| Column Address Inputs | A0 - A9 | A0 - A10 |
| Row Address Strobe | | $\overline{\text{RAS}}$ |
| Column Address Strobe | | $\overline{\text{CAS}}$ |
| Output Enable | | $\overline{\text{OE}}$ |
| Data Input/Output | | I/O1 - I/O4 |
| Read/Write Input | | $\overline{\text{WE}}$ |
| Power Supply | | V_{CC} |
| Ground (0 V) | | V_{SS} |
| Not Connected | — | N.C. |

Pin Configuration





Block Diagram for HYB 5(3)116400 (4k-refresh)



SPB02823

Block Diagram for HYB 5(3)117400 (2k-refresh)

Absolute Maximum Ratings

| | |
|---|--|
| Operating temperature range | 0 to 70 °C |
| Storage temperature range..... | – 55 to 150 °C |
| Input/output voltage (5 V versions) | – 0.5 to min ($V_{CC} + 0.5$, 7.0) V |
| Input/output voltage (3.3 V versions) | – 0.5 to min ($V_{CC} + 0.5$, 4.6) V |
| Power supply voltage (5 V versions) | – 1.0 V to 7.0 V |
| Power supply voltage (3.3 V versions) | – 1.0 V to 4.6 V |
| Power dissipation(5 V versions) | 1.0 W |
| Power dissipation (3.3 V versions) | 0.5 W |
| Data out current (short circuit) | 50 mA |

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $t_T = 2$ ns

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|----------|----------------|----------------|------|----------------|
| | | min. | max. | | |
| 5 V Versions | | | | | |
| Power supply voltage | V_{CC} | 4.5 | 5.5 | V | |
| Input high voltage | V_{IH} | 2.4 | $V_{CC} + 0.5$ | V | 1 |
| Input low voltage | V_{IL} | – 0.5 | 0.8 | V | 1 |
| Output high voltage ($I_{OUT} = -5$ mA) | V_{OH} | 2.4 | – | V | 1 |
| Output low voltage ($I_{OUT} = 4.2$ mA) | V_{OL} | – | 0.4 | V | 1 |
| 3.3 V Versions | | | | | |
| Power supply voltage | V_{CC} | 3.0 | 3.6 | V | |
| Input high voltage | V_{IH} | 2.0 | $V_{CC} + 0.5$ | V | 1 |
| Input low voltage | V_{IL} | – 0.5 | 0.8 | V | 1 |
| TTL Output high voltage ($I_{OUT} = -2$ mA) | V_{OH} | 2.4 | – | V | 1 |
| TTL Output low voltage ($I_{OUT} = 2$ mA) | V_{OL} | – | 0.4 | V | 1 |
| CMOS Output high voltage ($I_{OUT} = -100$ μA) | V_{OH} | $V_{CC} - 0.2$ | – | V | |
| CMOS Output low voltage ($I_{OUT} = 100$ μA) | V_{OL} | – | 0.2 | V | |

DC Characteristics (cont'd)

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $t_T = 2$ ns

| Parameter | Symbol | Limit Values | | Unit | Notes | |
|--|------------|--------------|----------|----------|----------------------------|--------------------|
| | | min. | max. | | | |
| | | | 2k | | | 4k |
| Common Parameters | | | | | | |
| Input leakage current ($0 \text{ V} \leq V_{IH} \leq V_{CC} + 0.3 \text{ V}$, all other pins = 0 V) | $I_{I(L)}$ | - 10 | 10 | | μA | 1 |
| Output leakage current (DO is disabled, $0 \text{ V} \leq V_{OUT} \leq V_{CC} + 0.3 \text{ V}$) | $I_{O(L)}$ | - 10 | 10 | | μA | 1 |
| Average V_{CC} supply current -50 ns version -60 ns version ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, address cycling: $t_{RC} = t_{RC \text{ MIN.}}$) | I_{CC1} | - | 80 70 | 50 40 | mA mA | 2, 3, 4 2, 3, 4 |
| Standby V_{CC} supply current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$) | I_{CC2} | - | 2 | | mA | - |
| Average V_{CC} supply current, during $\overline{\text{RAS}}$ -only refresh cycles -50 ns version -60 ns version ($\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = t_{RC \text{ MIN.}}$) | I_{CC3} | - | 80 70 | 50 40 | mA mA | 2, 4 2, 4 |
| Average V_{CC} supply current, during fast page mode -50 ns version -60 ns version ($\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, address cycling: $t_{PC} = t_{PC \text{ MIN.}}$) | I_{CC4} | - | 25 20 | | mA mA | 2, 3, 4 2, 3, 4 |
| Standby V_{CC} supply current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2 \text{ V}$) | I_{CC5} | - | 1 | | mA | 1 |
| Average V_{CC} supply current, during $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode -50 ns version -60 ns version ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling: $t_{RC} = t_{RC \text{ MIN.}}$) | I_{CC6} | - | 80 70 | 50 40 | mA mA | 2, 4 2, 4 |

Capacitance

$T_A = 0$ to 70 °C, $f = 1$ MHz

| Parameter | Symbol | Limit Values | | Unit |
|---|----------|--------------|------|------|
| | | min. | max. | |
| Input capacitance (A0 to A11) | C_{I1} | – | 5 | pF |
| Input capacitance (\overline{RAS} , \overline{CAS} , \overline{WE} , \overline{OE}) | C_{I2} | – | 7 | pF |
| I/O capacitance (I/O1 - I/O4) | C_{IO} | – | 7 | pF |

AC Characteristics ^{5, 6}

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V ± 10 % / $V_{CC} = 3.3$ V ± 0.3 V, $t_T = 5$ ns

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|-----------|--------|--------------|------|------|------|------|------|
| | | -50 | | -60 | | | |
| | | min. | max. | min. | max. | | |

Common Parameters

| | | | | | | | |
|---|-----------|----|-----|-----|-----|----|--------------|
| Random read or write cycle time | t_{RC} | 90 | – | 110 | – | ns | |
| \overline{RAS} precharge time | t_{RP} | 30 | – | 40 | – | ns | |
| \overline{RAS} pulse width | t_{RAS} | 50 | 10k | 60 | 10k | ns | |
| \overline{CAS} pulse width | t_{CAS} | 13 | 10k | 15 | 10k | ns | |
| Row address setup time | t_{ASR} | 0 | – | 0 | – | ns | |
| Row address hold time | t_{RAH} | 8 | – | 10 | – | ns | |
| Column address setup time | t_{ASC} | 0 | – | 0 | – | ns | |
| Column address hold time | t_{CAH} | 10 | – | 15 | – | ns | |
| \overline{RAS} to \overline{CAS} delay time | t_{RCD} | 18 | 37 | 20 | 45 | | |
| \overline{RAS} to column address delay time | t_{RAD} | 13 | 25 | 15 | 30 | ns | |
| \overline{RAS} hold time | t_{RSH} | 13 | | 15 | – | ns | |
| \overline{CAS} hold time | t_{CSH} | 50 | | 60 | – | ns | |
| \overline{CAS} to \overline{RAS} precharge time | t_{CRP} | 5 | – | 5 | – | ns | |
| Transition time (rise and fall) | t_T | 3 | 50 | 3 | 50 | ns | ⁷ |
| Refresh period for 2k refresh version | t_{REF} | – | 32 | – | 32 | ms | |
| Refresh period for 4k refresh version | t_{REF} | – | 64 | – | 64 | ms | |

Read Cycle

| | | | | | | | |
|-----------------------------------|-----------|---|----|---|----|----|-------|
| Access time from \overline{RAS} | t_{RAC} | – | 50 | – | 60 | ns | 8, 9 |
| Access time from \overline{CAS} | t_{CAC} | – | 13 | – | 15 | ns | 8, 9 |
| Access time from column address | t_{AA} | – | 25 | – | 30 | ns | 8, 10 |

AC Characteristics (cont'd) ^{5, 6}

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V \pm 10 % / $V_{CC} = 3.3$ V \pm 0.3 V, $t_T = 5$ ns

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|---|-----------|--------------|------|------|------|------|------|
| | | -50 | | -60 | | | |
| | | min. | max. | min. | max. | | |
| \overline{OE} access time | t_{OEA} | – | 13 | – | 15 | ns | |
| Column address to \overline{RAS} lead time | t_{RAL} | 25 | – | 30 | – | ns | |
| Read command setup time | t_{RCS} | 0 | – | 0 | – | ns | |
| Read command hold time | t_{RCH} | 0 | – | 0 | – | ns | 11 |
| Read command hold time referenced to \overline{RAS} | t_{RRH} | 0 | – | 0 | – | ns | 11 |
| \overline{CAS} to output in low-Z | t_{CLZ} | 0 | – | 0 | – | ns | 8 |
| Output buffer turn-off delay | t_{OFF} | 0 | 13 | 0 | 15 | ns | 12 |
| Output buffer turn-off delay from \overline{OE} | t_{OEZ} | 0 | 13 | 0 | 15 | ns | 12 |
| Data to \overline{OE} low delay | t_{DZO} | 0 | – | 0 | – | ns | 13 |
| \overline{CAS} high to data delay | t_{CDD} | 13 | – | 15 | – | ns | 14 |
| \overline{OE} high to data delay | t_{ODD} | 13 | – | 15 | – | ns | 14 |

Write Cycle

| | | | | | | | |
|---|-----------|----|---|----|---|----|----|
| Write command hold time | t_{WCH} | 8 | – | 10 | – | ns | |
| Write command pulse width | t_{WCP} | 8 | – | 10 | – | ns | |
| Write command setup time | t_{WCS} | 0 | – | 0 | – | ns | 15 |
| Write command to \overline{RAS} lead time | t_{RWL} | 13 | – | 15 | – | ns | |
| Write command to \overline{CAS} lead time | t_{CWL} | 13 | – | 15 | – | ns | |
| Data setup time | t_{DS} | 0 | – | 0 | – | ns | 16 |
| Data hold time | t_{DH} | 10 | – | 10 | – | ns | 16 |
| Data to \overline{CAS} low delay | t_{DZC} | 0 | – | 0 | – | ns | 13 |

Read-Modify-Write Cycle

| | | | | | | | |
|--|-----------|-----|---|-----|---|----|----|
| Read-write cycle time | t_{RWC} | 126 | – | 150 | – | ns | |
| \overline{RAS} to \overline{WE} delay time | t_{RWD} | 68 | – | 80 | – | ns | 15 |
| \overline{CAS} to \overline{WE} delay time | t_{CWD} | 31 | – | 35 | – | ns | 15 |
| Column address to \overline{WE} delay time | t_{AWD} | 43 | – | 50 | – | ns | 15 |
| \overline{OE} command hold time | t_{OEH} | 13 | – | 15 | – | ns | |

AC Characteristics (cont'd) ^{5, 6}

$T_A = 0$ to 70 °C, $V_{CC} = 5\text{ V} \pm 10\%$ / $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $t_T = 5\text{ ns}$

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|-----------|--------|--------------|------|------|------|------|------|
| | | -50 | | -60 | | | |
| | | min. | max. | min. | max. | | |

Fast Page Mode Cycle

| | | | | | | | |
|--|------------|----|------|----|------|----|--------------|
| Fast page mode cycle time | t_{PC} | 35 | – | 40 | – | ns | |
| $\overline{\text{CAS}}$ precharge time | t_{CP} | 10 | – | 10 | – | ns | |
| Access time from $\overline{\text{CAS}}$ precharge | t_{CPA} | – | 30 | – | 35 | ns | ⁷ |
| $\overline{\text{RAS}}$ pulse width | t_{RAS} | 50 | 200k | 60 | 200k | ns | |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay | t_{RHPC} | 30 | – | 35 | – | ns | |

Fast Page Mode Read-Modify-Write Cycle

| | | | | | | | |
|---|------------|----|---|----|---|----|--|
| Fast page mode read-write cycle time | t_{PRWC} | 71 | – | 80 | – | ns | |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ | t_{CPWD} | 48 | – | 55 | – | ns | |

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

| | | | | | | | |
|---|-----------|----|---|----|---|----|--|
| $\overline{\text{CAS}}$ setup time | t_{CSR} | 10 | – | 10 | – | ns | |
| $\overline{\text{CAS}}$ hold time | t_{CHR} | 10 | – | 10 | – | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time | t_{RPC} | 5 | – | 5 | – | ns | |
| Write to $\overline{\text{RAS}}$ precharge time | t_{WRP} | 10 | – | 10 | – | ns | |
| Write hold time referenced to $\overline{\text{RAS}}$ | t_{WRH} | 10 | – | 10 | – | ns | |

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

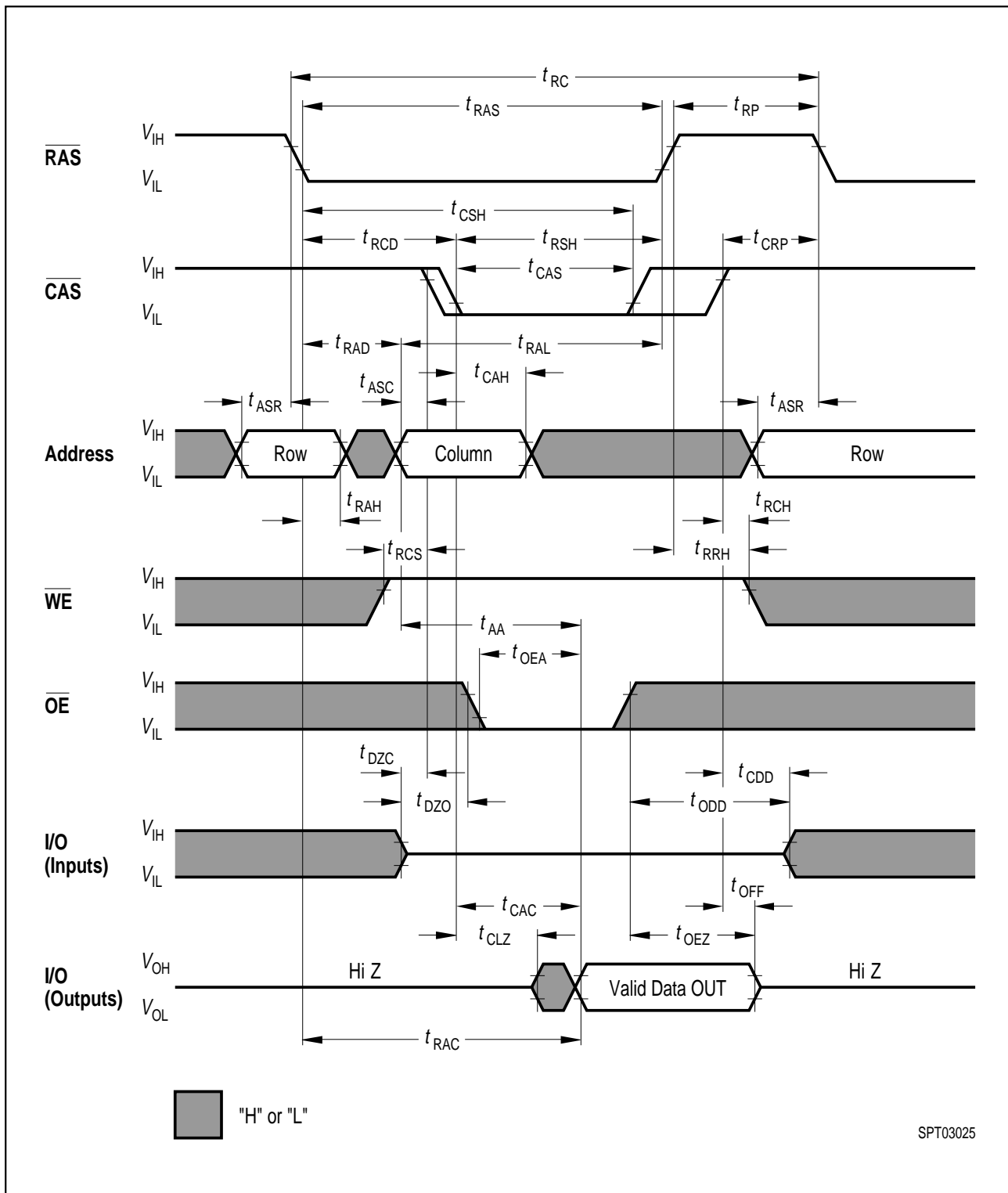
| | | | | | | | |
|--|-----------|----|---|----|---|----|--|
| $\overline{\text{CAS}}$ precharge time | t_{CPT} | 35 | – | 40 | – | ns | |
|--|-----------|----|---|----|---|----|--|

Test Mode

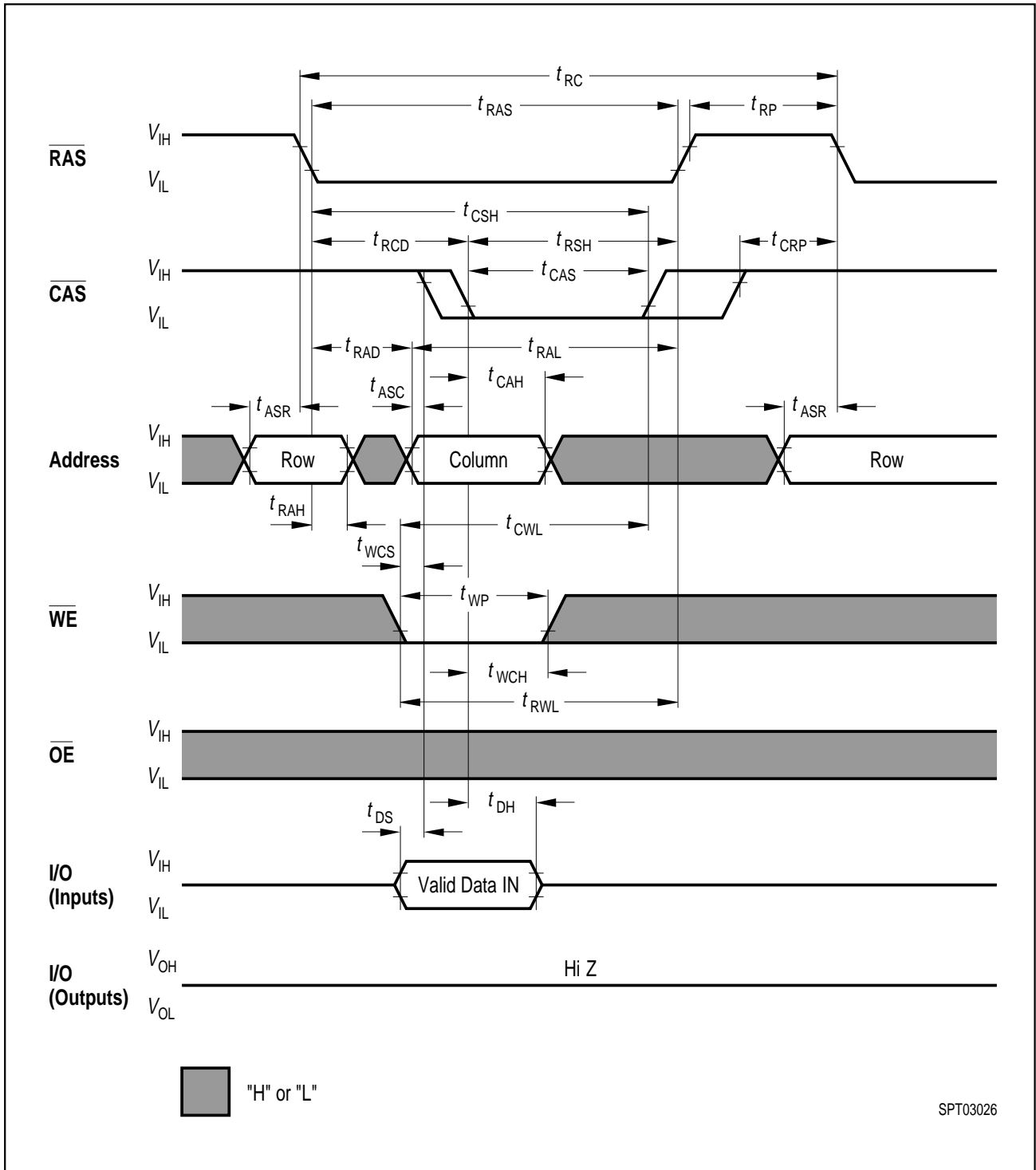
| | | | | | | | |
|--|------------|----|---|----|---|----|--|
| $\overline{\text{CAS}}$ hold time | t_{CHRT} | 30 | – | 30 | – | ns | |
| Write command setup time | t_{WTS} | 10 | – | 10 | – | ns | |
| Write command hold time | t_{WTH} | 10 | – | 10 | – | ns | |
| $\overline{\text{RAS}}$ hold time in test mode | t_{RAHT} | 30 | – | 30 | – | ns | |

Notes

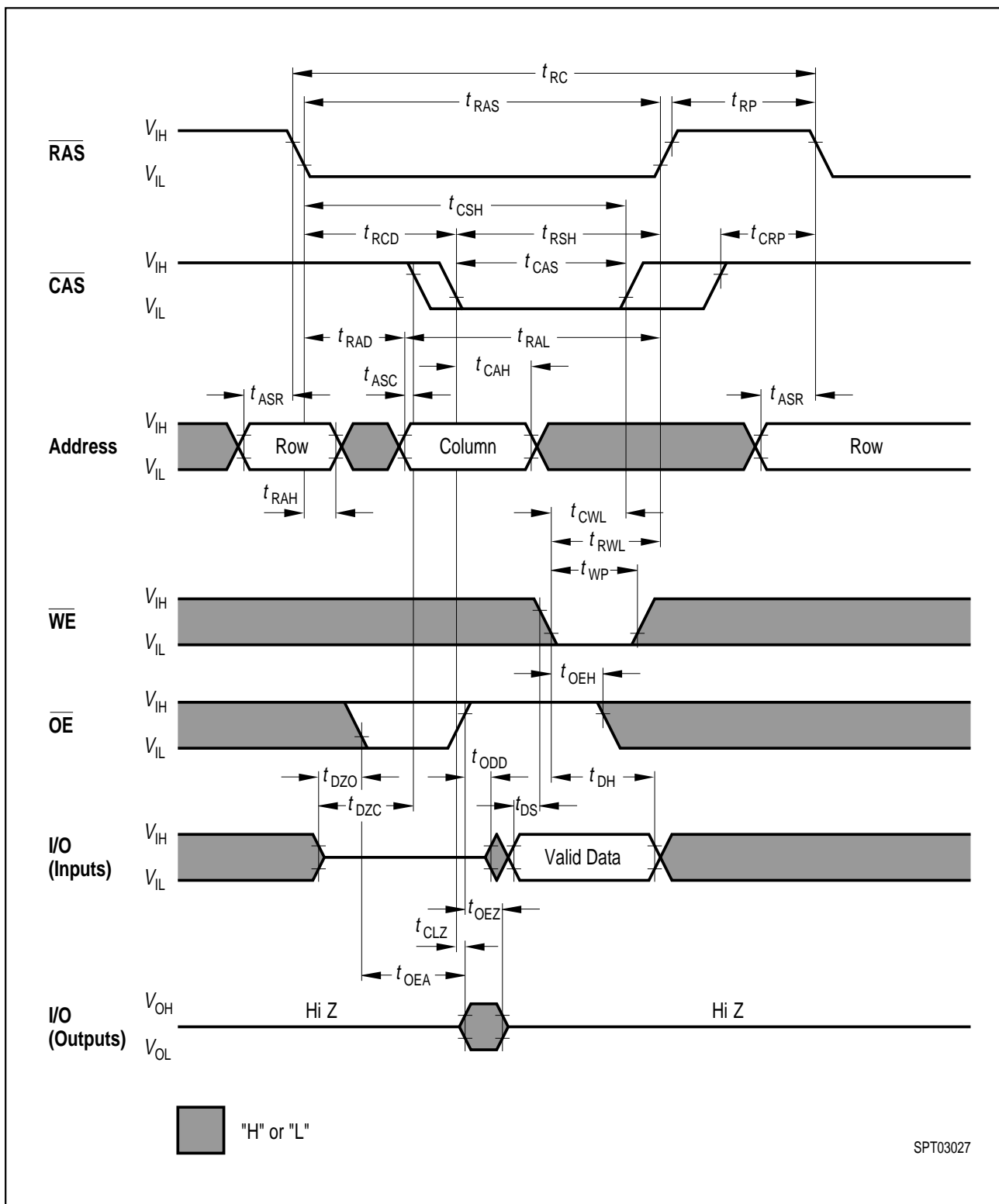
1. All voltages are referenced to V_{SS} .
2. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
3. I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while $\overline{RAS} = V_{IL}$. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).
5. An initial pause of 200 μs is required after power-up followed by 8 \overline{RAS} cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required.
6. AC measurements assume $t_T = 5$ ns.
7. $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
8. Measured with a load equivalent to 2 TTL loads and 100 pF.
9. Operation within the $t_{RCD(MAX.)}$ limit ensures that $t_{RAC(MAX.)}$ can be met. $t_{RCD(MAX.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD(MAX.)}$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD(MAX.)}$ limit ensures that $t_{RAC(MAX.)}$ can be met. $t_{RAD(MAX.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD(MAX.)}$ limit, then access time is controlled by t_{AA} .
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
13. Either t_{DZC} or t_{DZO} must be satisfied.
14. Either t_{CDD} or t_{ODD} must be satisfied.
15. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS(MIN.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD(MIN.)}$, $t_{CWD} > t_{CWD(MIN.)}$, $t_{AWD} > t_{AWD(MIN.)}$ and $t_{CPWD} > t_{CPWD(MIN.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
16. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{WE} leading edge in read-write cycles.



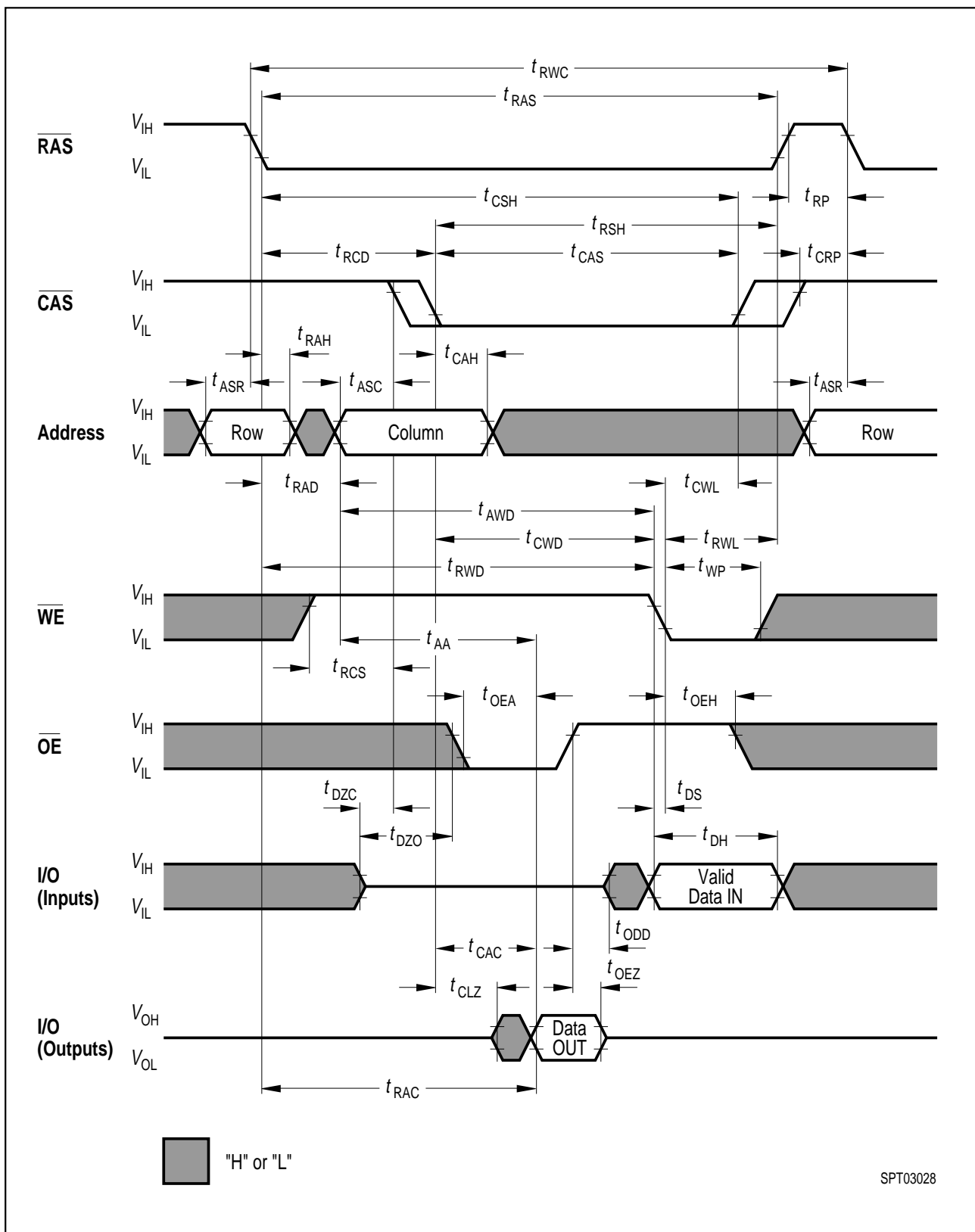
Read Cycle



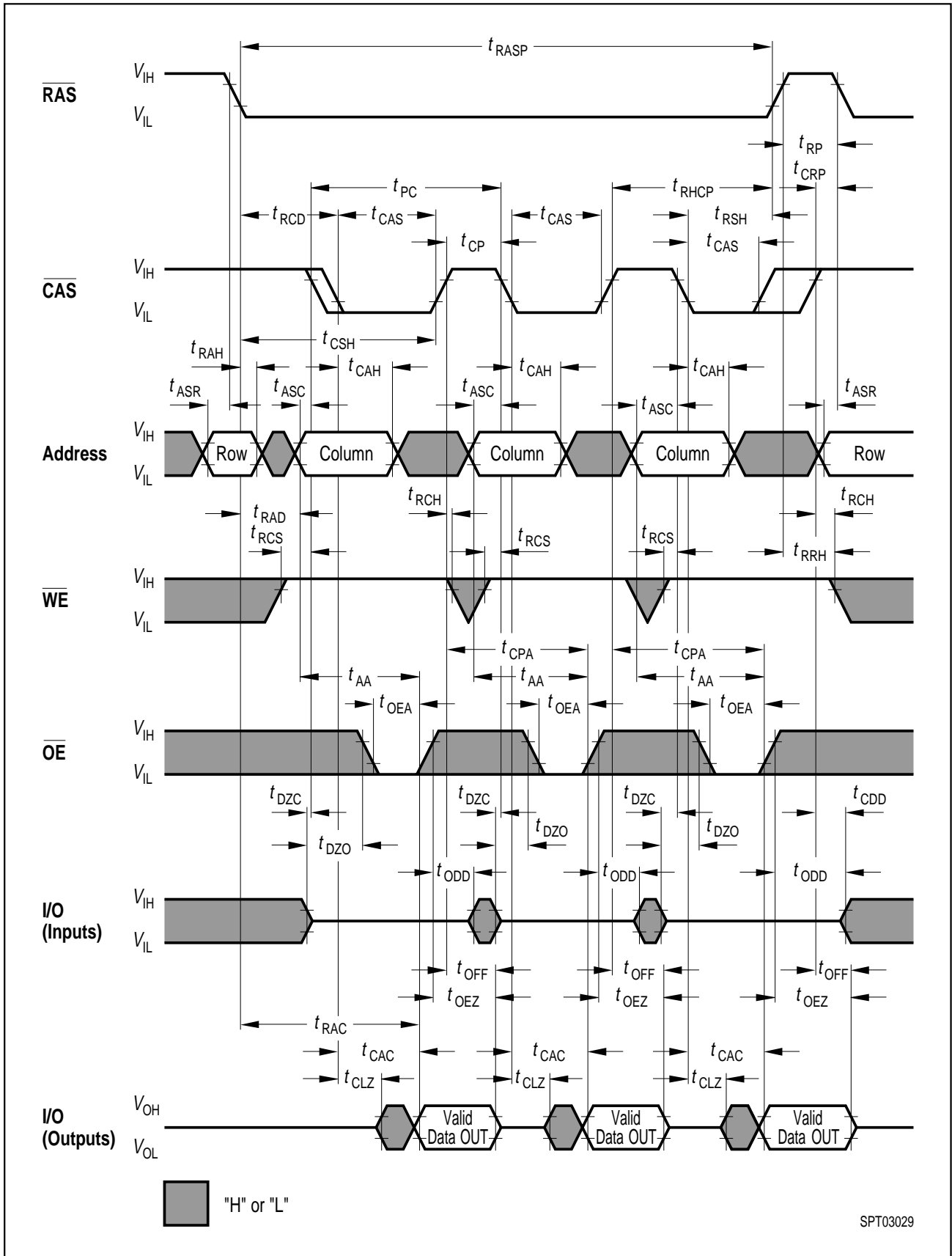
Write Cycle (Early Write)



Write Cycle (\overline{OE} Controlled Write)

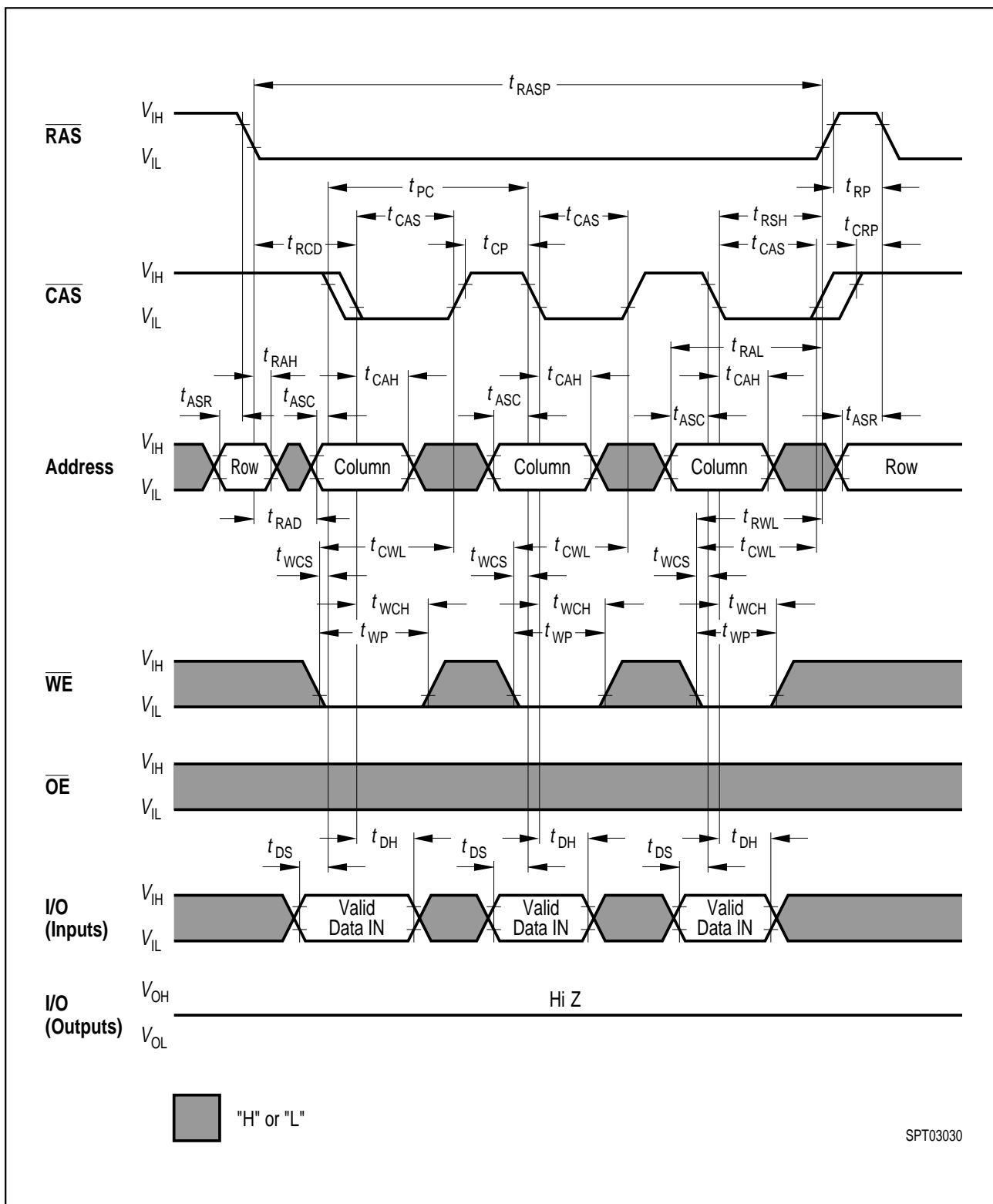


Read-Write (Read-Modify-Write) Cycle

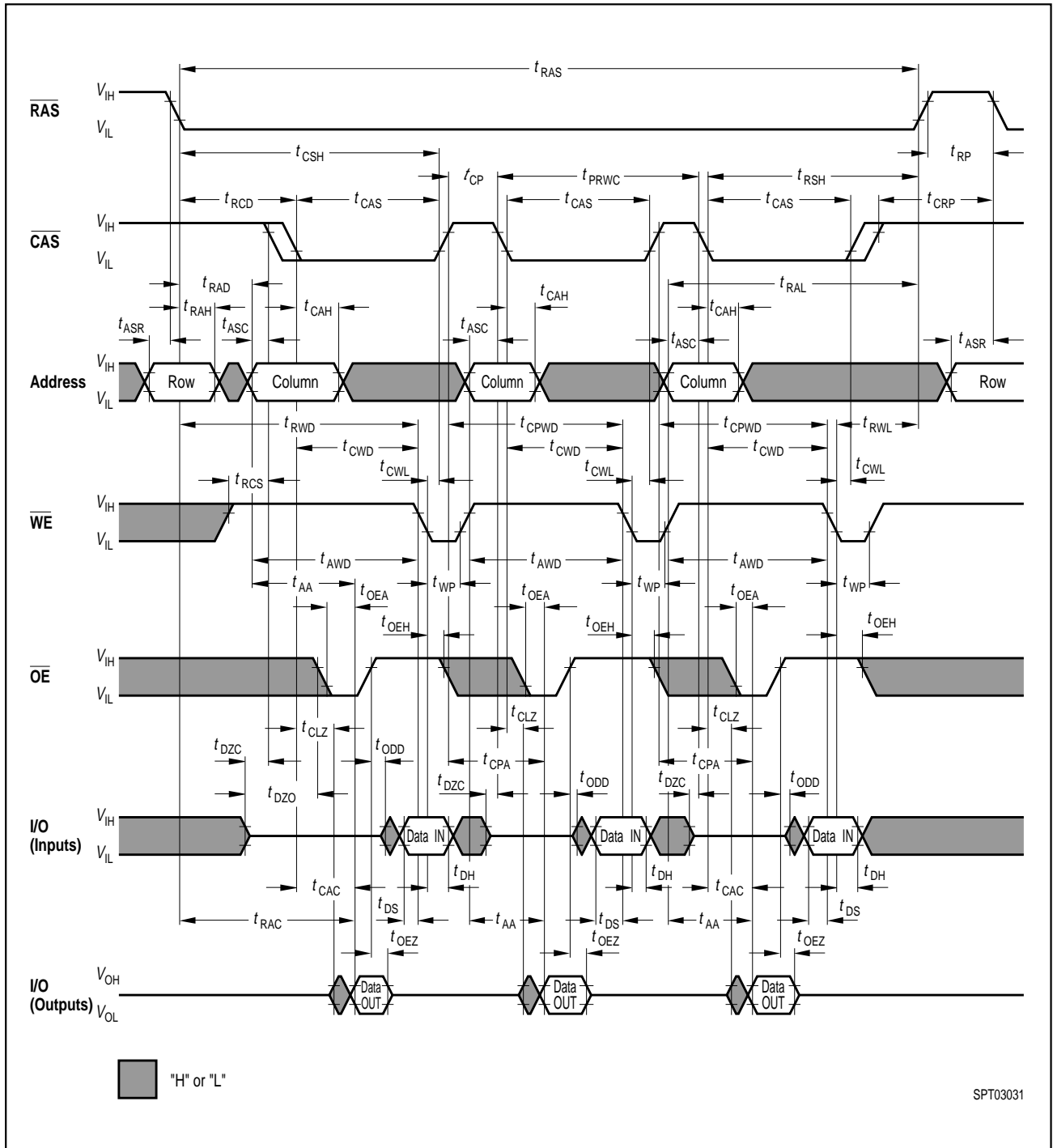


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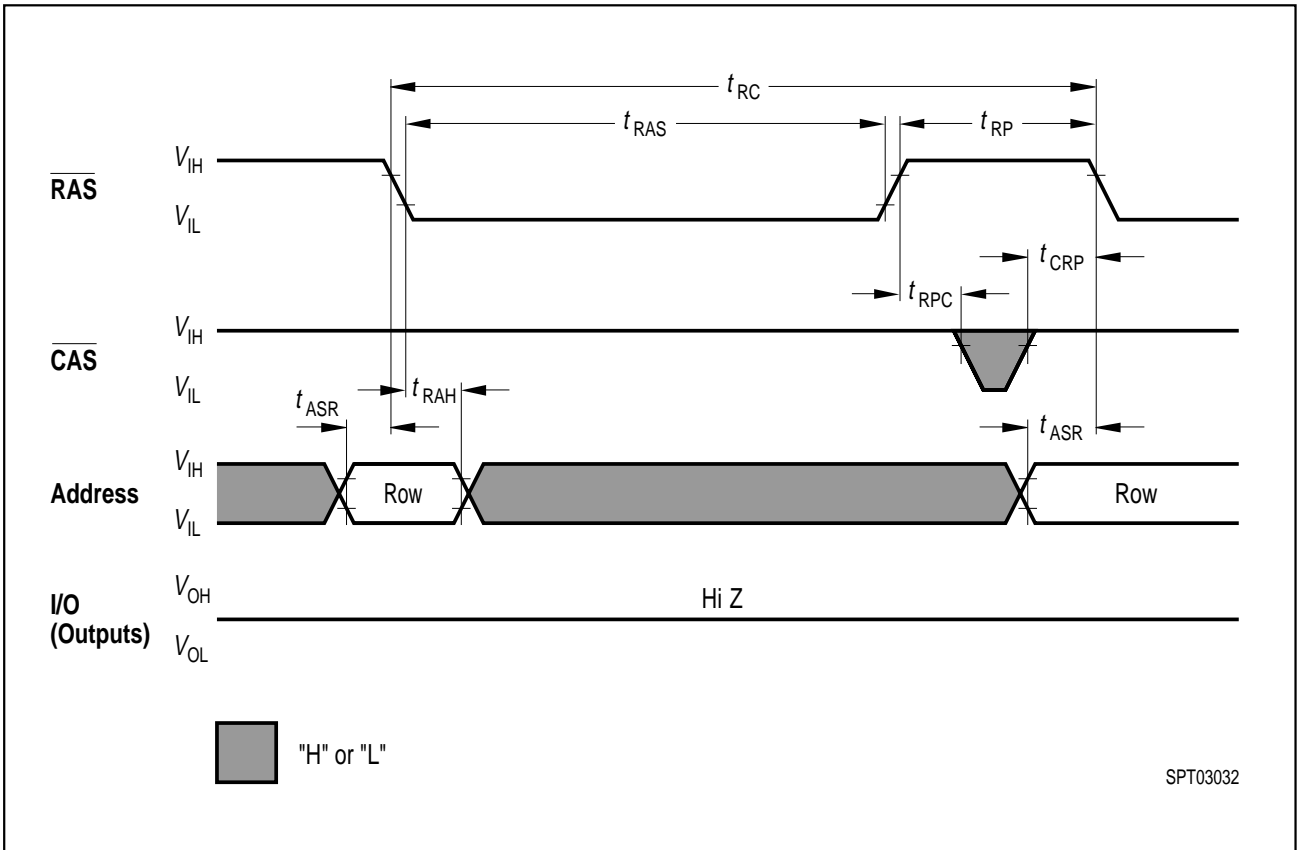
Fast Page Mode Read Cycle



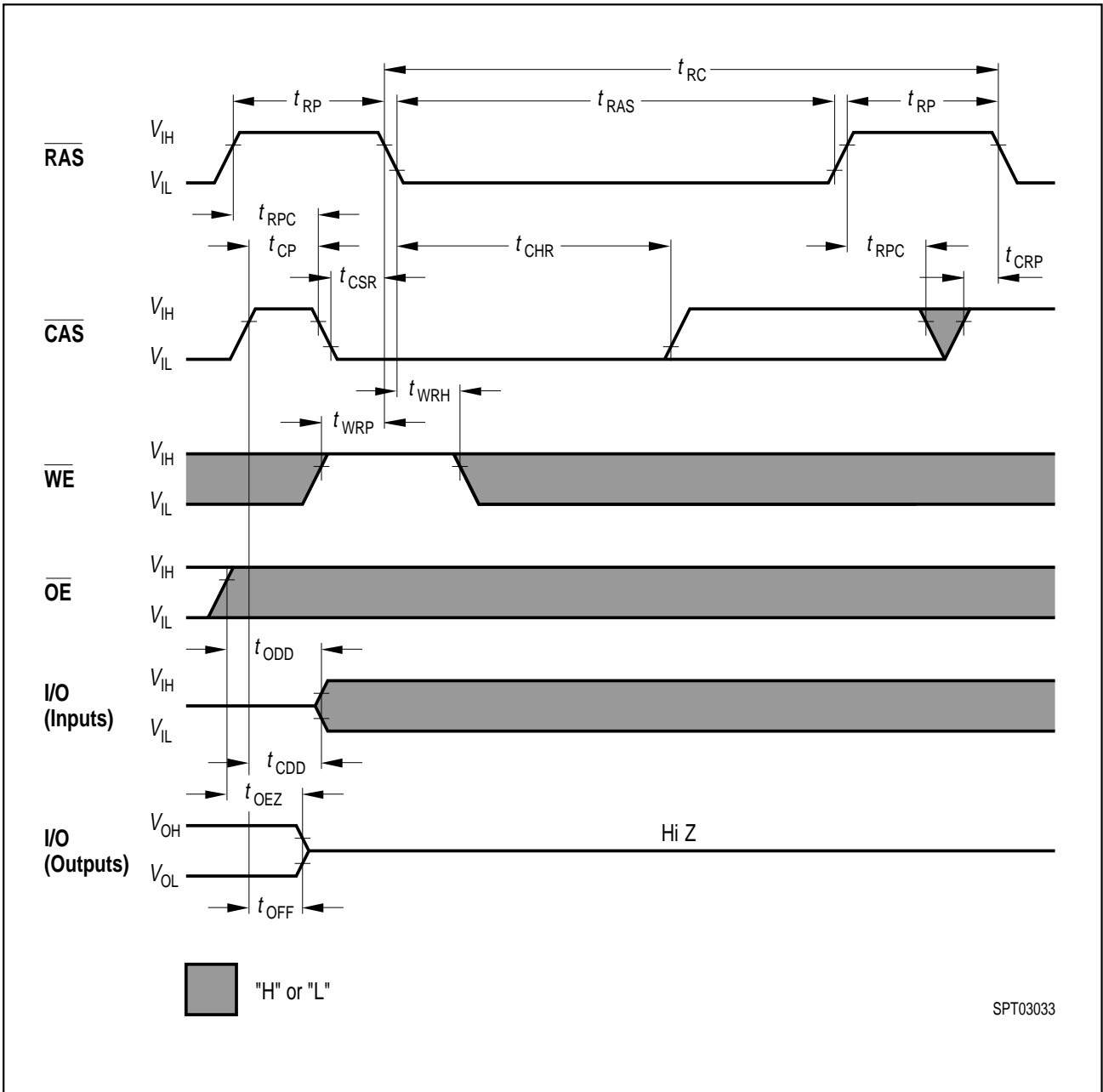
Fast Page Mode Early Write Cycle



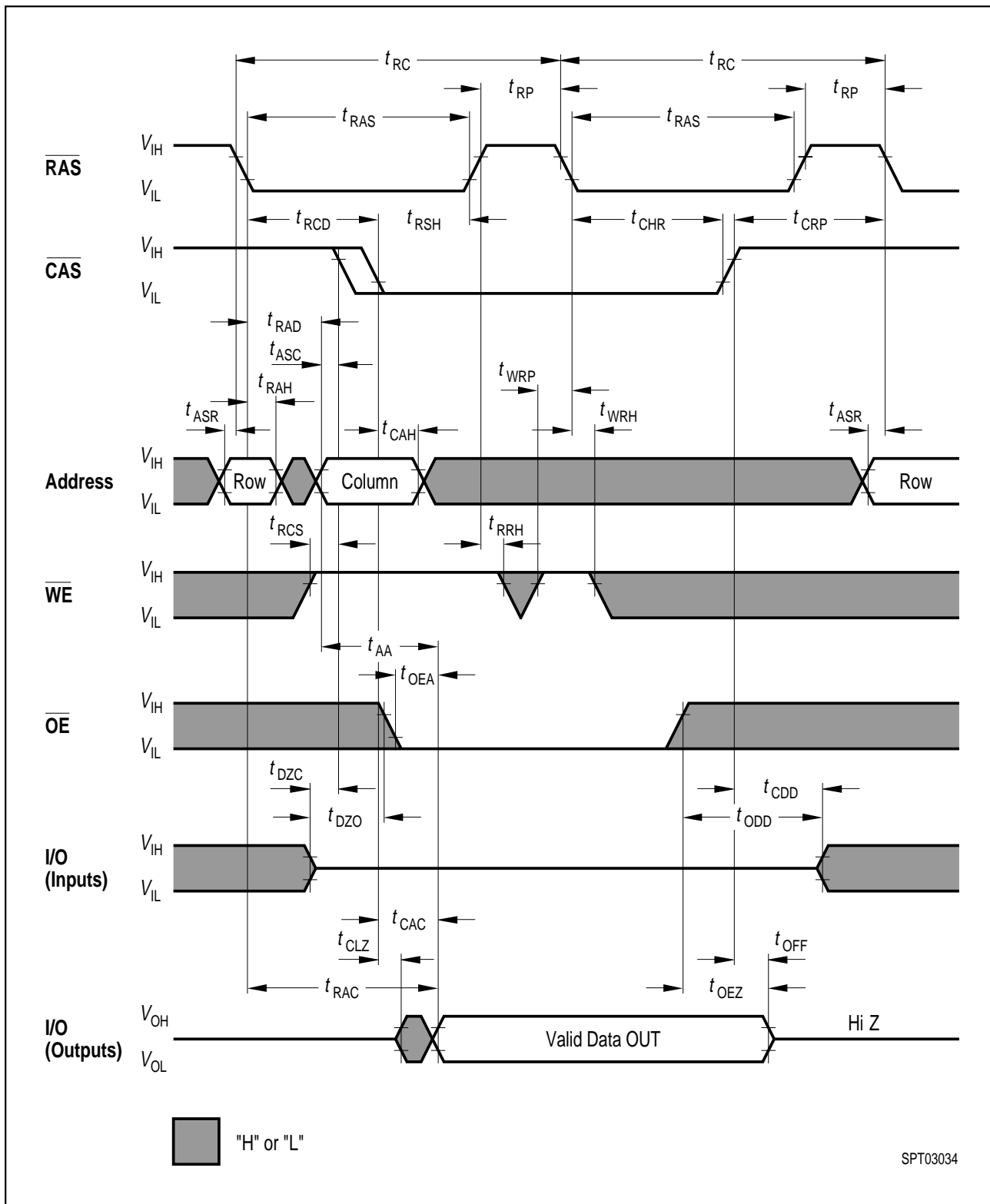
Fast Page Mode Late Write and Read-Modify Write Cycle



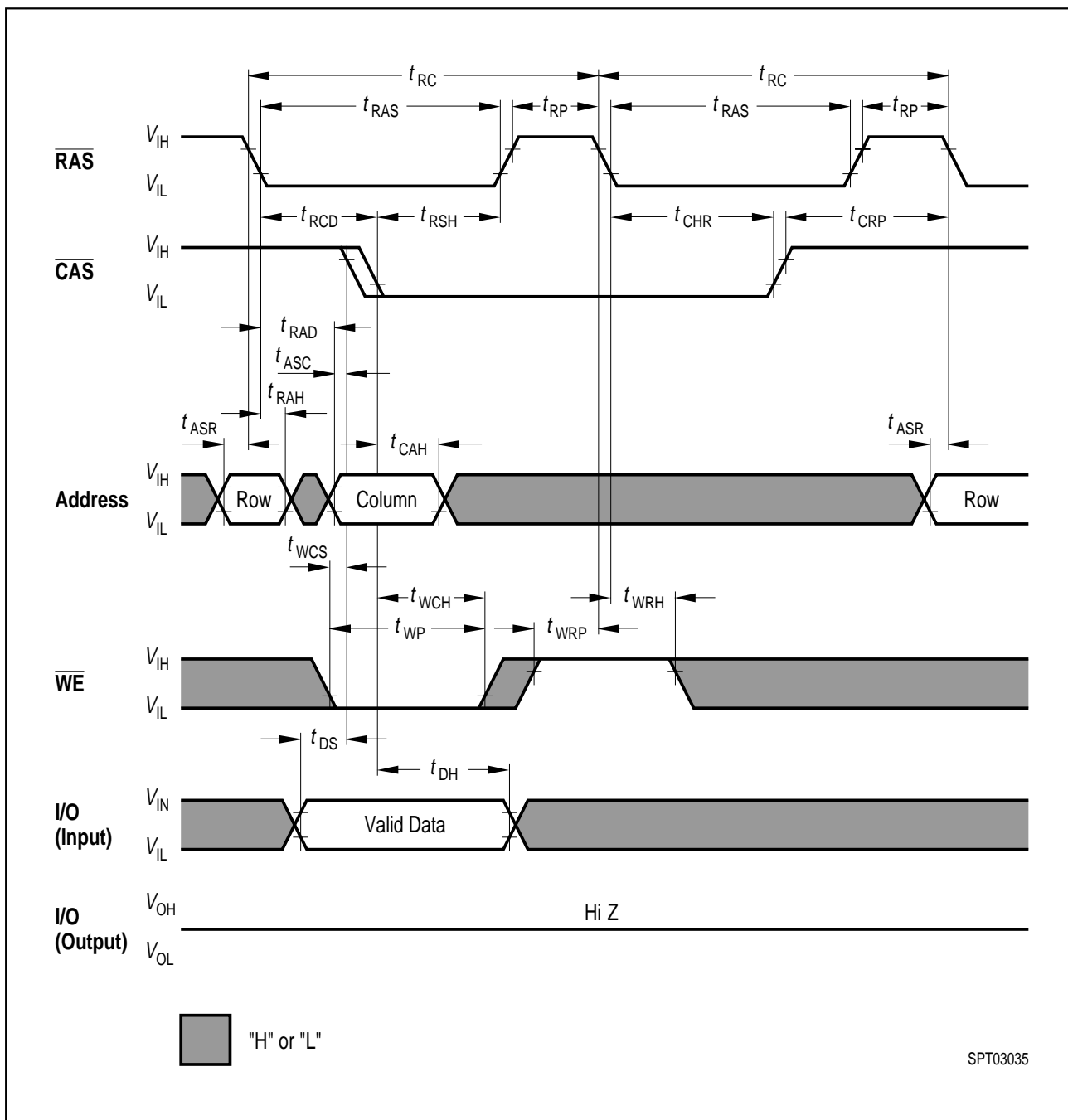
$\overline{\text{RAS}}$ -only Refresh Cycle



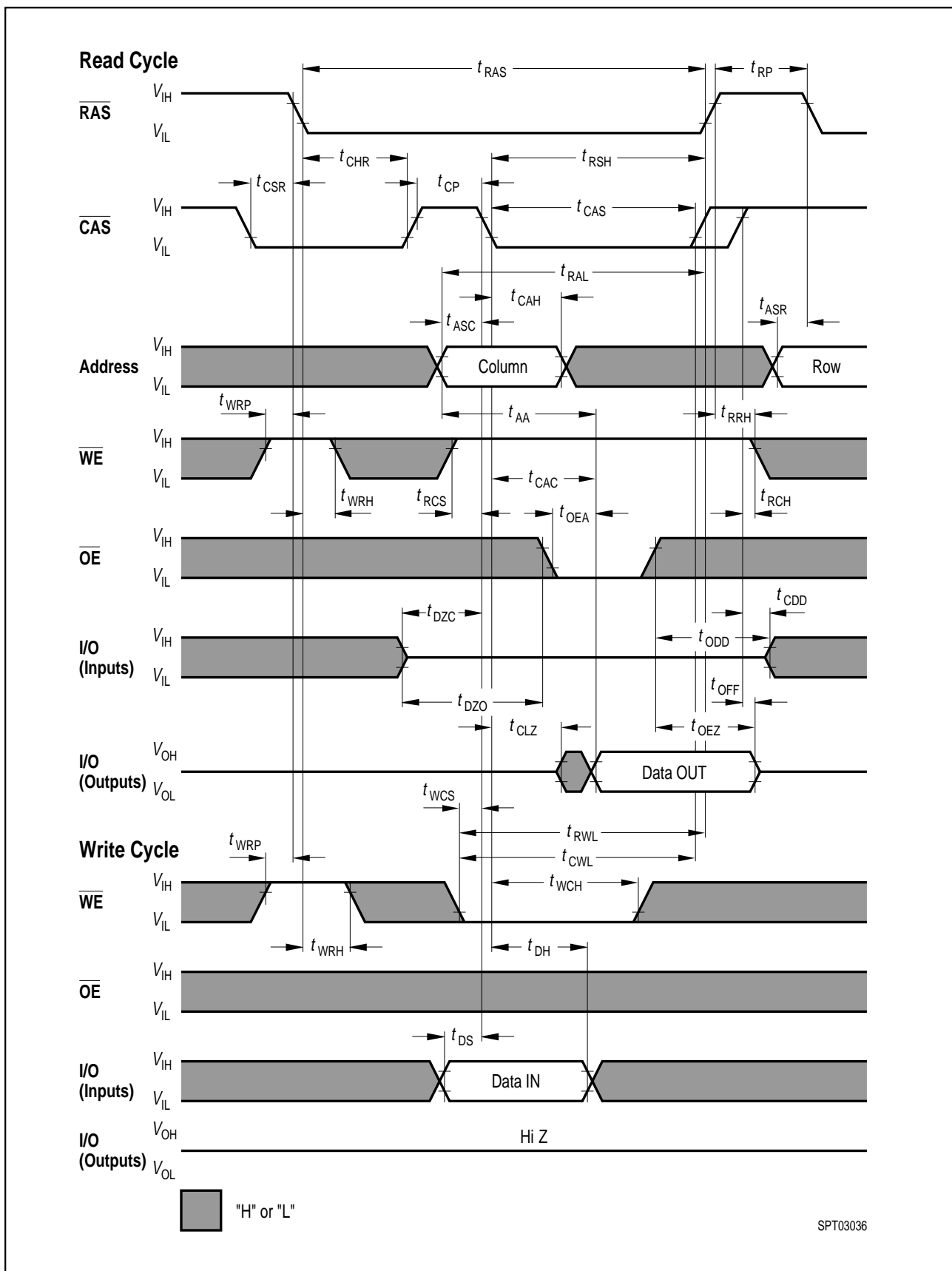
CAS-before-RAS Refresh Cycle



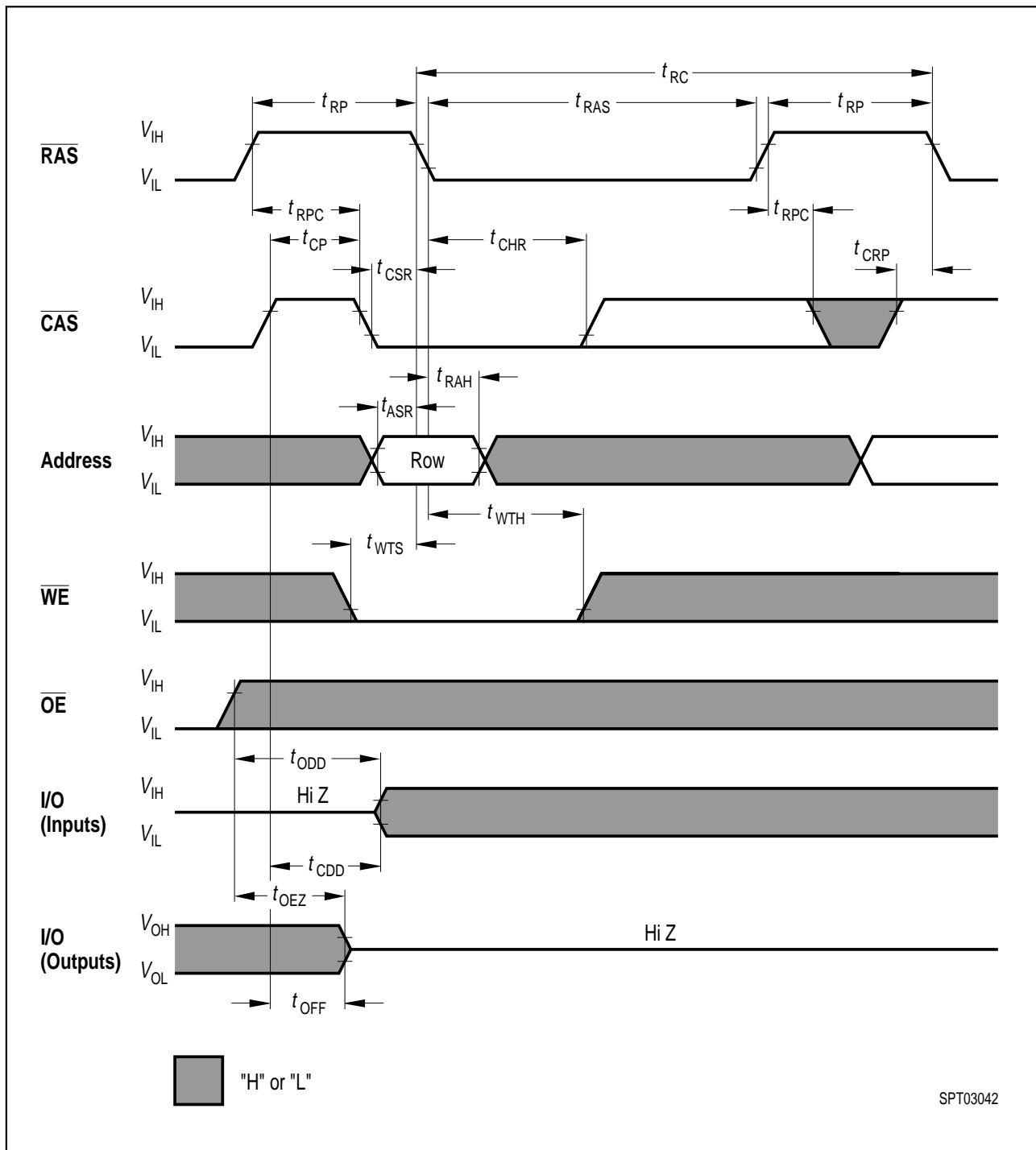
Hidden Refresh Cycle (Read) Cycle



Hidden Refresh Early Write Cycle



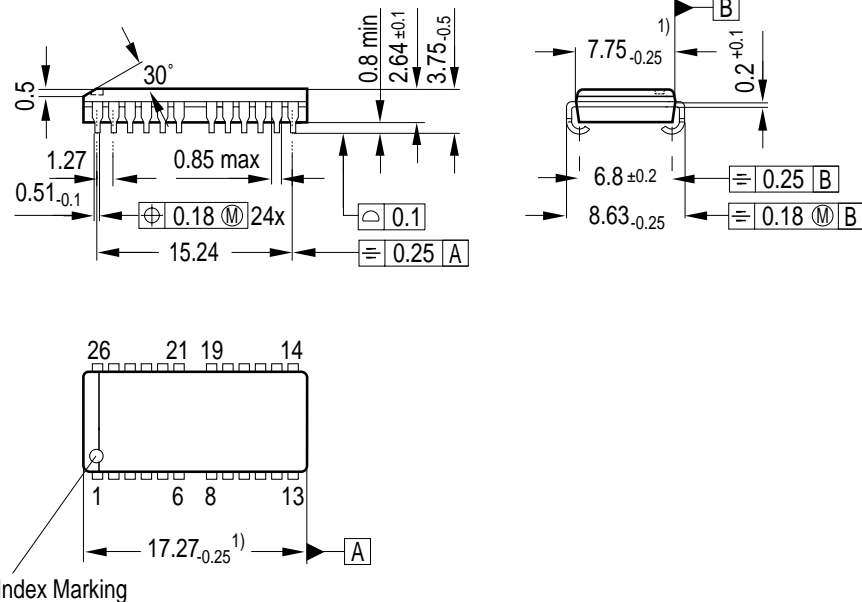
CAS-before-RAS Refresh Counter Test Cycle



Test Mode Entry

Package Outlines

Plastic Package P-SOJ-26/24-1 (SMD) (300mil)
 (Plastic small outline J-leaded)



1) Does not include plastic or metal protrusions of 0.15 max per side

GPJ05628

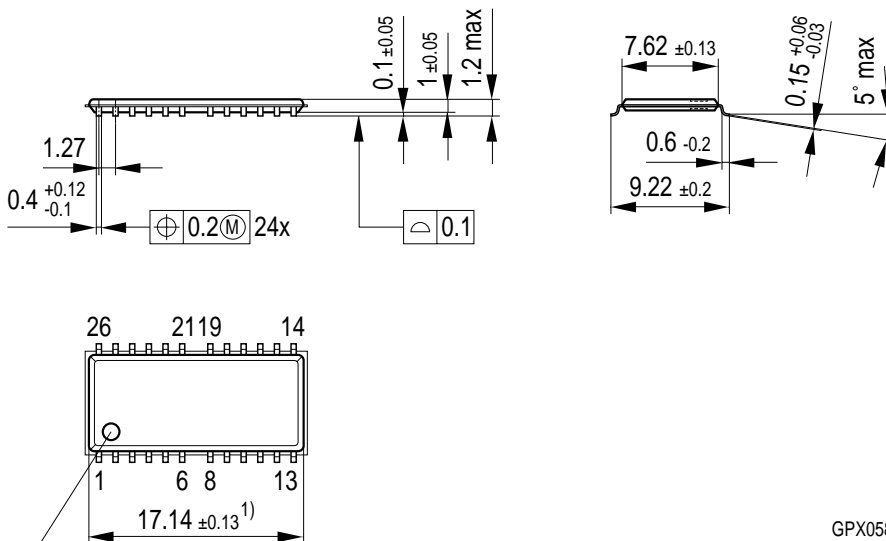
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

**Plastic Package P-TSOPII-26/24-1 (400 mil) (SMD)
(Plastic Thin Small Outline Package (Type II))**



Index Marking

¹⁾ Does not include plastic or metal protrusion of 0.15 max per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm