

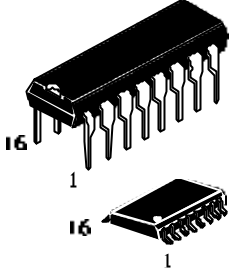
# Dual Up-Counter

## High-Voltage Silicon-Gate CMOS

The SL4518B Dual BCD Up-Counter consists two identical, internally synchronous 4stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply



**H SUFFIX PLASTIC**

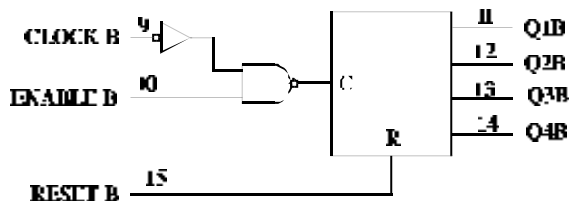
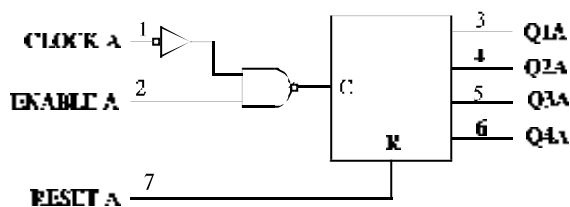
**D SUFFIX SOIC**

**ORDERING INFORMATION**  
 SL4518BN Plastic  
 SL4518BD SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

### PIN ASSIGNMENT

CLOCK A	1	16	V <sub>CC</sub>
ENABLE A	2	15	RESET B
Q1A	3	14	Q4B
Q2A	4	13	Q3B
Q3A	5	12	Q2B
Q4A	6	11	Q1B
RESET A	7	10	ENABLE B
GND	8	9	CLOCK B

### LOGIC DIAGRAM



PIN 16=V<sub>CC</sub>  
 PIN 8= GND

### FUNCTION TABLE

Inputs			Outputs
CLOCK	ENABLE	RESET	Mode
	H	L	Increment Counter
L		L	Increment Counter
	X	L	No Change
X		L	No Change
	L	L	No Change
H		L	No Change
X	X	H	Q1 thru Q4=L

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P <sub>D</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.  
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V V <sub>OUT</sub> = 1.5 V or V <sub>CC</sub> - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V <sub>IL</sub>	Maximum Low -Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V V <sub>OUT</sub> = 1.5 V or V <sub>CC</sub> - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	µA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0	5	5	150	µA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OL</sub> =0.4 V U <sub>OL</sub> =0.5 V U <sub>OL</sub> =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OH</sub> =2.5 V U <sub>OH</sub> =4.6 V U <sub>OH</sub> =9.5 V U <sub>OH</sub> =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

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## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , $R_L=200\text{k}\Omega$ , Input $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$f_{\text{max}}$	Maximum Clock Frequency, (Figure 1)	5.0	1.5	1.5	0.75	MHz
		10	3	3	1.5	
		15	4	4	2	
$t_{\text{PHL}}, t_{\text{PLH}}$	Maximum Propagation Delay, Clock or Enable to Output (Figures 1,3)	5.0	560	560	1120	ns
		10	230	230	460	
		15	160	160	320	
$t_{\text{PHL}}$	Maximum Propagation Delay, Reset to Output (Figure 2)	5.0	650	650	1300	ns
		10	225	225	450	
		15	170	170	340	
$t_{\text{THL}}, t_{\text{TLH}}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
$C_{\text{IN}}$	Maximum Input Capacitance	-		7.5		pF

## TIMING REQUIREMENTS ( $C_L=50\text{pF}$ , $R_L=200\text{ k}\Omega$ , Input $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	70	70	140	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	5.0	250	250	500	ns
		10	110	110	220	
		15	80	80	160	
$t_w$	Minimum Pulse Width, Enable (Figure 3)	5.0	400	400	800	ns
		10	200	200	400	
		15	140	140	280	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	5.0	15	15	15	$\mu\text{s}$
		10	5	5	5	
		15	5	5	5	

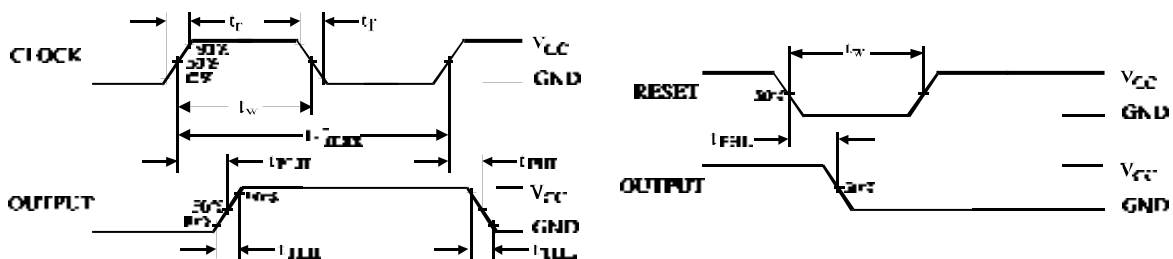


Figure 1. Switching Waveforms

Figure 2. Switching Waveforms

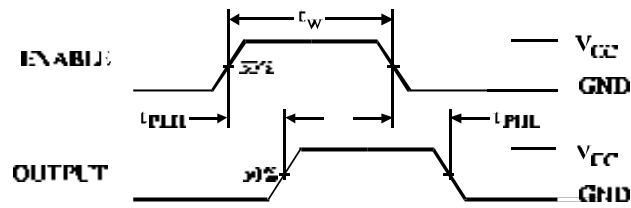
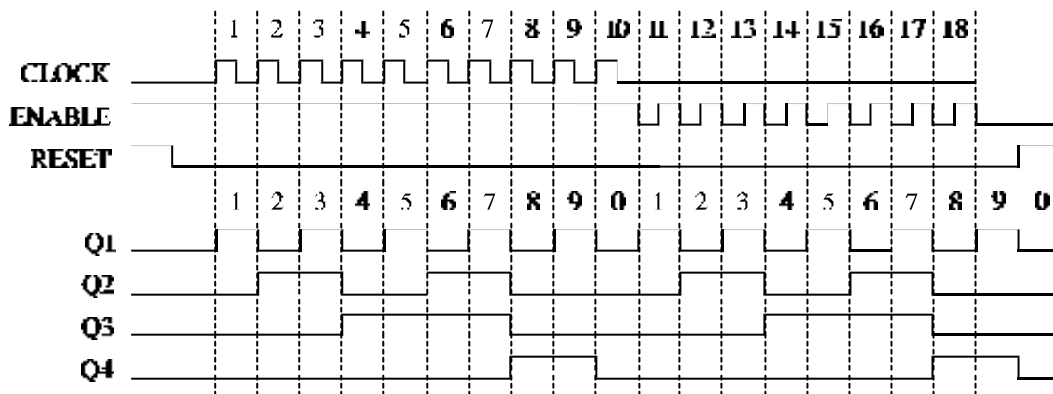


Figure 3. Switching Waveforms

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM  
(1/2 of the Device)

# SL4518B

