SL2150D

Cable Tuner Front End LNA with AGC

Data Sheet

DS5545 ISSUE 2.1 April 2002

Features

- Single chip dual output
- Wide dynamic range on both channels
- Independent AGC facility incorporated into all channel paths
- Independent disable facility incorporated into all channel paths
- Full ESD protection. (Normal ESD handling procedures should be observed)

Applications

- Multi-tuner cable set top box and cable modem applications
- Data communications systems
- Terrestrial TV tuner loop though

Ordering Information

SL2150D/KG/LH1S (tubes)
SL2150D/KG/LH1T (tape and reel)

Description

The SL2150D is a wide dynamic range front end for tuner applications.

The device offers two buffered outputs from a single input, where both paths contain an independently controllable AGC and disable facility.

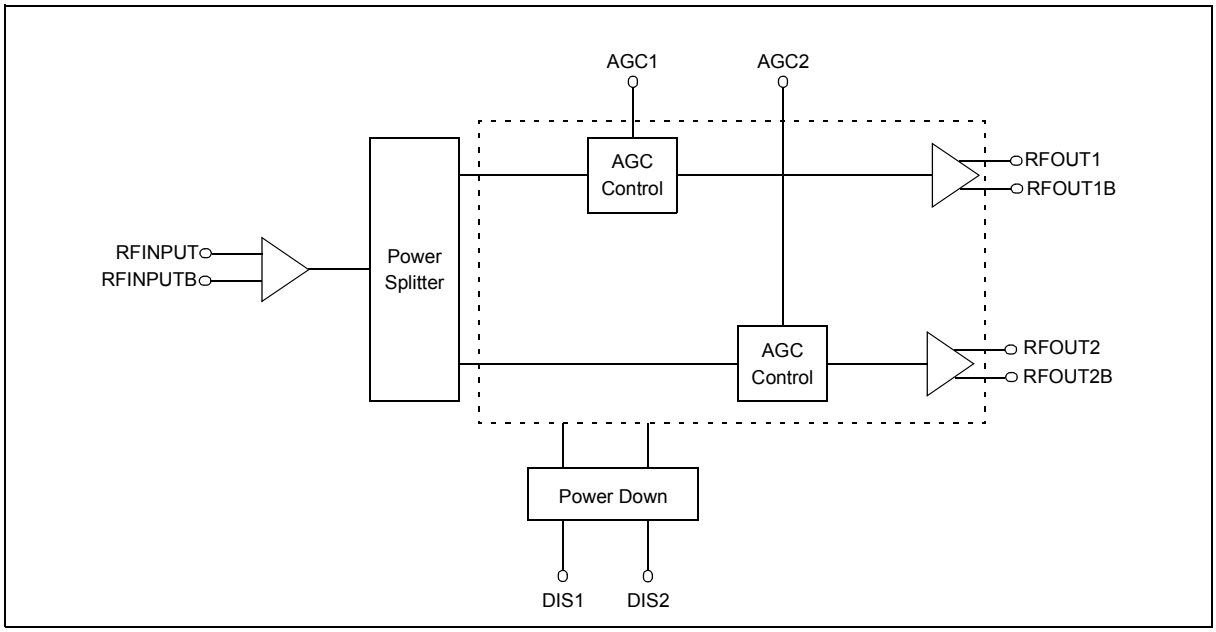


Figure 1 - SL2150D Block Diagram

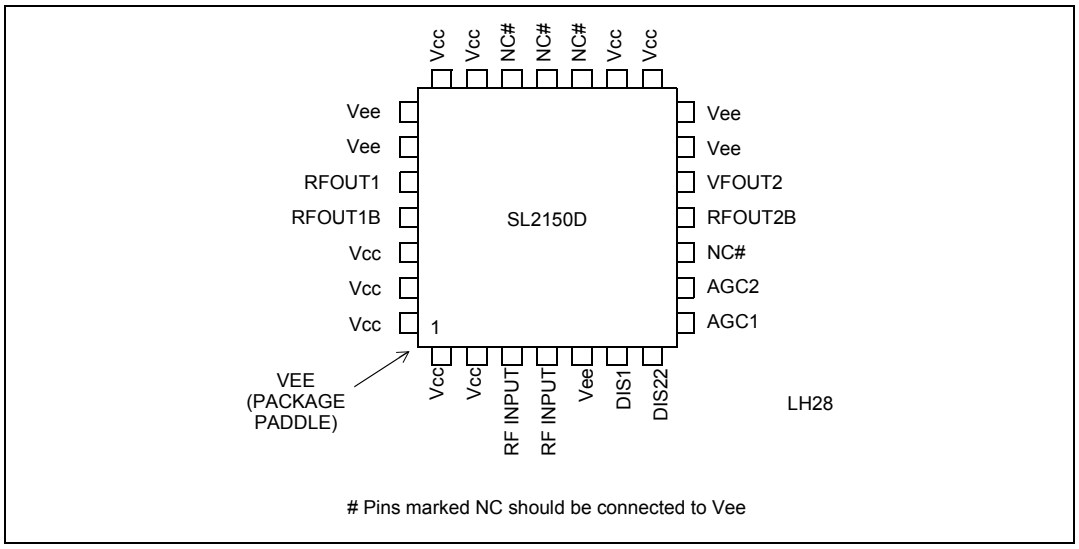


Figure 2 - Pin Allocation

1.0 Quick Reference Data

NB all data applies with differential termination and single ended source both of 75Ω.

Characteristics		Units
RF input operating range	50-860	MHz
Conversion gain, with external load as in Figure 11 maximum minimum	 11 -25	 dB dB
Input NF, both paths enabled at maximum conversion gain	6.4	dB
CTB, both paths enabled, all gain settings *	-66	dBc
CSO, both paths enabled, all gain settings *	-64	dBc
CXM, both paths enabled, all gain settings *	-60	dBc
Input impedance	75	Ω
Input VSWR	8	dB
Output impedance differential, all loops (requires external load for example as in Figure 11)	440	Ω
Input to output isolation (both outputs)	30	dB
Output to output isolation	25	dB

Table 1 - Reference Data

*132 channel matrix at +15 dBmV per channel, 75 Ω source impedance

2.0 Functional Description

The SL2150D is a broadband wide dynamic range dual output tuner front end LNA with AGC. It also has application is any system where a wide dynamic range broadband power splitter is required.

The pin assignment is contained in Figure 2 and the block diagram in Figure 1.The port internal peripheral circuits are contained in Figure 14.

In normal application the RF input is interfaced to the device input. The input preamplifier is designed for low noise figure, within the operating region of 50 to 860 MHz and for high intermodulation distortion intercept so offering good signal to noise plus composite distortion spurious performance when loaded with a multi carrier system. The preamplifier also provides an impedance match to a 75 Ω source; the typical impedance is shown in Figure 4.

The input NF is shown in Figure 6.

The output of the preamplifier is then power split to two independently controlled AGC stages. Each AGC stage provides for a minimum of 30 dB of gain control across the input frequency range. The typical AGC characteristic and NF versus gain setting are contained in Figure 5 and Figure 7 respectively.

Finally each of the AGC stages drive an output buffer of differential output impedance of 440 Ω, which provides a nominal 11 dB of conversion gain when terminated into a differential 75 Ω load, as in Figure 11. Each channel AGC and output buffer can be independently powered down.

In application it is important to avoid saturation of the output stage, therefore it is recommended that the output standing current be sunk to Vcc through an inductor. A resistive pull up can also be used as shown in Figure 13 - "Example Application Driving 100 Ω Load with Resistive Pull Up", however the resistor values should not exceed 20 ohm single ended.

If an inductive current sink is used the maximum available gain from the device is circa 26 dB. This gain can be reduced by application of an external load between the differential output ports. The gain can be approximately calculated from the following formula:

- GAIN = 20*log ((Parallel combination of 440 ohm and external load between ports)/22 ohm)+2dB

For example when driving a 100 ohm load as in Figure 12, the gain equals

- GAIN = 20 *log ((440 *100)/(440+100)/22)+2dB =12dB.

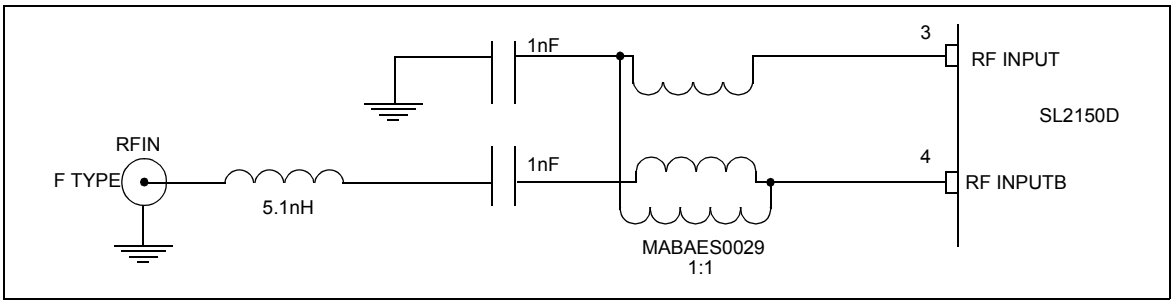


Figure 3 - Input Network

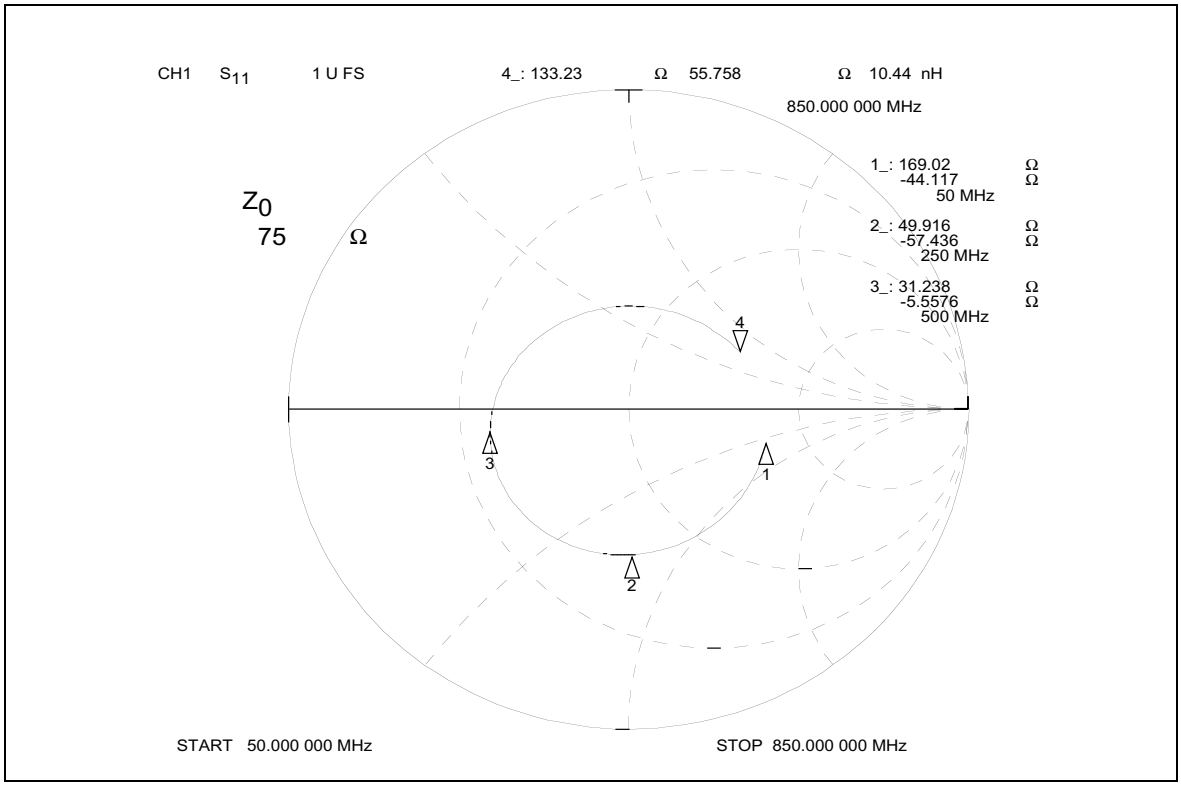


Figure 4 - Typical single-end input impedance

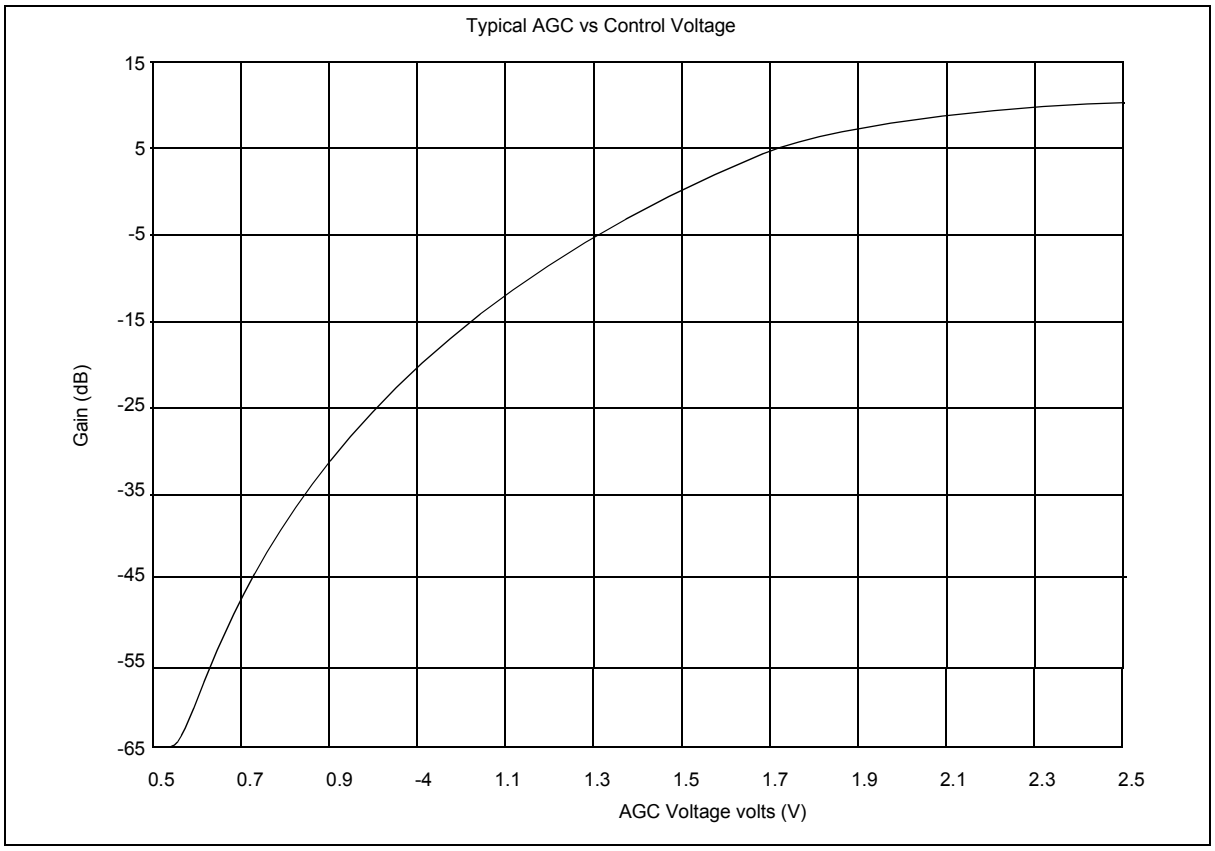


Figure 5 - Typical AGC versus Control Voltage Characteristic

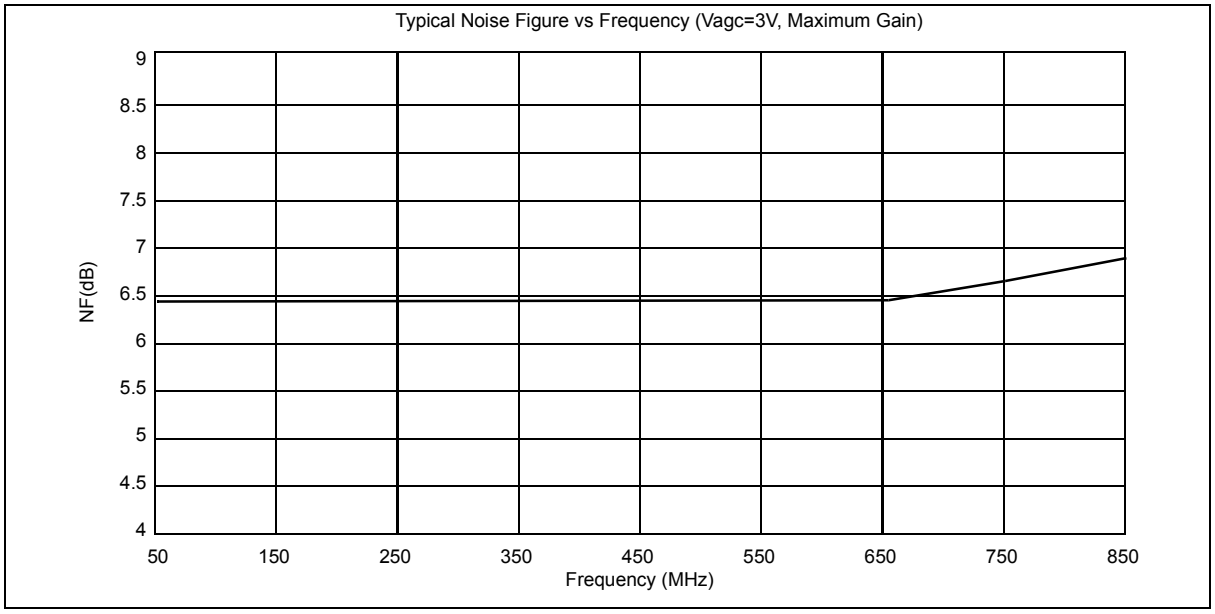


Figure 6 - Input Noise Figure at 25°C

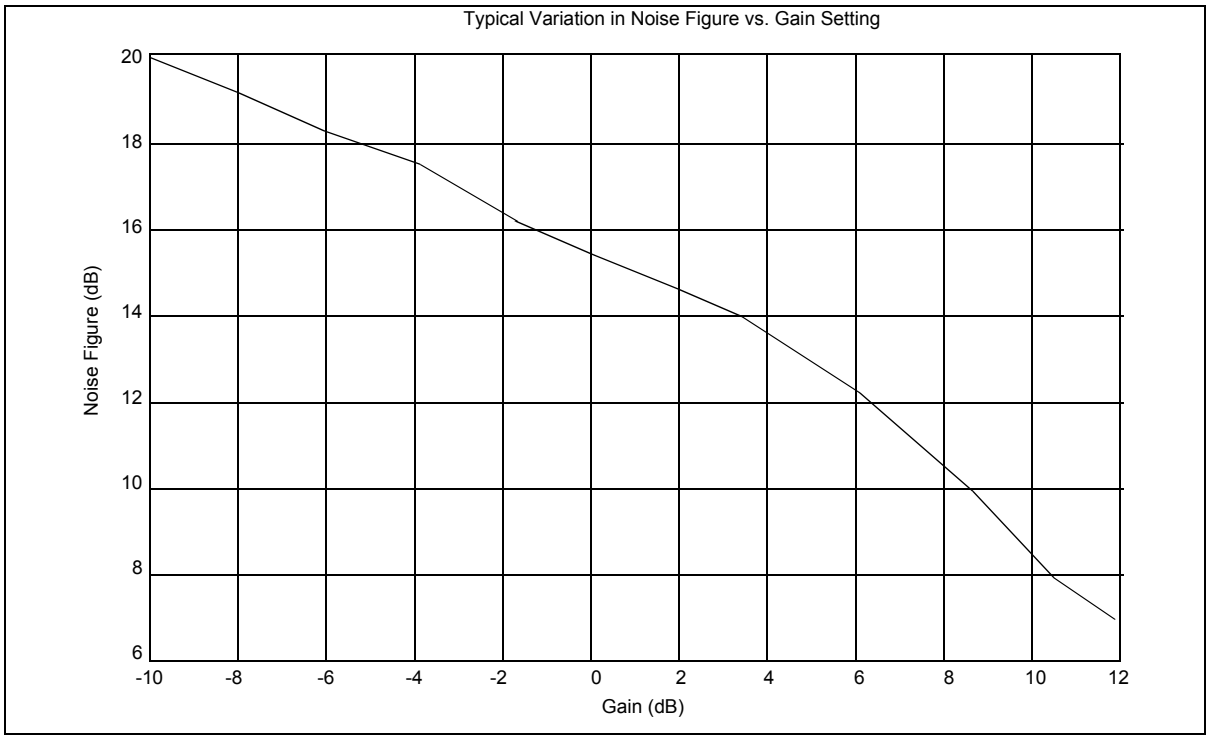


Figure 7 - Typical Variation in NF versus Gain Setting

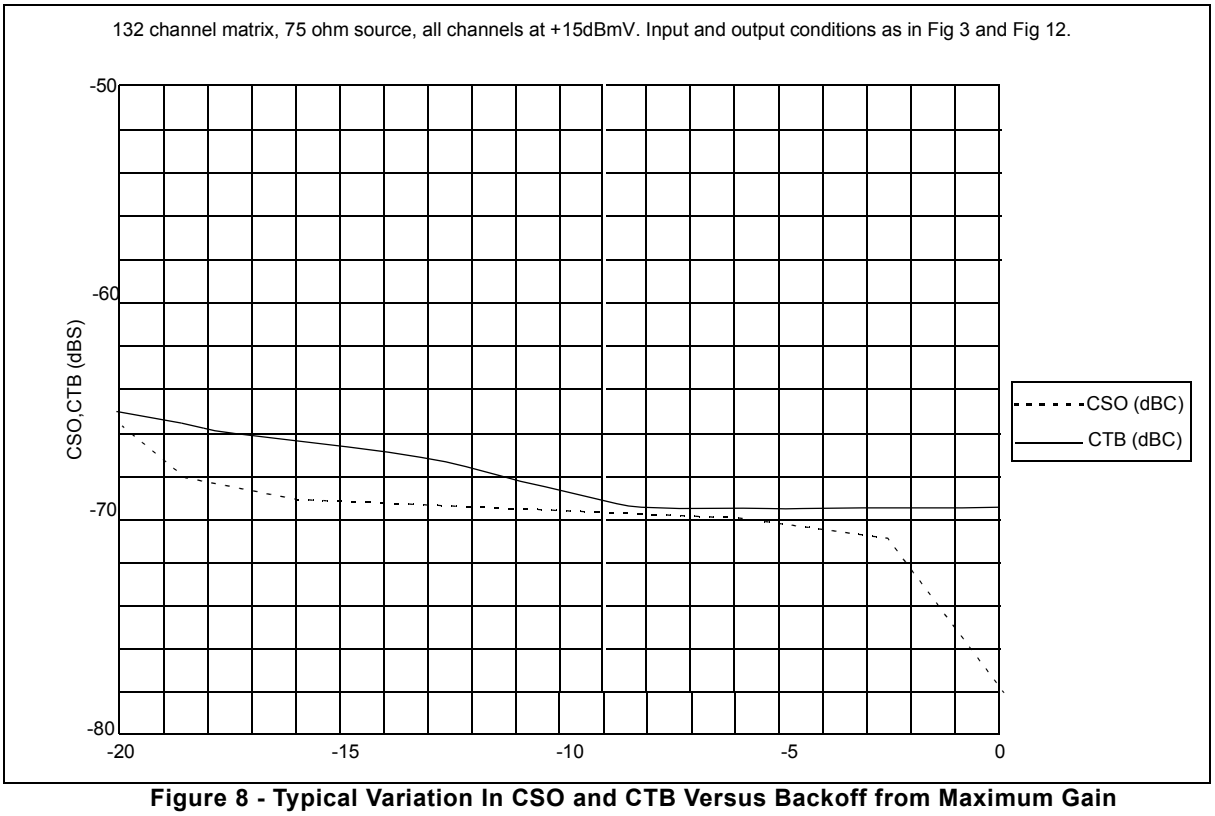


Figure 8 - Typical Variation In CSO and CTB Versus Backoff from Maximum Gain

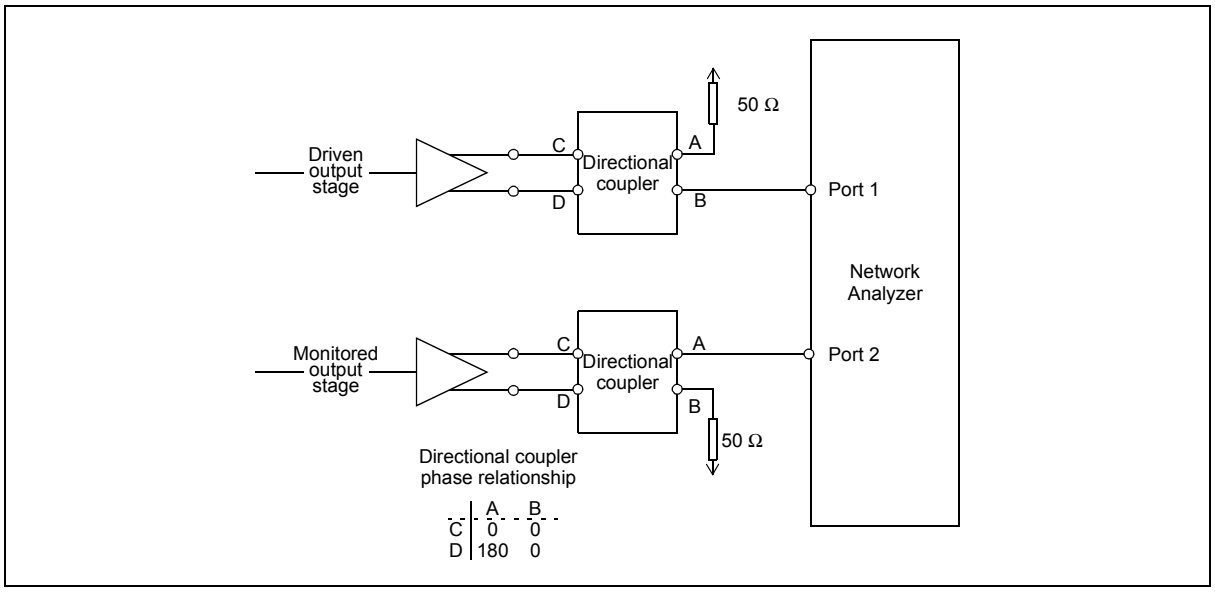


Figure 9 - Test Condition for Output Crosstalk

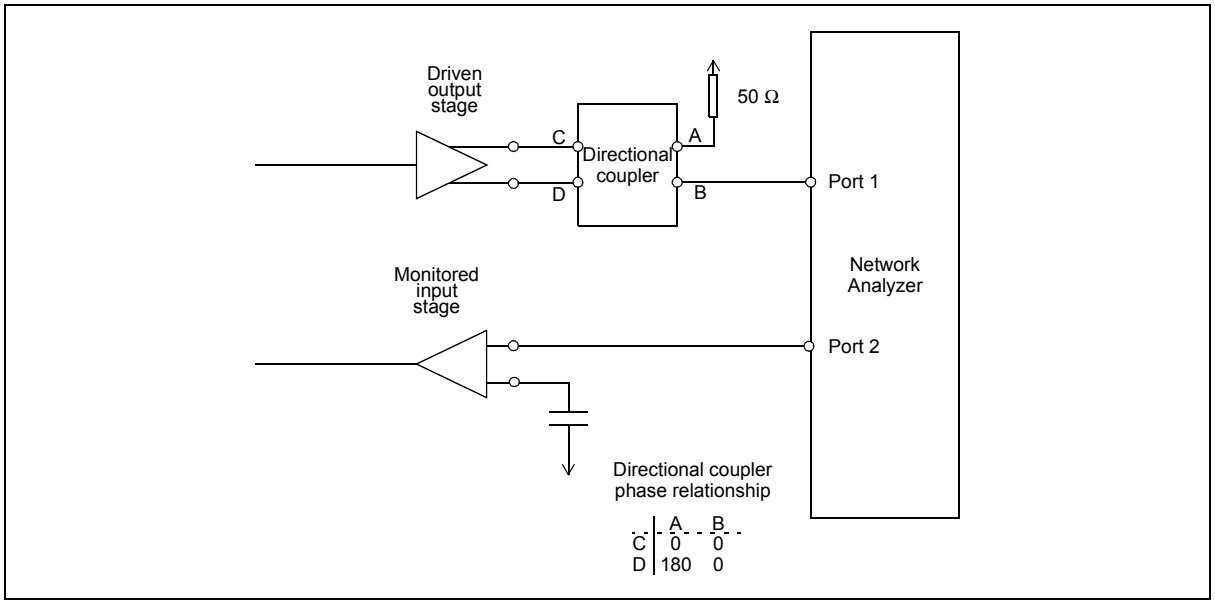


Figure 10 - Test Condition for Output to Input Crosstalk

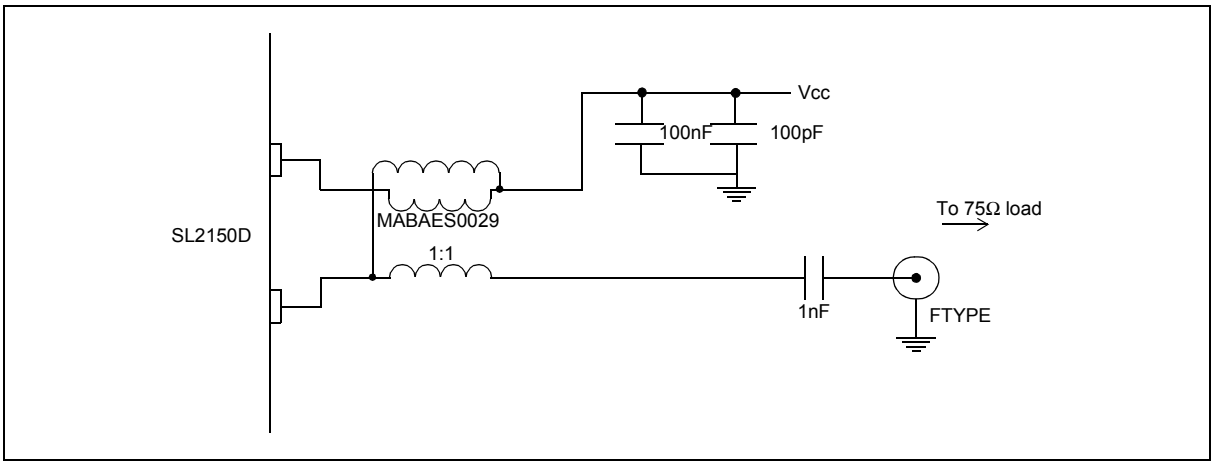


Figure 11 - Example Application Driving 75Ω load

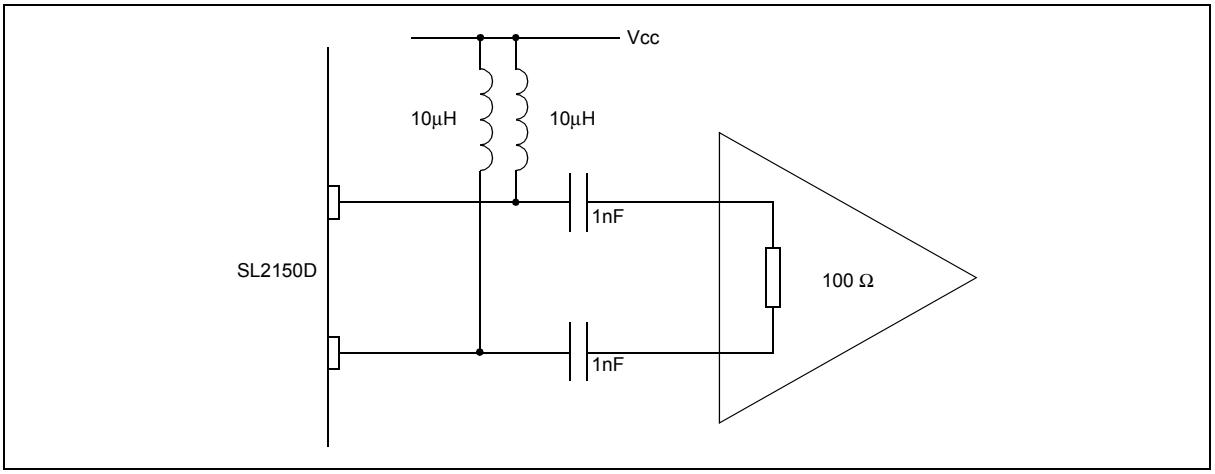


Figure 12 - Example Application Driving 100Ω Load with Inductive Pull up

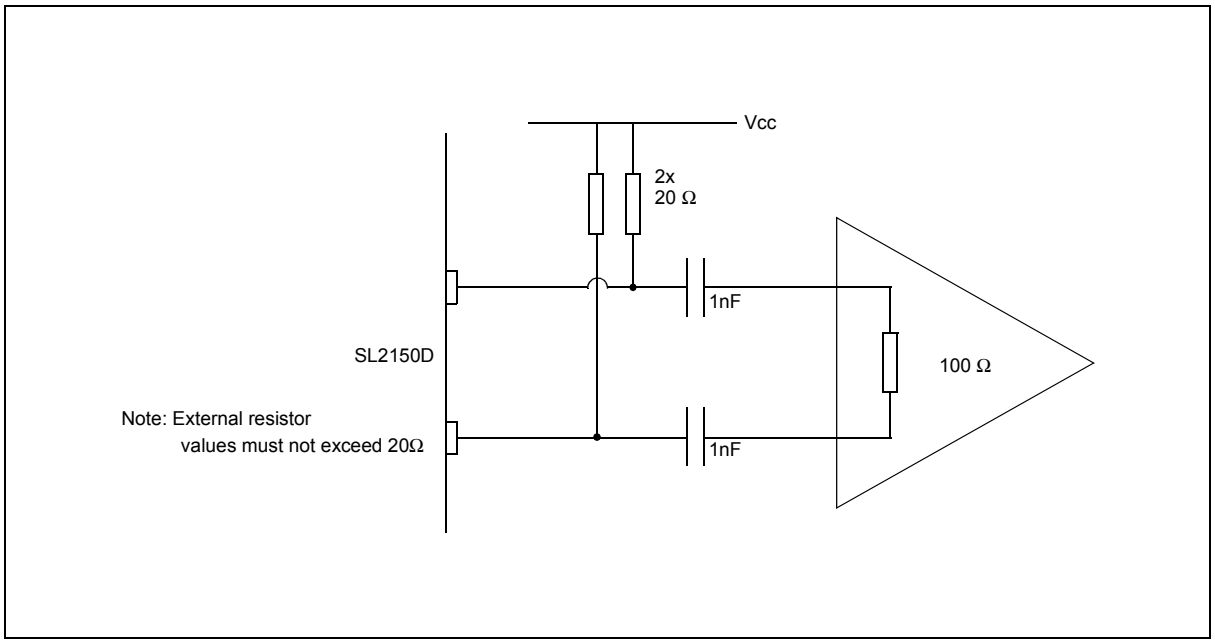


Figure 13 - Example Application Driving 100 Ω Load with Resistive Pull Up

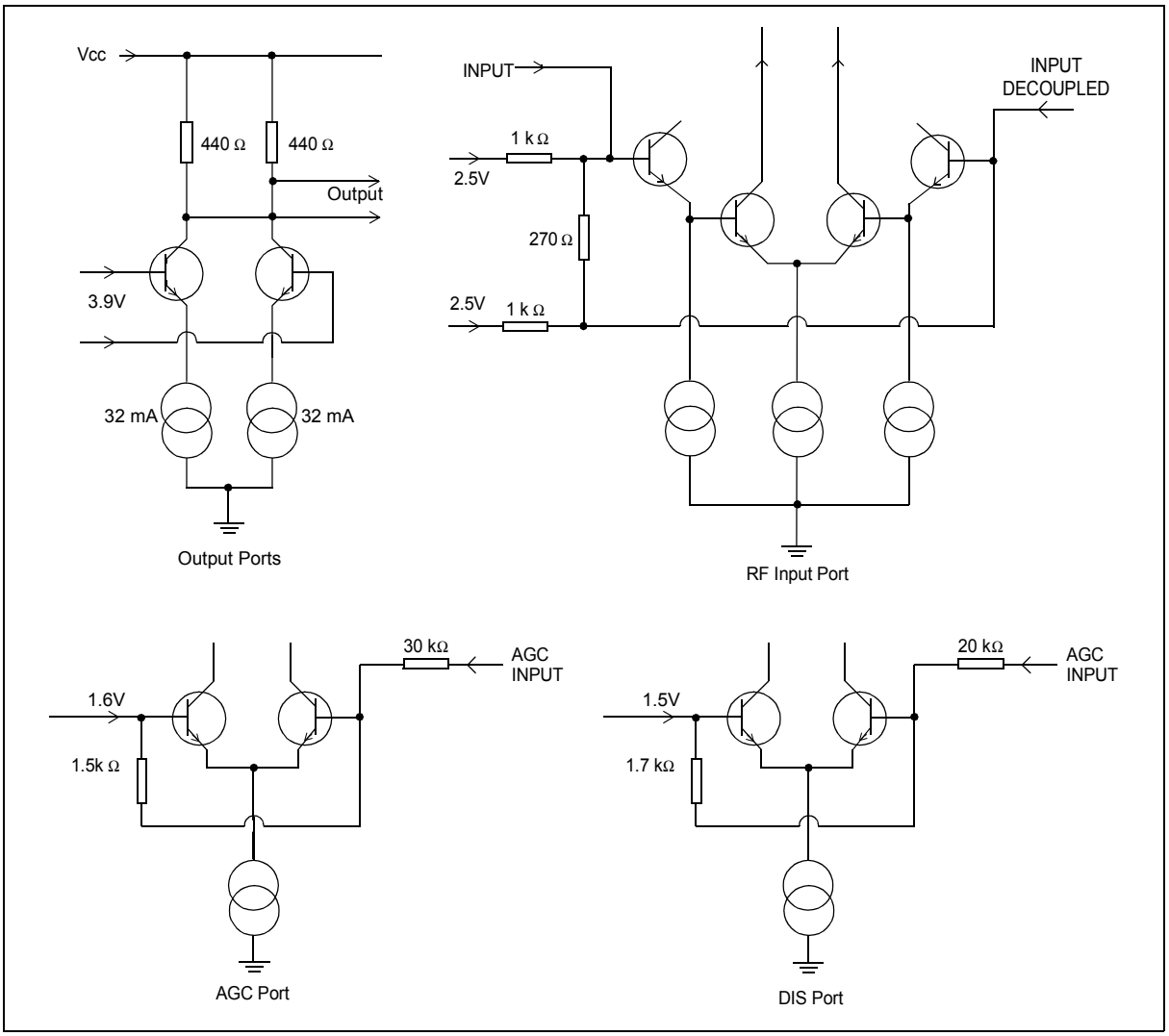


Figure 14 - Port Peripheral Circuitry

3.0 Electrical Characteristics

Test conditions (unless otherwise stated).

T_{amb} =-20^{o} to 85^{o} C, Vee=0V, Vcc=5V+-5%

These characteristics are guaranteed by either production test or design.

They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Electrical Characteristics

Characteristic	pin	min	typ	max	units	Conditions
Supply current			190 110 42	220 140 60	mA mA mA	Both outputs enabled One output enabled Both outputs disabled
Input frequency range		50		860	MHz	
Input impedance	3, 4		75		Ω	See Figure 4
Input return loss		6.8	8		dB	See Figure 4
Input Noise Figure			6.4	7.2	dB	Tamb=27^{0}C, see Figure 6 All loops at maximum conversion gain
Variation in NF with gain adjust				-1	dB/dB	See Figure 7
Gain maximum minimum minimum		9.5	11 -50	12.5 -25	dB dB dB	Power gain from 75 Ω single ended source to differential 75 Ω load, with application as in Figure 11. Vagcip=3.0V Vagcip=0.5V Vagcip=Vee AGC monotonic from Vee to Vcc. Refer to Functional description section for information on calculating maximum gain with other load conditions
CSO				-66 -62	dBc dBc	See note (2) See note (3)
CTB				-65 -62	dBc dBc	See note (2) See note (3)
CXM				-60	dBc	See note (2)

Electrical Characteristics (continued)

Characteristic	pin	min	typ	max	units	Conditions
Input P1dB			+4.5		dBm	All gain settings, with load as in Figure 11
Gain variation within channel				0.25	dB	Channel bandwidth 8 MHz within operating frequency range, all loops, all gain settings
Output impedance	11,12, 24,25		440		Ω	Differential
Output port DC standing current	11,12, 24,25			50	mA	Standing current that any external load has to sustain.
AGC1, 2 input leakage current	8,9	-200		200	µA	Vagcip =Vee to Vcc
DIS1, 2 input Input high voltage Input low voltage Leakage current	6, 7	 2.8 Vee -200		 Vcc 0.8 200	 V V µA	 Output disabled Output enabled DIS1, 2 = Vee to Vcc
Crosstalk between outputs				-25	dB	All gain settings, measured differential output to differential output, driven ports in phase and monitored ports out of phase, see Figure 9
Crosstalk between outputs and RF input				-30	dB	All gain settings, measured differential output to single ended input, driven ports in phase, see Figure 10

Note 1: All power levels are referred to 75Ω,and 0 dBm =109 dBµV.
Note 2: Load as in Figure 11 & Figure 12, at maximum gain, 132 channel matrix, 75 ohm source with all channels at +15 dBmV, assuming power match.
Note 3: Load as in Figure 11 & Figure 12, all gain settings, 132 channel matrix, 75 ohm source with all channels at +15 dBmV, assuming power match.

Absolute Maximum Ratings All voltages are referred to Vee at 0V

Characteristic	min	max	units	conditions
Supply voltage	-0.3	6	V	
RF input voltage		8	dBm	Differential
All I/O port DC offsets	-0.3	Vcc+0.3	V	
Storage temperature	-55	150	^{o}C	
Junction temperature		125	^{o}C	Power applied
Package thermal resistance, chip to ambient		35	^{o}C/W	Paddle to be soldered to ground plane
Power consumption at 5.25V		1155	mW	
ESD protection	1.5		kV	Mil-std 883B method 3015 cat1

4.0 SL2150D Demonstration Board

The SL2150D demonstration board is designed to allow testing of device functionality as a stand alone power splitter. It allows for testing of the AGC function and independent testing of all channels.

The SL2150D is designed to interface differentially into a silicon tuner such as the SL2101 with simple inductive or resistive pull-ups. However to facilitate testing the differential output is converted to a single ended signal through a balun, the differential conversion is necessary for achieving second order performance.

All outputs require a DC return path to Vcc to prevent output saturation. This can be provided by the balun, inductive pull up or resistive pull up. In the case of a resistive pull up the maximum load value is 20Ω.

The balun also provides the DC bias to the outputs; all outputs have to be DC 'shorted' to Vcc to prevent saturation of the output stages.

All input and output terminations are 75Ω.

The board schematic and board layouts are contained in Figure 15 and Figures 16-19 respectively.

Operation note

The supply voltage must be connected and enabled before any AGC or disable voltage is applied unless these supplies currents are limited to <1 mA or else permanent damage may occur through the ESD structures on the device.

4.1 Pin Connections

All references are with the board oriented as in bottom view on figure (2).

Pin 1 of the header is defined as the left-hand pin.

4.1.1 Power supply

A single 5V supply is required.

Power is supplied through the two-pin header PL1, located top right hand corner.

Pin	Function
1	Vcc
2	Vee

4.1.2 RF input

The RF input F type, SK1, is located on the right hand side of the board.

4.1.3 RF outputs

Output 1 is the F type connector, SK2, located at the top of the board.

Output 2 is the F type connector, SK5, located at the bottom of the board

4.1.4 AGC & Disable control

AGC & Disable controls are connected through the 5-pin header, PL2, located in the bottom right hand corner. See note on connection of supplies in power supply section. Pin allocation is as follows:

Pin	Function
1	Disable 1
2	Disable 2
3	Vagc 1
4	Vagc 2
5	Vee

AGC control voltage is Vee to 3V for minimum to maximum gain setting. Disable control voltage is 0V for enable, 3V for disable.

4.2 Test Procedure

4.2.1 CSO

CSO is tested using an RDL matrix generator set to deliver all channels from 55.25 MHz to 859.25 MHz at 15 dBmV per carrier.

Each output is tested independently over maximum gain setting through 15 dB of gain reduction.

The output intermodulation is monitored on a spectrum analyzer with video bandwidth of 1 kHz and resolution bandwidth of 10 kHz. To avoid intermodulation in the test set up the output channel is filtered through a narrow band filter and then amplified to compensate for insertion loss. The higher of all CSO beats is recorded.

Under gain reduction the amplitude is normalized to channel 2 output at the required AGC onset

4.2.2 CTB

CTB is tested using an RDL matrix generator set to deliver all channels from 55.25 MHz to 859.25 MHz at 15 dBmV per carrier.

Each output is tested independently over maximum gain setting through 15 dB of gain reduction.

The output intermodulation is monitored on a spectrum analyzer with video bandwidth of 1 kHz and resolution bandwidth of 10 kHz. To minimize intermodulation in the test set up the output channel is filtered through a narrow band filter and then amplified to compensate for insertion loss.

CTB is measured with N+-1 also disabled since these channels were found to produce intermodulation in the filter and the post amplifier.

Under gain reduction the amplitude is normalized to channel 2 output at the required AGC onset.

4.2.3 CXM

CTB is tested using an RDL matrix generator set to deliver all channels from 55.25 MHz to 859.25 MHz at 15 dBmV per carrier with 100% modulation at line rate.

Each output is tested independently over maximum gain setting through 15 dB of gain reduction.

To minimize cross modulation in the test set up the output channel is filtered through a narrow band filter and then amplified to compensate for insertion loss. The amplifier output is then demodulated on a first spectrum analyzer set to linear mode with maximum resolution and video bandwidth. The video out of the first spectrum analyzer, which will be the demodulated AM on the carrier, is connected to a second spectrum analyzer centred on line rate frequency with video averaging enabled. The cross modulation can then be monitored on the second spectrum

analyzer.

The CXM is measured with modulation disabled on N+-1 since these channels were found to produce cross modulation in the filter and the post amplifier.

Under gain reduction the amplitude is normalized to channel 2 output at the required AGC onset.

4.2.4 Gain

Gain is measured using a network analyzer with 50/75Ω pads to ensure correct source and load impedance.

4.2.5 AGC

Output amplitude at a given channel is measured on a spectrum analyzer with all AGC settings from 0V to Vcc.

4.2.6 S11

S11 is measured at the test board RF input F type connector, using a network analyzer calibrated to 75Ω F type connector.

4.2.7 S22

S22 is not measured since the device is not designed to be impedance matched on its output. Rather the output load is used as the terminating impedance for the device.

4.2.8 NF

NF is measured using a NF meter with a 50/75Ω pad on the input.

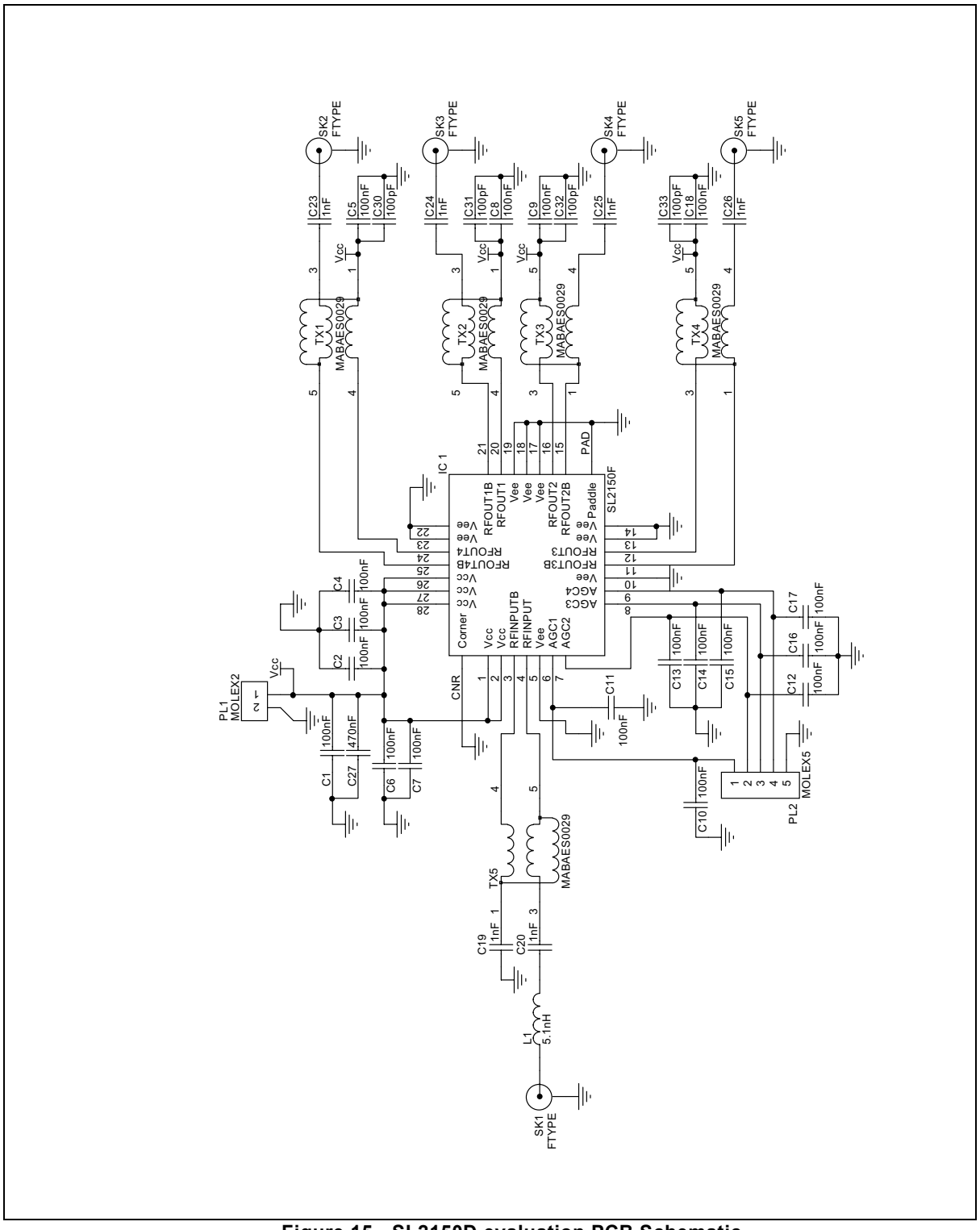


Figure 15 - SL2150D evaluation PCB Schematic

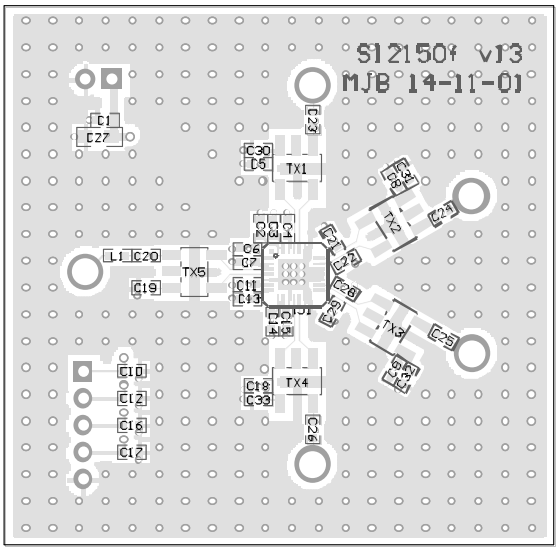


Figure 16 - SL2150D evaluation PCB (Top View)

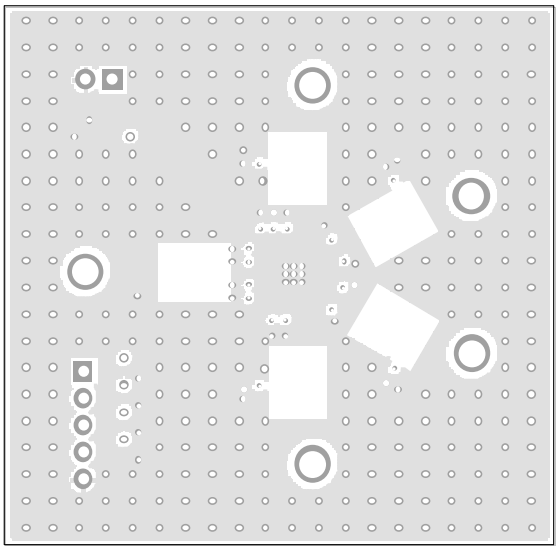


Figure 17 - SL2150D evaluation PCB (Layer 2 view)

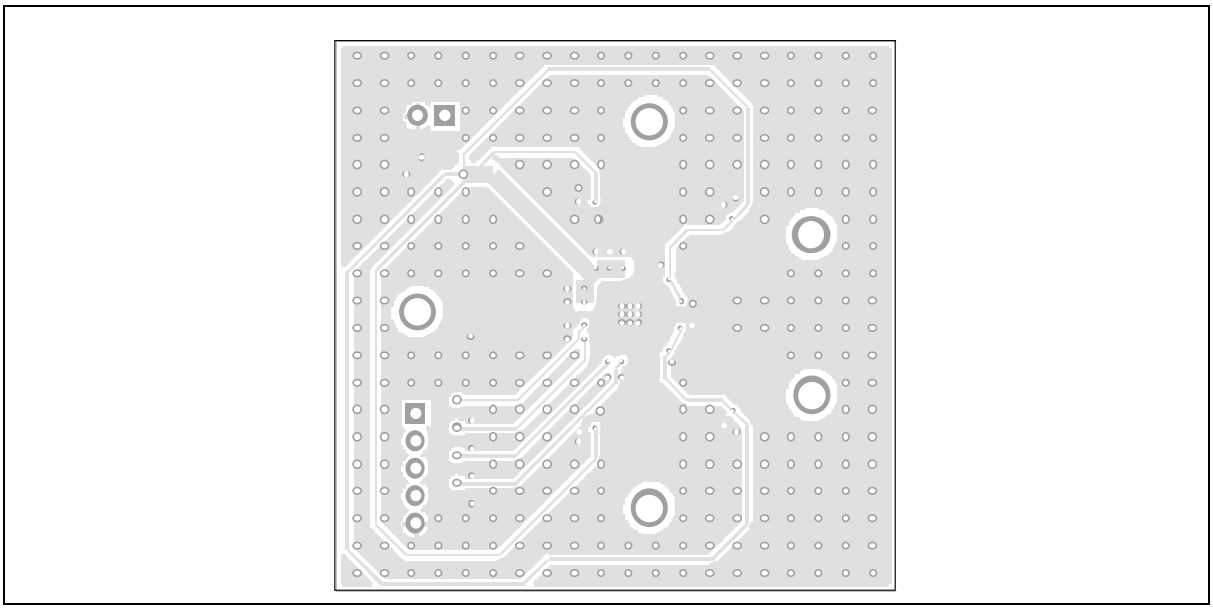


Figure 18 - SL2150D evaluation PCB (Layer 3 view)

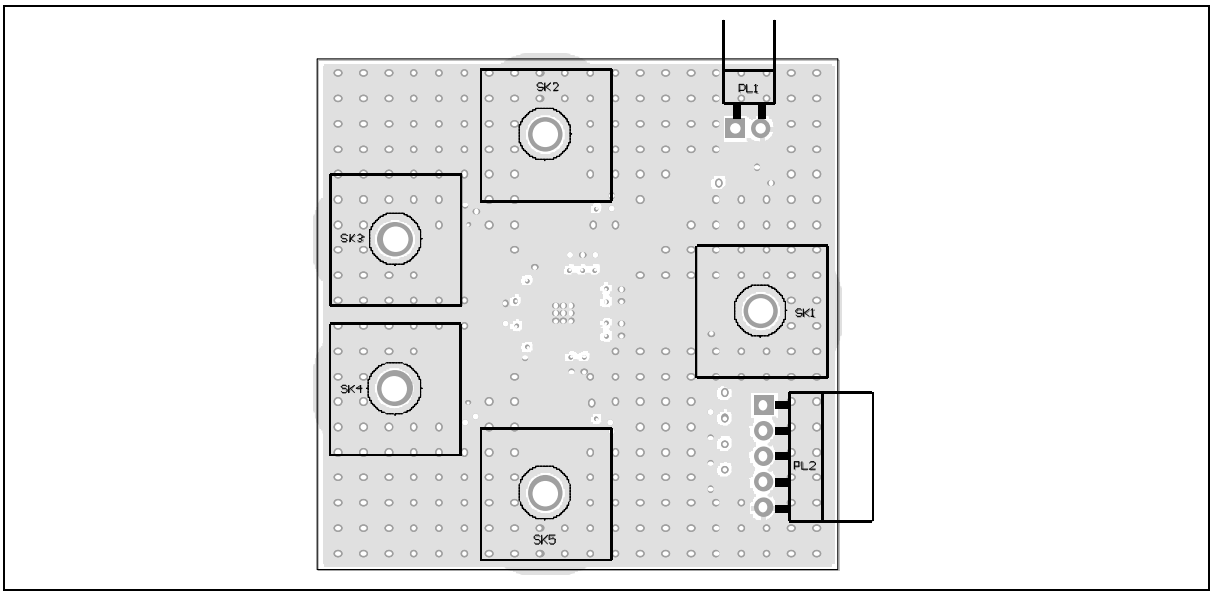
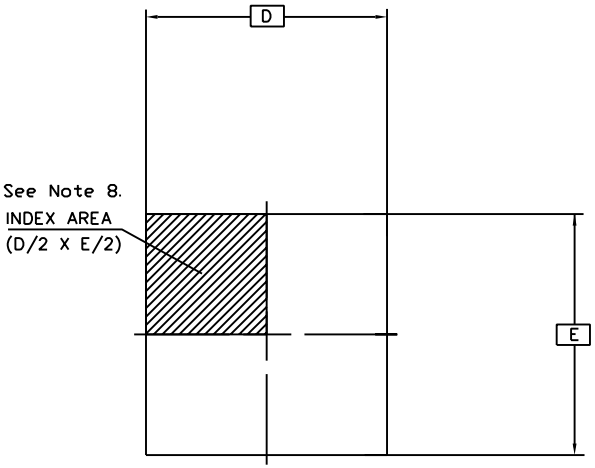
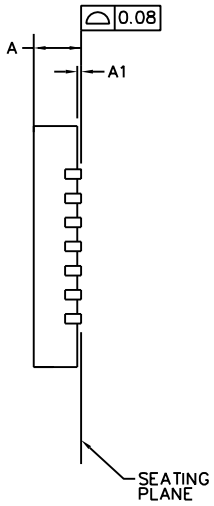
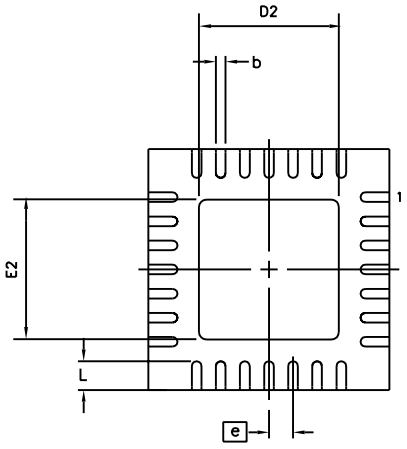


Figure 19 - SL2150D evaluation PCB (Bottom View Mirrored)



TOP VIEW





BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS	
	MIN.	MAX.
A	–	1.00
A1	0.00	0.05
b	0.18	0.30
D	5.00 BSC	
D2	3.00	3.25
E	5.00 BSC	
E2	3.00	3.25
N	28	
Nd	7	
Ne	7	
e	0.50 BSC	
L	0.35	0.75

Conforms to JEDEC MO-220 VHHD-1 iss A

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 28 .
6. PACKAGE WARPAGE MAX 0.08mm.
7. NOT TO SCALE.
8. TERMINAL #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED AND MAY BE EITHER A MOULD OR MARKED FEATURE.

ISSUE	1	2	3	
ACN	209757	212494	212973	
DATE	26Oct00	8Apr02	21Jun02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

LH

Package Code LC

Package Outline for 28 lead MLP (5 x 5mm)

GPD00747

For more information about all Zarlink products visit our Web Site at

www.zarlink.com