

**MCM67H618A**

*Product Preview*  
**64K x 18 Bit BurstRAM™**  
**Synchronous Fast Static RAM**  
**With Burst Counter and Self-Timed Write**

The MCM67H618A is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high-performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ( $\bar{G}$ ) are clock (K) controlled through positive-edge-triggered noninverting registers.

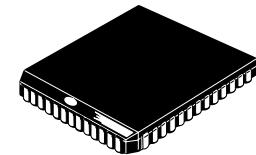
Bursts can be initiated with either address status processor ( $\overline{ADSP}$ ) or address status cache controller ( $\overline{ADSC}$ ) input pins. Subsequent burst addresses can be generated internally by the MCM67H618A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ( $\overline{ADV}$ ) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ( $\overline{LW}$  and  $\overline{UW}$ ) are provided to allow individually writeable bytes.  $\overline{LW}$  controls DQ0 – DQ8 (the lower bits), while  $\overline{UW}$  controls DQ9 – DQ17 (the upper bits).

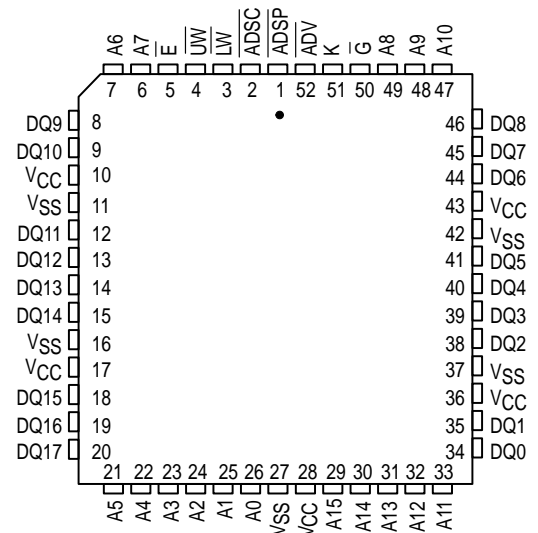
This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$ ,  $\overline{ADSC}$ , and  $\overline{ADV}$  Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package
- $\overline{ADSP}$  Disabled with Chip Enable ( $\bar{E}$ ) – Supports Address Pipelining



**FN PACKAGE  
PLASTIC  
CASE 778-02**

**PIN ASSIGNMENT**



**PIN NAMES**

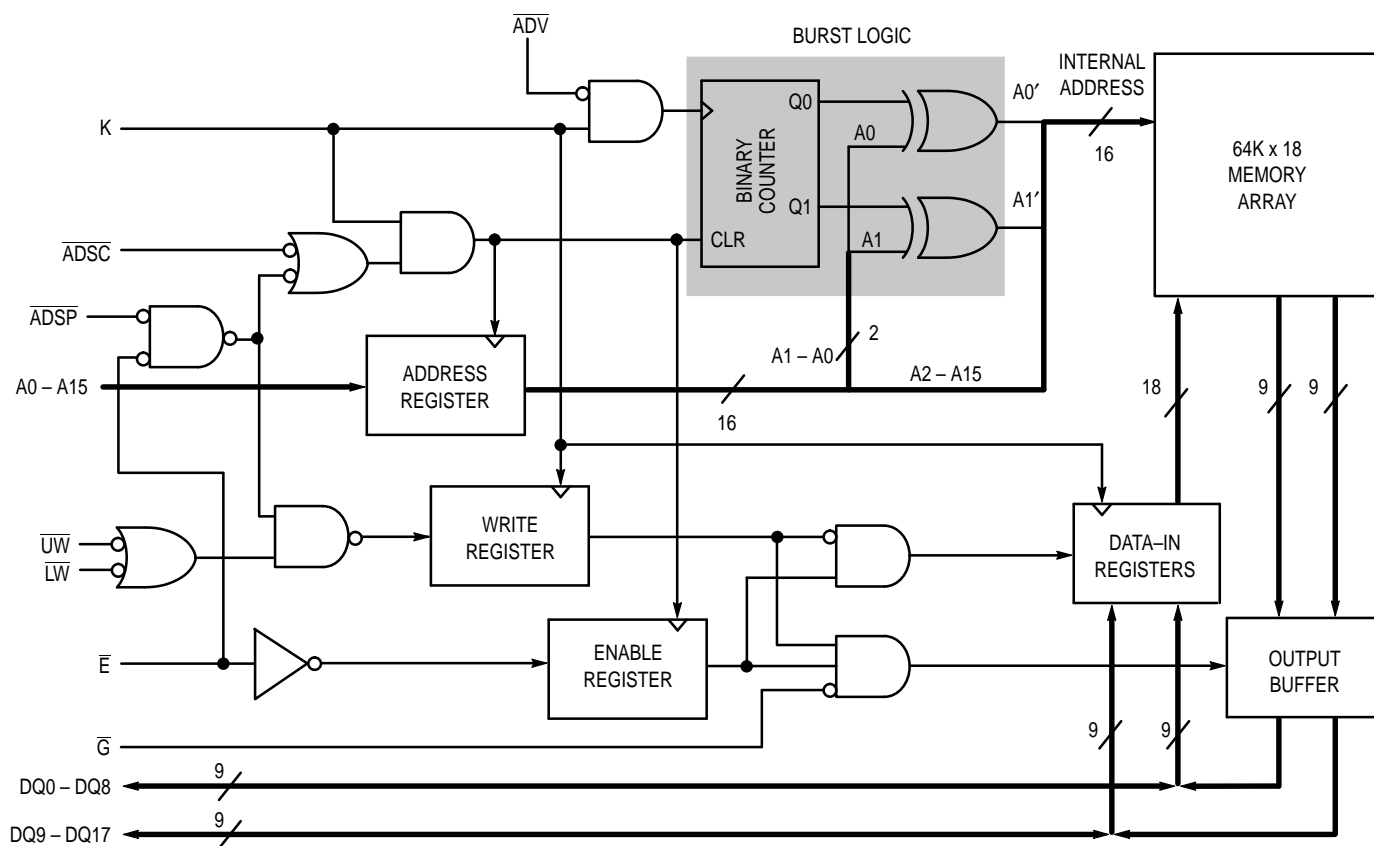
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

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**BLOCK DIAGRAM** (See Note)



NOTE: All registers are positive-edge triggered. The  $\overline{ADSC}$  or  $\overline{ADSP}$  signals control the duration of the burst and the start of the next burst. When  $\overline{ADSP}$  and  $\overline{E}$  are sampled low, any ongoing burst is interrupted and a read (independent of  $\overline{W}$  and  $\overline{ADSC}$ ) is performed using the new external address. Alternatively, an  $\overline{ADSP}$ -initiated two cycle WRITE can be performed by asserting  $\overline{ADSP}$ ,  $\overline{E}$ , and a valid address on the first cycle, then negating both  $\overline{ADSP}$  and  $\overline{ADSC}$  and asserting  $\overline{LW}$  and/or  $\overline{UW}$  with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram). Note that when  $\overline{E}$  and  $\overline{ADSC}$  are high,  $\overline{ADSP}$  is ignored – the external address is not registered in this case. When  $\overline{ADSC}$  is sampled low (and  $\overline{ADSP}$  is sampled high), any ongoing burst is interrupted and a read or write (dependent on  $\overline{W}$ ) is performed using the new external address. Chip enable ( $\overline{E}$ ) is sampled only when a new base address is loaded. After the first cycle of the burst,  $\overline{ADV}$  controls subsequent burst cycles. When  $\overline{ADV}$  is sampled low, the internal address is advanced prior to the operation. When  $\overline{ADV}$  is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ( $\overline{LW}$ ,  $\overline{UW}$ ).

**BURST SEQUENCE TABLE** (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

**SYNCHRONOUS TRUTH TABLE** (See Notes 1, 2, and 3)

$\bar{E}$	ADSP	ADSC	$\bar{ADV}$	UW or LW	K	Address Used	Operation
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:

1. X means Don't Care.
2. All inputs except  $\bar{G}$  must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

**ASYNCHRONOUS TRUTH TABLE** (See Notes 1 and 2)

Operation	$\bar{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:

1. X means Don't Care.
2. For a write operation following a read operation,  $\bar{G}$  must be high before the input data required setup time and held high through the input data hold time.

**ABSOLUTE MAXIMUM RATINGS** (Voltages Referenced to  $V_{SS} = 0$  V)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	- 0.5 to + 7.0	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$	$V_{in}, V_{out}$	- 0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	$I_{out}$	$\pm 30$	mA
Power Dissipation	$P_D$	1.6	W
Temperature Under Bias	$T_{bias}$	- 10 to + 85	°C
Operating Temperature	$T_A$	0 to +70	°C
Storage Temperature	$T_{stg}$	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.75	5.25	V
Input High Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	$V_{IL}$	-0.5*	0.8	V

\*  $V_{IL} \text{ (min)} = -0.5 \text{ V dc}$ ;  $V_{IL} \text{ (min)} = -2.0 \text{ V ac}$  (pulse width  $\leq 20.0 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .

\*\*  $V_{IH} \text{ (max)} = V_{CC} + 0.3 \text{ V dc}$ ;  $V_{IH} \text{ (max)} = V_{CC} + 2.0 \text{ V ac}$  (pulse width  $\leq 20.0 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .

### DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0 \text{ to } V_{CC}$ )	$I_{lkg(I)}$	—	$\pm 1.0$	$\mu\text{A}$
Output Leakage Current ( $\bar{G} = V_{IH}$ )	$I_{lkg(O)}$	—	$\pm 1.0$	$\mu\text{A}$
AC Supply Current ( $\bar{G} = V_{IH}$ , $\bar{E} = V_{IL}$ , $I_{out} = 0 \text{ mA}$ , All Inputs = $V_{IL}$ or $V_{IH}$ , $V_{IL} = 0.0 \text{ V}$ and $V_{IH} \geq 3.0 \text{ V}$ , Cycle Time $\geq t_{KHKH} \text{ min}$ )	$I_{CCA9}$ $I_{CCA10}$ $I_{CCA12}$	—	275 265 250	mA
AC Standby Current ( $\bar{E} = V_{IH}$ , $I_{out} = 0 \text{ mA}$ , All Inputs = $V_{IL}$ and $V_{IH}$ , $V_{IL} = 0.0 \text{ V}$ and $V_{IH} \geq 3.0 \text{ V}$ , Cycle Time $\geq t_{KHKH} \text{ min}$ )	$I_{SB1}$	—	95	mA
Output Low Voltage ( $I_{OL} = +8.0 \text{ mA}$ )	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = -4.0 \text{ mA}$ )	$V_{OH}$	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

### CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	$C_{in}$	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $T_A = 0\text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V  
 Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V  
 Output Load ..... See Figure 1A Unless Otherwise Noted

### READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67H618A-9		MCM67H618A-10		MCM67H618A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	$t_{KHKH}$	15	—	16.6	—	20	—	ns	
Clock Access Time	$t_{KHQV}$	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	$t_{GLQV}$	—	5	—	5	—	6	ns	
Clock High to Output Active	$t_{KHQX1}$	6	—	6	—	6	—	ns	
Clock High to Output Change	$t_{KHQX2}$	3	—	3	—	3	—	ns	
Output Enable to Output Active	$t_{GLQX}$	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	$t_{GHQZ}$	—	6	—	7	—	7	ns	6
Clock High to Q High-Z	$t_{KHQZ}$	3	6	3	7	3	7	ns	
Clock High Pulse Width	$t_{KHKL}$	5	—	5	—	6	—	ns	
Clock Low Pulse Width	$t_{KLKH}$	5	—	5	—	6	—	ns	
Setup Times:									
Address	$t_{AVKH}$	2.5	—	2.5	—	2.5	—	ns	7
Address Status	$t_{ADSVKH}$								
Data In	$t_{DVKH}$								
Write	$t_{WVKH}$								
Address Advance	$t_{ADVVKH}$								
Chip Enable	$t_{EVKH}$								
Hold Times:									
Address	$t_{KHAX}$	0.5	—	0.5	—	0.5	—	ns	7
Address Status	$t_{KHADSX}$								
Data In	$t_{KHDX}$								
Write	$t_{KH WX}$								
Address Advance	$t_{KHADVX}$								
Chip Enable	$t_{KH EX}$								

#### NOTES:

- In setup and hold times, W (write) refers to either one or both byte write enables  $\overline{LW}$  and  $\overline{UW}$ .
- A read cycle is defined by  $\overline{UW}$  and  $\overline{LW}$  high or ADSP low for the setup and hold times. A write cycle is defined by  $\overline{LW}$  or  $\overline{UW}$  low and  $\overline{ADSP}$  high for the setup and hold times.
- All read and write cycle timings are referenced from K or  $\overline{G}$ .
- $\overline{G}$  is a don't care when  $\overline{UW}$  or  $\overline{LW}$  is sampled low.
- Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
- Transition is measured  $\pm 500\text{ mV}$  from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature,  $t_{KHQZ}\text{ max}$  is less than  $t_{KHQX1}\text{ min}$  for a given device and from device to device.
- This is a synchronous device. All addresses must meet the specified setup and hold times for **ALL** rising edges of K whenever  $\overline{ADSP}$  or  $\overline{ADSC}$  is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for **ALL** rising edges of K when the chip is enabled. Chip enable must be asserted at each rising edge of clock for the device (when  $\overline{ADSC}$  is low) to remain enabled.

### AC TEST LOADS

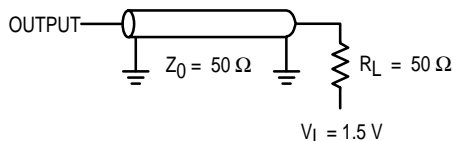


Figure 1A

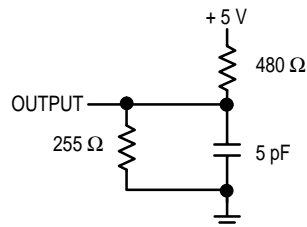
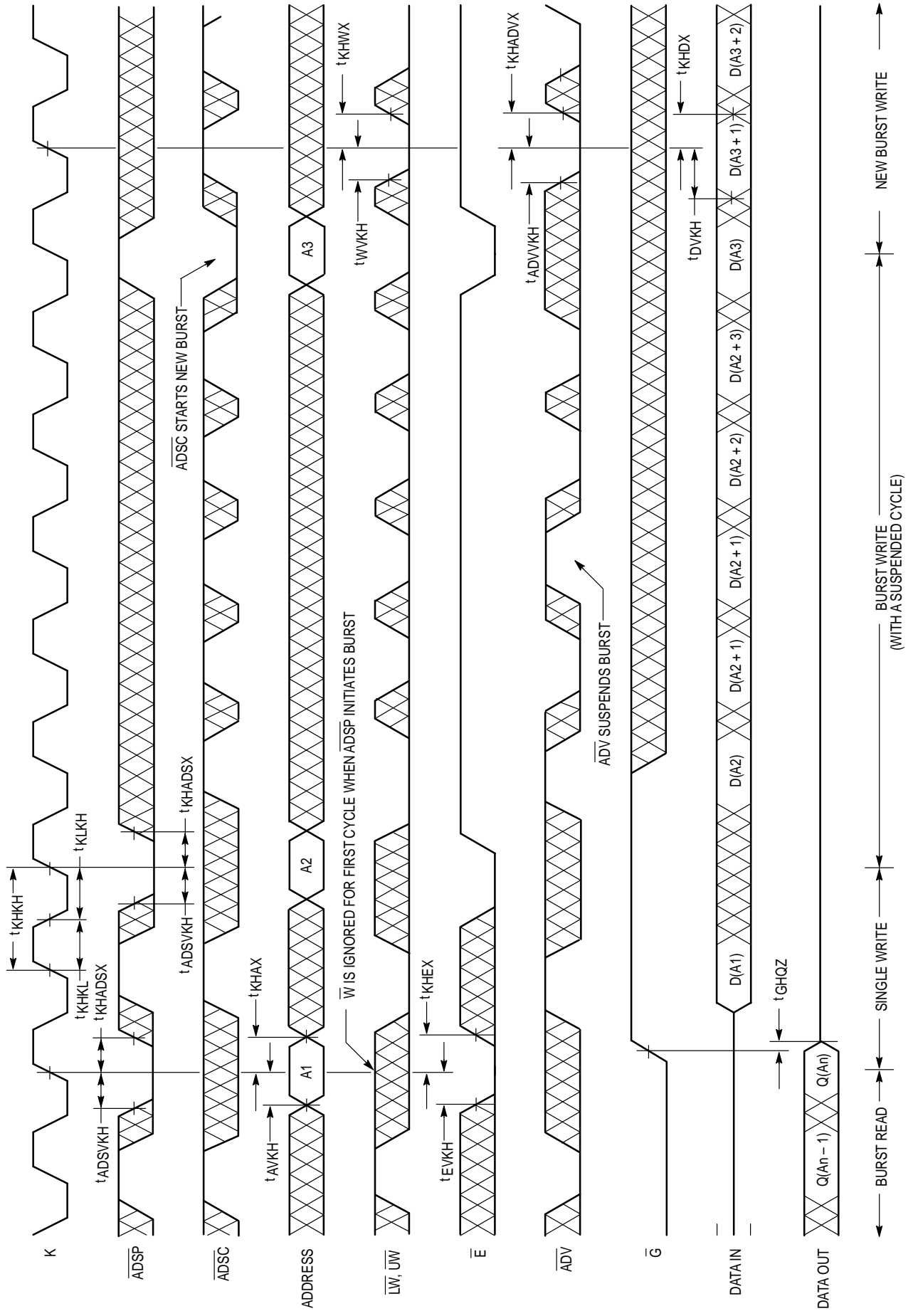


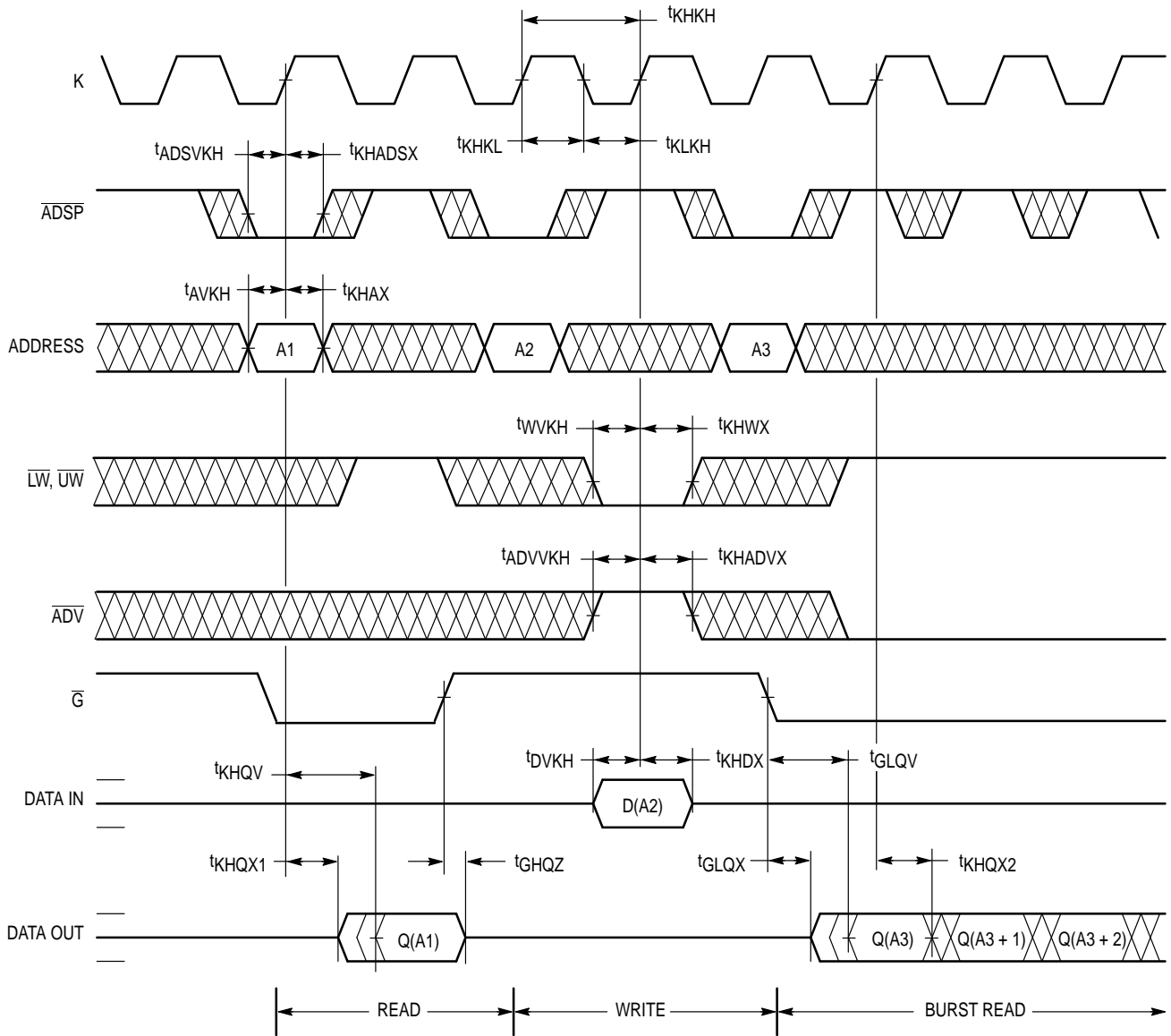
Figure 1B



# WRITE CYCLES

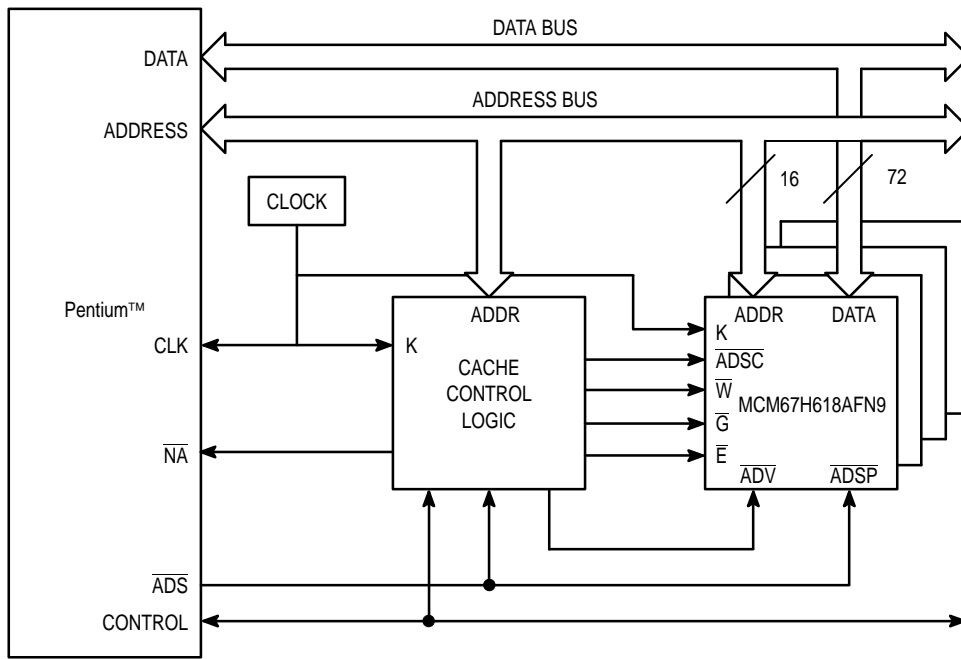


COMBINATION READ/WRITE CYCLE ( $\overline{E}$  low,  $\overline{ADSC}$  high)





### APPLICATION EXAMPLE

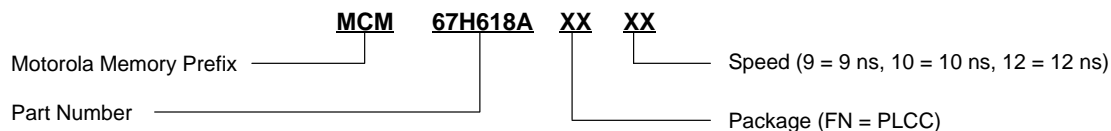


512K Byte Burstable, Secondary Cache  
Using Four MCM67H618AFN9s with a 66 MHz Pentium


**Figure 2**

## ORDERING INFORMATION

(Order by Full Part Number)

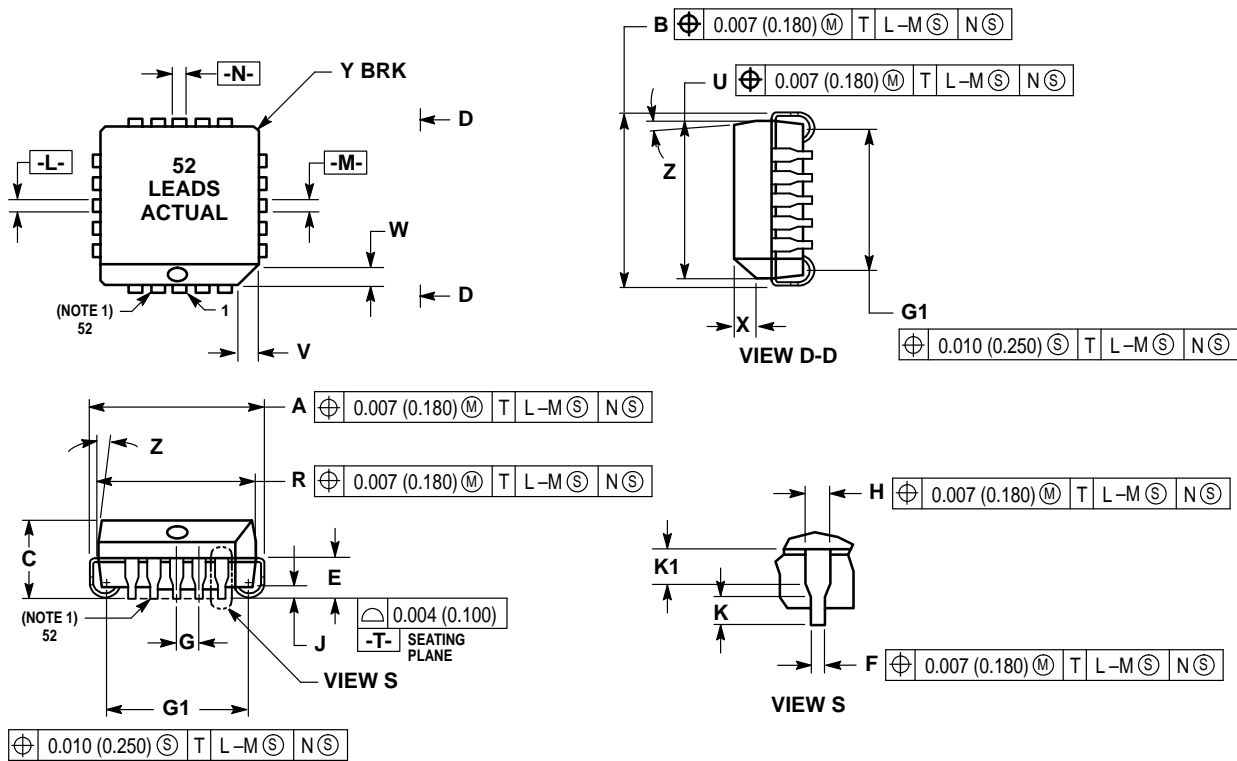


Full Part Numbers — MCM67H618AFN9 MCM67H618AFN10 MCM67H618AFN12

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# PACKAGE DIMENSIONS

## FN PACKAGE 52-LEAD PLCC CASE 778-02



### NOTES:

1. DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

**Literature Distribution Centers:**

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JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

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MCM67H618A/D

