PRELIMINARY DATA SHEET

MAS 3506D
WorldSpace
Broadcast Channel
Audio Decoder

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WorldSpace Broadcast Channel Audio Decoder

1. Introduction

The WorldSpace system is a satellite-based digital radio service for direct-to-home transmission of digital radio programs. The coverage areas of this service are Africa, South America, and parts of Asia.

The MAS 3506D is the source decoder of Micronas' StarMan chip set that is designed for the reception of WorldSpace signals. The MAS 3506D extracts one Service Component (SC) of an incoming digital World-Space Broadcast Channel (BC) and decodes MPEG 1/2/2.5 Layer 3[1)] encoded audio data contained in the selected Service Component. The Service Control Header (SCH) information from the Broadcast Channel is accessible via the embedded fast mode serial control interface. The MAS 3506D provides digital audio data output in I^2S and similar formats. An embedded digital buffer-controlled loop recovers the sampling frequency of the audio signal and generates a synchronized 24.576 MHz clock signal which is used as an oversampling clock for D/A converters. A block diagram of the MAS 3506D is shown in Figure 1–2 on page 5.

[1)] MPEG 2.5 is a compatible extension of MPEG 2 audio, defined in ISO/IEC 13818-3.2 that covers additionally very low sampling frequencies down to 8 kHz.

1.1. Features of the MAS 3506D

– Single-chip WorldSpace Broadcast Channel bit-stream demultiplexer
– ISO MPEG 1/2/2.5 Layer 3 decoder
– ISO MPEG compliance tests passed
– Data processing by a high-performance RISC DSP core (MASC)
– Download feature provides additional functionality
– Self-synchronized operation
– Output audio data delivered (in various formats) via an I^2S bus (SDO)
– Digital volume control and stereo channel mixer
– Automatic soft-mute function
– WorldSpace SCH-data output via I^2C interface
– MPEG ancillary data provided via I^2C interface
– Status information accessible via PIO pins or I^2C
– "CRC Error", "MPEG Frame Synchronization" and "BC-Frame-Synchronization" indicators
– Power management for reduced power consumption at lower sampling frequencies
– Low power dissipation (30 mW at fs ≤ 12 kHz, 46 mW at fs ≤ 24 kHz, 86 mW at fs > 24 kHz at 2.7 V)
– Supply voltage range: 2.7 V to 3.6 V
– Adjustable built-in DC/DC up-converter for one-cell and two-cell battery operation (typically down to V_{bat} = 0.9 V)
– Adjustable power supply supervision
– Power-off function

1.2. System Overview

The Micronas StarMan chip set consists of the channel decoder DRD 3515A and the MPEG Layer 3 audio decoder MAS 3506D. All essential analog and digital building blocks for WorldSpace reception are provided by the chip set. Together with an L-band tuner and an appropriate microcontroller this set creates a complete StarMan radio receiver (Figure 1–1)

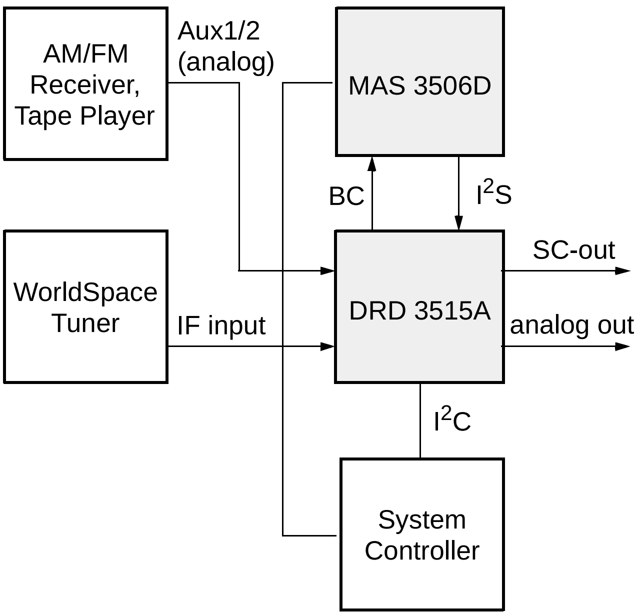

Fig. 1–1: Standard application of the StarMan chip set

Since the DRD 3515A also contains an audio amplifier for headphone or small loudspeaker operation, only a minimum of external components is necessary. The additional inputs for analog signals (e.g. conventional AM/FM receiver, tape etc.) make the amplifier accessible to these audio sources and thus considerably simplify the design of complete radio receivers.

The analog audio output of the WorldSpace signal can be connected to an external stereo amplifier for higher power or quality. Also a digital audio signal in standard I^2S format is provided for high-end applications that may require an external D/A converter.

The complete WorldSpace Broadcast Channel (BC) is available as a serial output signal from the DRD 3515A and provides full access to all WorldSpace data. The additional Service Component (SC) output of the DRD 3515A may be useful in applications where a data and an audio channel are transmitted simultaneously. In this case, the data component is directed to the SC output. This function is independent from the audio Service Component extraction in the MAS 3506D.

Service Control Header data are available via I^{2}C controller interface from the MAS 3506D. (N.B. The Time Slot Control Channel data are available only from the DRD 3515A.)

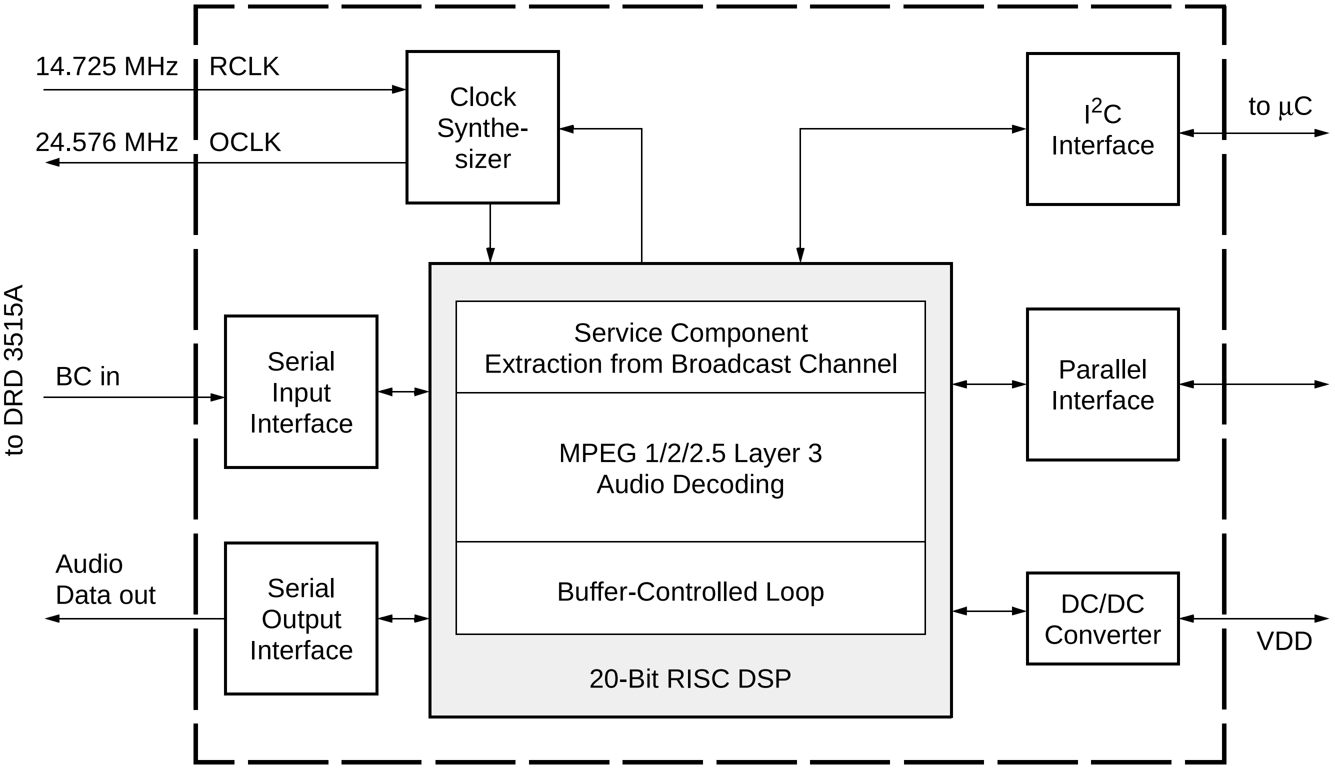

Fig. 1–2: Block diagram of the MAS 3506D

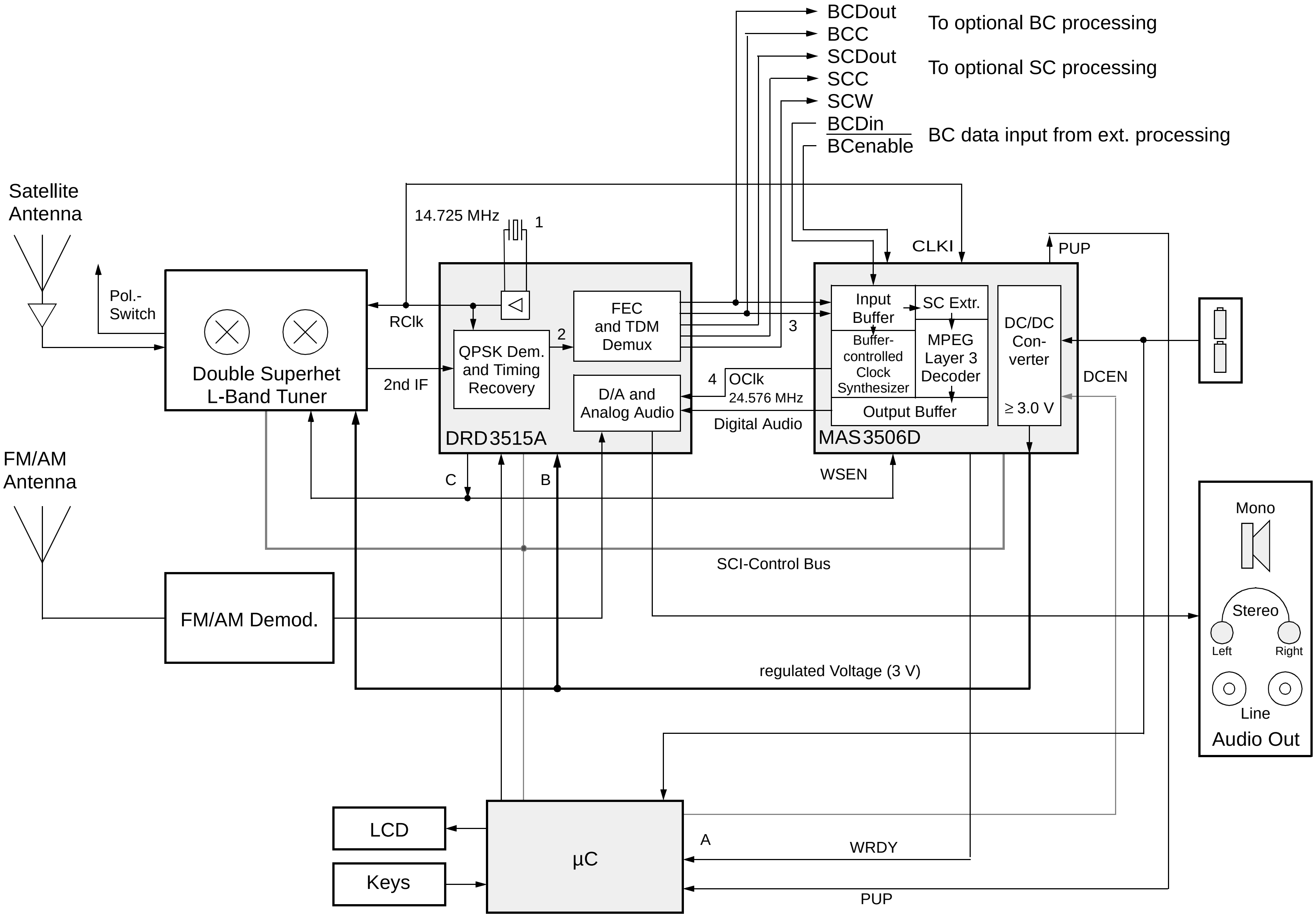

Fig. 1–3: Complete WorldSpace receiver block diagram

2. Functional Description of the MAS 3506D

2.1. Overview

The hardware of the MAS 3506D consists of a high-performance RISC Digital Signal Processor (DSP) and appropriate interfaces for WorldSpace Broadcast Channel decoding (see Figure 2–1). The internal processor works with a memory word length of 20 bits and an extended range of 32 bits in its accumulators. The instruction set of the DSP is highly optimized for audio data compression and decompression. Thus, only very small areas of internal RAM and ROM are required. All the data input and output actions are based on a 'non-cycle-stealing' background DMA that does not cause any computational overhead (except for some initialization). The overall function of the MAS 3506D can be altered by downloading up to 1 kWord of program code into the internal RAM and executing this code instead of the built-in firmware ROM code[1]. Dedicated clock management hardware supports synchronization on the transmitted data signal. A DC/DC step-up converter has been integrated for efficient battery-based operation. Fig. 2–1 shows the building blocks of the MAS 3506D.

[1] Detailed information about downloading is provided in combination with the MAS 3506D software development package or together with the MAS 3506D software modules available from Micronas.

2.2. Firmware (Internal Program ROM)

The firmware of the MAS 3506D operates on the Broadcast Channel signal generated by the DRD 3515A. The MAS 3506D firmware processes the input signal in four steps.

– Broadcast Channel synchronization

– Broadcast Channel demultiplexing

– MPEG audio decoding

– Frame synchronization and decoding error signals are provided at output pins of the MAS 3506D.

2.2.1. Broadcast Channel Synchronization

The MAS 3506D analyzes the incoming BC bitstream and detects the Service Control Header (SCH) preamble. If the preamble is found, the BC-SYNC signal (available at a MAS 3506D output pin) indicates that the MAS 3506D is in synchronized state. If synchronization is lost, the MAS 3506D automatically resets the BC-SYNC signal and performs an audio soft-mute until the next SC-header is detected.

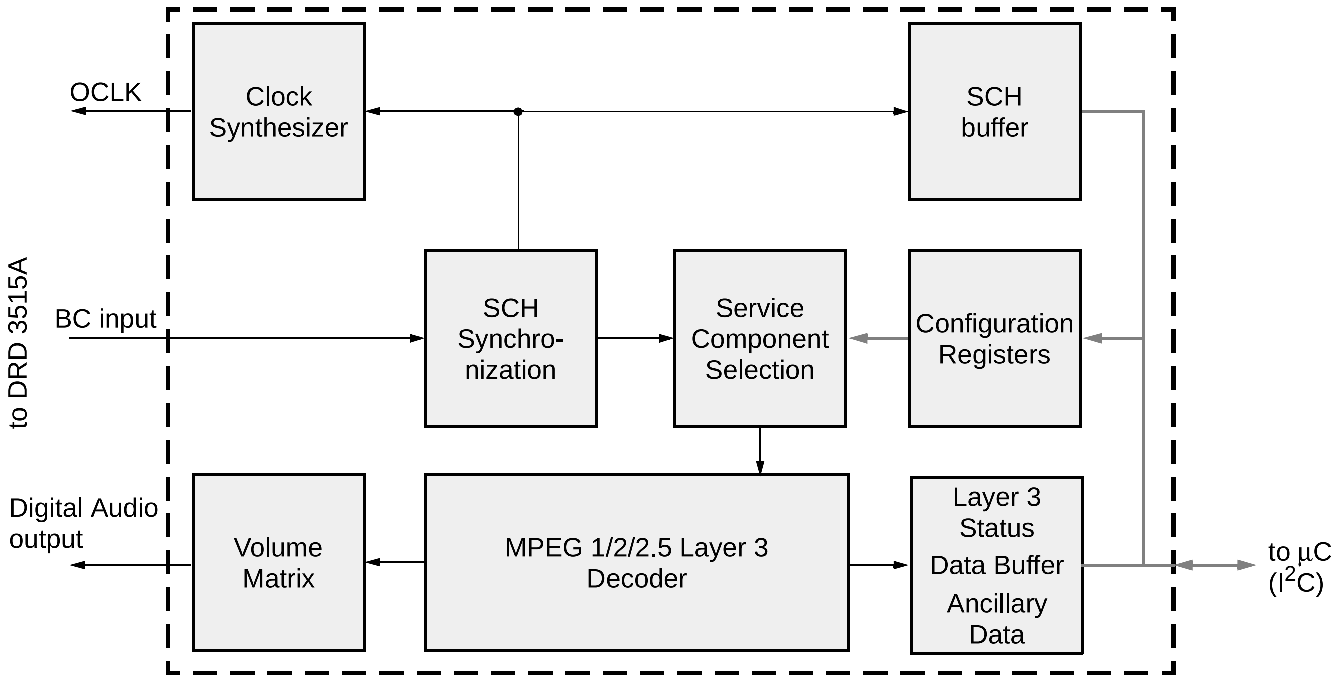

Fig. 2–1: Functional overview of the MAS 3506D

2.2.1.1. Broadcast Channel Timing

The incoming Broadcast Channel bitstream has a framing with a period between Prime Rate Channel Preambles (PRCP) of

prcpt = 432 ms

During one frame the transmission of the BC is interrupted by a gap *prcpgap* of:

prcpgap = 2.5 ms

The data transmission is interrupted by a second gap *mfpgap* with a duration of

mfpgap = 1.2 ms

that is synchronous with the Master Frame Preamble (MFP) cycle with a period of:

mfpt = 138 ms

Both cycles *mfpt* and *prcpt* have a least common multiple at 9936 ms. These gaps are independent of the number of Prime Rate Channels (PRC) *n* that create the considered Broadcast Channel.

2.2.1.2. Buffer-Controlled Loop

For the recovery of the audio sample clock, a buffer-controlled loop is used that operates on the incoming Broadcast Channel bit stream. The buffer control loop characteristic suppresses the effects of these gaps on the stability of the generated audio sample frequency by more than 40 dB. Thus, no audible jitter is introduced to the derived reference clock for the D/A converter (see section 2.3. "Clock Management").

The step response of the buffer-controlled loop is plotted in Figure 2–2 with respect to different number of PRCs. The settling time for the buffer-controlled loop is about 10 s.

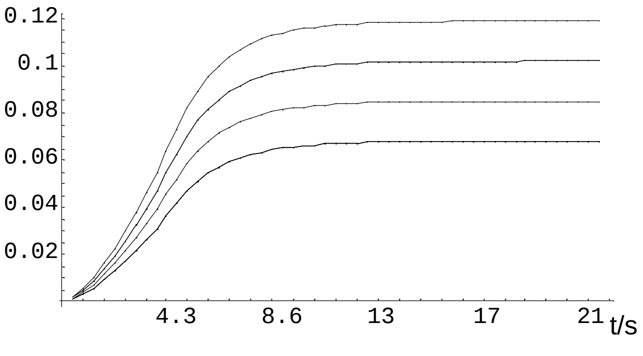

Fig. 2–2: buffer-controlled loop step response

2.2.2. Broadcast Channel Demultiplexing

The Service Control Header that directly follows the SCH-preamble in the BC bitstream is made accessible to the controller after it has been detected. Its availability is indicated by the BC-FRAME-SYNC signal. Information about the content of the Broadcast Channel is given in the Service Control Header data. The controller may select the number of the Service Component that is to be passed to the internal MPEG audio decoder. By default, always Service Component “0” is decoded by the MAS 3506D. An implemented autoscan mode can be selected that skips non-audio Service Components.

2.2.3. MPEG Audio Decoding

The MPEG 1/2/2.5 Layer 3 decoder performs the audio decoding. The steps for decoding are:

– Synchronization

– Side information extraction

– Huffman decoding

– Synthesis filter bank

– Ancillary data extraction

The bit rates and sampling rates that are supported by the MAS 3506D are listed in Table 2–1.

Table 2–1: Sampling frequencies and bit rates

Sampling Freq. in kHz	Bit rates in kBit/s
48, 32, 24, 16, 12, 8	128, 112, 96, 80, 64, 56, 48, 40, 32, 24, 16, 8

Frame synchronization and decoding error signals are provided at output pins of the MAS 3506D.

2.2.4. Baseband Processing

A digital volume control matrix is applied to the digital stereo audio data. This matrix may also perform additional balance control and a simple kind of stereo basewidth enhancement. The four factors LL, LR, RL, and, RR are adjustable via the controller with 20 bit resolution (see Fig. 3–2 on page 28).

2.3. Clock Management

The complete StarMan chip set is driven by a single crystal with a nominal frequency of 14.725 MHz.

The DRD 3515A contains the crystal oscillator and an appropriate clock buffer to generate the clock signal *RClk*. This *RClk* signal is used as reference clock for the MAS 3506D by an internal clock synthesizer that generates an internal system clock of 24.576 MHz.

This synchronized clock frequency is passed back to the DRD 3515A for use in its embedded audio D/A converter.

2.4. Power Supply Concept

The MAS 3506D offers an embedded controlled DC/DC converter for battery based power supply concepts. It works as an up-converter.

2.4.1. Internal Voltage Monitor

An internal voltage monitor compares the input voltage at the VSENS pin with an internal reference value that is adjustable via I^2C bus. The PUP output pin should be observed by the controller. It becomes inactive when the voltage at the VSENS pin drops below the programmed value of the reference voltage.

It is important that the WSEN must not be activated before the PUP signal is generated. The PUP signal thresholds are listed in Table 3–10 on page 20. The internal voltage monitor will be activated with a high level at Pin DCEN.

2.4.2. DC/DC Converter

The DC/DC converter of the MAS 3506D is used to generate a fixed power supply voltage even if the chip set is powered by battery cells in portable applications. The DC/DC converter is designed for the application of 1 or 2 batteries or NiCd cells as shown in Fig. 2–5 which shows the standard application circuit. The DC/DC converter is switched on by activating the DCEN pin. Its output power is sufficient for supplying the complete radio receiver.

Note: Connecting DCEN directly to VDD leads to unexpected states of the DCCF register.

A 22 µH inductor is required for the application. The important specification item is the inductor saturation current rating, which should be greater than 2.5 times the DC load current. The DC resistance of the inductor is important for efficiency. The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR), as the product of the inductor current variation and the ESR determines the high-frequency amplitude seen on the output voltage. The Schottky diode should have a low voltage drop V_D for a high overall efficiency of the DC/DC converter. The current rating of the diode should also be greater than 2.5 times the DC output current. The VSENS pin has to be always connected to the output voltage.

2.4.3. Stand-by Functions

A high level at pin WSEN enables both, the DSP including the I^2C-block and the DC/DC-converter. If the DSP-functions (audio decoding) are not needed, the DC/DC-converter may remain active to supply other parts of the radio. This mode is entered by setting DCEN to “high” and WSEN to “low”. No I^2C control is possible in this mode.

2.4.4. Start-up Sequence

The DC/DC converter starts from a minimum input voltage of 0.9 V. There should be no output load during startup. WSEN must be “low”. The start-up script should be as follows:

1. Start the DC/DC-converter with a high signal (VDD, AVDD) at pin DCEN.
2. Wait until PUP goes “high”.
3. It is recommended to wait at least one millisecond to guarantee that the output voltage has settled.
4. The controller may now enable the DSP with a “high” signal at pin “WSEN”.

Please also refer to Figure 2–3.

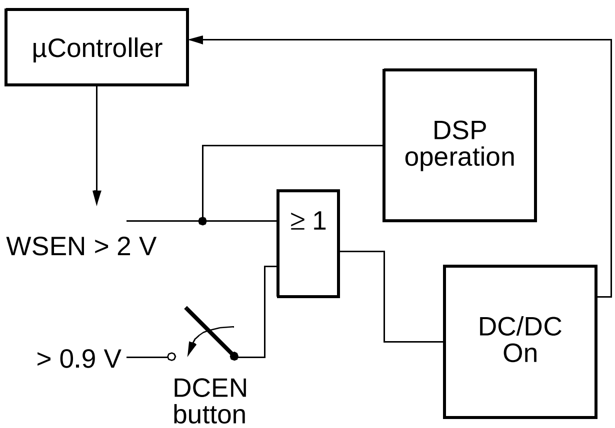

Fig. 2–3: DC/DC operation

2.5. Interfaces

The MAS 3506D uses an I^2C control interface, a serial input interface for the Broadcast Channel, and a digital audio output interface for the decoded audio data (I^2S or similar). Additionally, a general-purpose parallel I/O interface (PIO) may be used for monitoring and mode-selection tasks. The PIO lines are controlled by the internal firmware.

2.5.1. Broadcast Channel (BC) Input Interface

The BC input interface consists of the three pins SIC, SII, and SID. For WorldSpace operation the SII pin is always to be connected to VSS. The Broadcast Channel input signal format is shown in Figure 2–4. The data values are latched with the falling edge of the SIC signal. The input interface is asynchronous and accepts data streams generated by the DRD 3515A BC output.

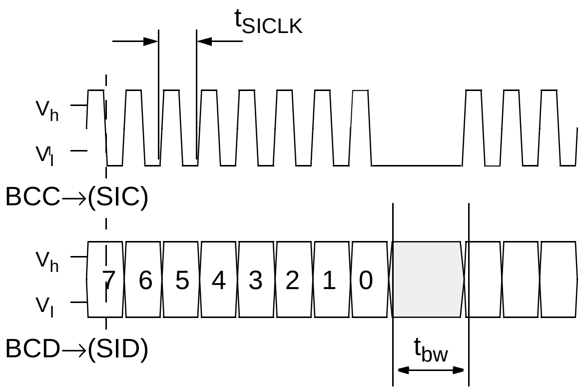

Fig. 2–4: Schematic timing of the SDI (BC) input

The BC input can be switched to an alternate port. This function is controlled by input pin PI18. For more details please see Section 3.1.3. on page 13

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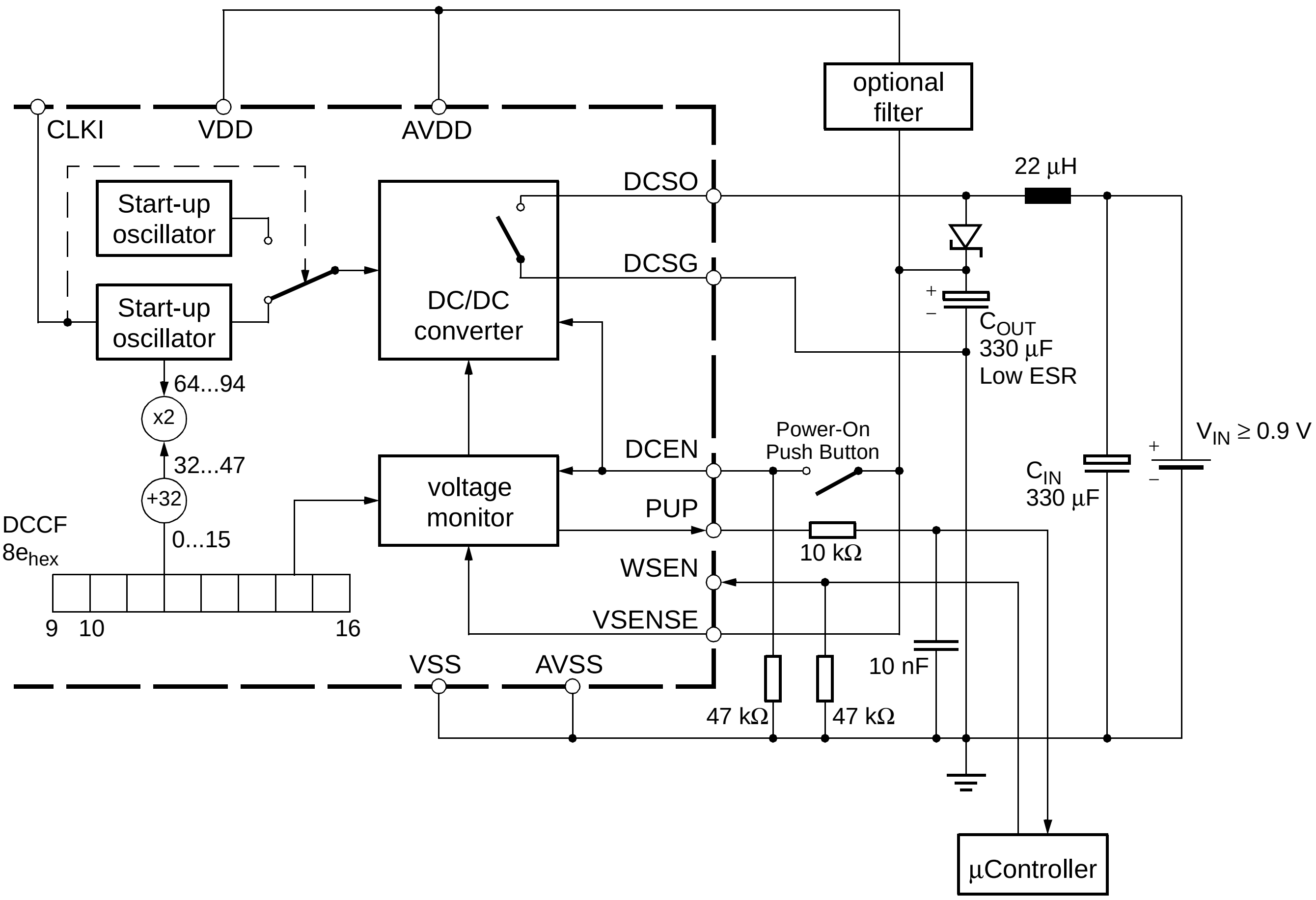


Fig. 2–5: DC/DC converter connections

2.5.2. Parallel Input Output Interface (PIO)

The parallel interface of the MAS 3506D consists of the lines PI0..PI4, PI8, PI12..PI19:

Table 2–2: PIO input and output pin assignment during MPEG decoding

PIO Pin	Name	Comment
PI19 (O)	BC-FRAME-TOGGLE 0 1	Output level toggled each BC-FRAME
PI18 (I)	$\overline{\text{BCINENABLE}}$ 0 1	 enables SI* inputs enables SI inputs
PI13 (O)	BC-FRAME-SYNC 0 1	 start of new frame
P12 (O)	BC-SYNC 0 1	 unsynched synched to BC
PI8 (O)	MPEG-CRC-ERROR 0 1	 no error CRC-error or sync lost
PI4 (O)	MPEG-FRAME-SYNC 0 1	 sync to a new MPEG frame
PI3 (I)	AUD-SW	May be used to monitor a signal indicating switching between Headphone and Loudspeaker mode.
PI2, PI1, PI0 (I)	Reserved	The PI-pins may be monitored by reading the PIO register (see Table 3–10)

These signals are used to indicate the status of the Broadcast Channel and the MPEG Layer 3 decoder. The PIO pin status is also accessible via I^2C interface (see Table 3–10).

2.5.3. Audio Output Interface

The audio output interface of the MAS 3506D is a standard serial audio interface. The interface is configurable by software to work in 16-bit/sample and 32-bit/sample mode. The default setup is a 16-bit mode which is also the default setting for the DRD 3515A. The 32-bit/sample mode is provided for high-resolution D/A converters that expect more than 16-bit/sample input data. The embedded D/A-converter of the DRD 3515A is also capable of decoding the 32-bit/sample format and provides a slightly better S/N performance in this mode[1]. The audio output interface timing is shown in Figure 2–6 and Figure 2–7.

[1] If the 32-bit mode is selected and the D/A converter of the DRD 3515A is still connected, it also has to be switched to 32-bit I^2S mode.

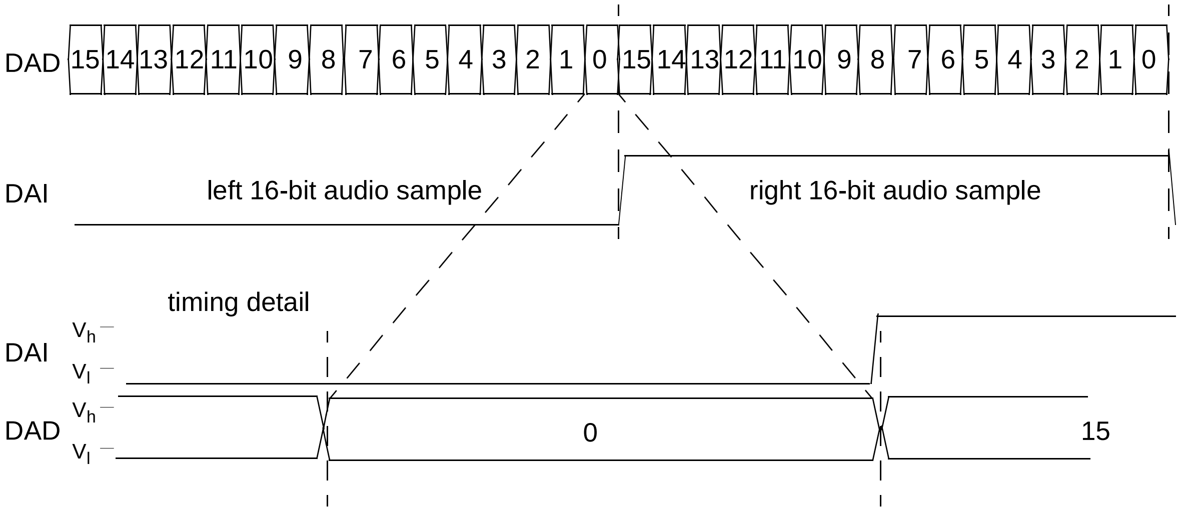


Fig. 2–6: Schematic timing of the digital audio output interface in 16-bit/sample mode

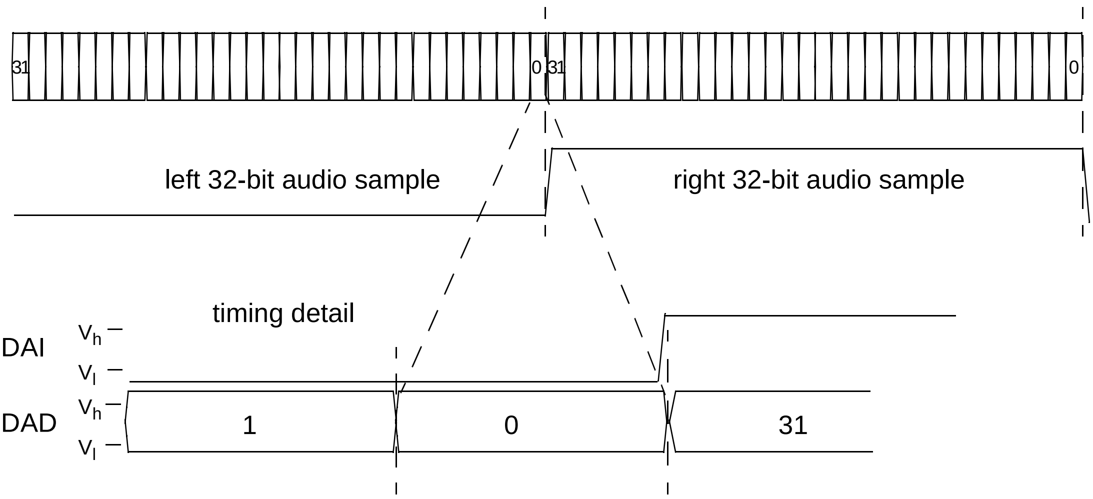


Fig. 2–7: Schematic timing of the digital audio output interface in 32-bit/sample mode

3. Controlling

3.1. I^{2}C-Access

Communication between the MAS 3506D and the external controller is done via an I^{2}C slave interface.

3.1.1. Device Address

The device addresses are $3a_{hex}$ for writing (DW) and $3b_{hex}$ for reading (DR), respectively. I^{2}C clock synchronization is used to slow down the bus if required.

Table 3–1: I^{2}C device address bits

A6	A5	A4	A3	A2	A1	A0	write/ read
0	0	1	1	1	0	1	0/1

3.1.2. I^{2}C Registers and Subaddresses

The interface uses one level of subaddresses. The MAS 3506D interface has 3 subaddresses allocated for the corresponding I^{2}C-registers.

Table 3–2: I^{2}C subaddresses

Sub-address	I^{2}C-Register	Function
68_{hex}	data_write	Controller writes to MAS 3506D data register
69_{hex}	data_read	Controller reads from MAS 3506D data register
$6a_{hex}$	control	Controller writes to MAS 3506D control register

The address $6a_{hex}$ is used for basic control, i.e. reset and task select. The other addresses are used for data transfer from/to the MAS 3506D.

The I^{2}C-control and data registers of the MAS 3506D are 16 bits wide, the MSB is denoted as bit [15]. Transmissions via I^{2}C-bus have to take place in 16-bit words (two byte transfers, MSB sent first); thus for each register access two 8-bit data words must be sent/ received via I^{2}C-bus.

3.1.3. Conventions for the Command Description

The description of the various controller commands uses the following formalism:

– **Abbreviations** used in the following descriptions:
  a address
  d data value
  n count value
  o offset value
  r register number
  x don't care

– Memory addresses like D1:89f are always in hexadecimal notation.

– A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.

– Data values in nibbles are always shown in hexadecimal notation.

– A hexadecimal 20-bit number **d** is written, e.g. as **d** = $17c63_{hex}$, its five nibbles are d0 = 3_{hex}, d1 = 6_{hex}, d2 = c_{hex}, d3 = 7_{hex}, and d4 = 1_{hex}.

– **Variables** used in the following descriptions:

DW	$3a_{hex}$	I^{2}C-device write
DR	$3b_{hex}$	I^{2}C-device read
data_write	68_{hex}	data register write
data_read	69_{hex}	data register read
control	$6a_{hex}$	control register write

– **Bus signals**
  S Start
  P Stop
  A ACK = Acknowledge
  N NAK = Not acknowledge
  W Wait = a wait time (≤ 4 ms) may occur

– **Symbols** in the telegram examples
  < Start condition
  > Stop
  dd data byte
  xx ignore
  All telegram digits are hexadecimal, data originating from the MAS 3506D are grayed.
  Example:
  <3a 68 *dd dd*> write data to DSP
  <3a 69 <3b *dd dd* > read data from DSP

Figure 3–1 shows I^{2}C bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the I^{2}C-device address with the read command (DR). Fields with signals/data originating from the MAS 3506D are marked by a gray background. Note that in some cases the data reading process must be concluded by a NAK condition.

The MAS 3506D firmware scans the I^{2}C interface periodically and checks for pending or new commands.

The commands are then executed by the DSP during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. However, due to some time critical firmware parts, a certain latency time for the response has to be expected at the locations marked with a “W” (= wait). The theoretical worst case response time does not exceed 4 ms. However, the typical response time is less than 0.5 ms.

3.2. I²C Control Register (Subaddress $6A_{hex}$)

S	DW	W	A	control	A	d3,d2	A	d1,d0	W	A	P

The I²C control register is a write-only register. Its main purpose is the software reset of the MAS 3506D. The software reset is done by writing a 16-bit word to the MAS 3506D with bit 8 set. The 4 least significant bits are reserved for task selection. The task selection is only useful in combination with download software. In the standard application these bits must always be set to 0.

Table 3–3: Control register data bit assignment[1)]

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
x	x	x	x	x	x	x	R	0	0	0	0	T3	T2	T1	T0

1) x = don’t care, R = reset, T3...T0 = task selection

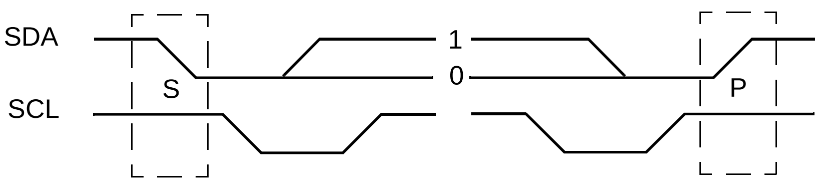
Example: I²C write access

S	DW ($3a_{hex}$)	W	A	data_write (68_{hex})	A	high byte data	A	low byte data	W	A	P

Example: I²C read access

S	DW ($3a_{hex}$)	W	A	data_read (69_{hex})	A	S	DR ($3b_{hex}$)	W	A

high byte data	A	low byte data	W	N	P



W = Wait
A = Acknowledge (Ack)
N = Not Acknowledge (NAK)
S = Start
P = Stop

Fig. 3–1: I²C-bus protocol for the MAS 3506D. Signals originating from the MAS 3506D are grayed.

3.3. I²C-Data Register (Subaddresses 68_{hex} and 69_{hex}) and the MAS 3506D DSP-Command Syntax

The I²C data register is used to communicate with the internal firmware of the MAS 3506D. It is readable (subaddress “data_read”) and writable (subaddress “data_write”) and also has a length of 16 bits. The data transfer is done with the most significant bit (m) first.

Table 3–4: Data register bit assignment

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
m															l

A special command language is used that allows the controller to access the DSP-registers and RAM-cells and thus monitor internal states, set the parameters for the DSP-firmware, control the hardware, and even provide a download of alternative software modules. The DSP-commands consist of a “Code” which is sent to to I²C-data register together with additional parameters.

S	DW	W	A	data_write	A	**Code**,...	A	...,...	A	...

Table 3–5 gives an overview over the different commands which the DSP-core may receive. The “Code” is always the first data nibble transmitted after the “data_write” byte.

The control interface is also used for low-bit-rate data transmission, i.e. MPEG-embedded ancillary data and the WorldSpace Service Control Header. These data are available in a specified memory area of the MAS 3506D after successful decoding. The synchronization between controller and the MAS 3506D will be done by observing the BC-FRAME-SYNC and MPEG-FRAME-SYNC signals in register $c8_{hex}$ or at the corresponding pins.

Table 3–5: Basic controller command codes for the MAS 3506D

Code (hex)	Command	Function
0	Run	Start execution of an internal program. *Run* with start address 0_{hex} means freeze the operating system
1	Run Config	Start execution of an internal program and switch config RAM to P-RAM
5	Select SC	Select the Service Component
6	Read Ancillary Data	Read MPEG ancillary data
8	Read SCH-Data	Read Service Control Header
9	Write Register	An internal register of the MAS 3506D can directly be written to by the controller
a, b	Write Memory	A block of the DSP memory can be written to by the controller. (This feature may be used to download alternate programs.)
d	Read Register	The controller can read an internal register of the MAS 3506D
e, f	Read Memory	A block of the DSP memory can be read by the controller

3.3.1. Data Formats

The internal data word size is 20 bits. All RAM-addresses can be accessed in a 20-bit mode via I^2C-bus. Because of the 16-bit width of the I^2C-data register the full transfer of all 20 bits requires two 16-bit I^2C-words. Some commands only access the lower 16 bits of a cell. For fast access of internal DSP-states the processor core also has an address space of 256 data registers.

The internal data format is a 20 bit two's complement denoted "r". If in some cases a fixed point notation "v" is necessary. The conversion between the two forms of notation is done as follows:

r = v*524288.0+0.5; $(-1.0 \le v < 1.0)$
v = r/524288.0; $(-524288 < r < 524287)$

3.3.2. Run and Freeze (Codes 0_{hex} to 1_{hex})

S	DW	W	A	data_write	A	a3,a2	A	a1,a0	W	A	P

The Run command causes the start of a program part at address **a** = (a3,a2,a1,a0). Note that nibble a3 is also the command code (see Table 3–5) and thus it is restricted to certain values. This command is especially used to start alternate code or downloaded code from a RAM-area that has been configured as program RAM.

Example 1: Start program execution at address 345_{hex}:

```
<3a 68 03 45>
```

Freeze is a special run command with start address 0. It suspends all normal program execution. The operating system will enter an idle loop so that all registers and memory cells can be watched. This state is useful for operations like downloading code or contents of memory cells because the internal program cannot overwrite these values. This freezing will be required if alternative software is downloaded into the internal RAM of the MAS 3506D.

Freeze has the following I^2C protocol:

```
<3a 68 00 00>
```

The entry point of the default software will be accessed automatically after a reset, thus issuing a *Run* or *Freeze* command is only necessary for starting downloaded software or special program modules which are not part of the standard set.

3.3.3. Select Service Component (Code 5_{hex})

S	DW	W	A	data_write	A	**5**,0	A	0,0	W	A	
						0,0	A	0,d0	W	A	P

Select the (zero-based) service component with the number **d** = d0. The number of available service components is to be taken from the SCH information. A maximum of 8 service components are allowed in one Broadcast Channel. SC-selection is also possible by writing to memory cell D1:7ef (see Table 3–11 on page 23).

3.3.4. Read Ancillary MPEG Data (Code 6_{hex})

1) send command (Read D0)

S	DW	W	A	data_write	A	**6**,o2	A	o1,o0	W	A	P

2) get ancillary data values

S	DW	W	A	data_read	A	S	DR	W	A		
						d3,d2	A	d1,d0	W	A	

....repeat for n data values....

						d3,d2	A	d1,d0	W	N	P

The availability of new ancillary data is indicated by the MPEG-FRAME-SYNC signal in register $c8_{hex}$ or at the corresponding pin. Ancillary data are available every 24 to 32 ms depending on the sample rate of the MPEG-bitstream. The instruction parameters are embedded in the 3 nibbles o2..o0. The 6 MSBs indicate the address offset counted in 16-bit words where the read-out of the ancillary data shall start. The 6 LSBs indicate the number of 16-bit words that are to be transmitted by MAS 3506D.

Table 3–6: Arrangement of o-bits

11	10	9	8	7	6	5	4	3	2	1	0
o2				o1				o0			
address offset						number of 16-bit words					

The data values that are returned are organized in the following table:

Table 3–7: Content of ancillary data field

Offset	Content
0	Bit 17..32 of MPEG header[1)]
1	Bit 12..16 of MPEG header[2)]
2	Number of ancillary data bits
3	Last 16 bits of ancillary data
...	
$\leq$28	First 16 bits of ancillary data

1) see address D1:7f6 in Table 3–11 on page 23
2) see address D1:7f5 in Table 3–11 on page 23

The ancillary data values are copied in the reverse order into this data field where the last bit received is place at bit 0 of the data word at offset 3. The number of data words with content can be calculated as follows:

int [(NumberOfAncillaryBits-1)/16] + 1

Limitations:

– The maximum number of data words that can be read out are 28.

– The upper limit for ancillary data bitrate is 9600 bps.

– The ancillary data are only valid for 6 ms after the MPEG-FRAME-SYNC signal.

Memory example:

The MPEG bitstream contains 20 bits of ancillary data with the content f0f08$_{hex}$. Then the ancillary data field content will be:

Table 3–8: Ancillary data example

Offset	Content
0	Bit 17..32 of MPEG header
1	Bit 12..16 of MPEG header
2	14$_{hex}$ (number of anc bits)
3	0f08$_{hex}$ (bit-order reversed)
4	xxxf$_{hex}$

Telegram example:

First get the content of 'Number of ancillary bits':

<3a	device write (I^2C-address)
68	data write
60 81>	code 6$_{hex}$, offset 2, count 1: Get number of ancillary bits
<3a 69 <3b	initiate reading
dd dd >	and read number of bits

Calculate number of words to be read from the number of bits received (e.g. 20 bits require two words).

<3a	device write (I^2C-address)
68	data write
60 c2>	code 6$_{hex}$, offset 3, count 2: Read two words from offset 3.
<3a 69 <3b	initiate reading
dd dd	and read two words
dd dd >	

3.3.5. Read SCH-Data (Code 8_{hex})

1) send command (Read D0)

S	DW	W	A	data_write	A	**8**,o2	A	o1,o0	W	A	P

2) get SCH-values

S	DW	W	A	data_read	A	S	DR	W	A		
						d3,d2	A	d1,d0	W	A	

....repeat for n data values....

d3,d2	A	d1,d0	W	N	P

The availability of Service Control Header data is indicated by the related status registers or the BC-FRAME-SYNC. The instruction parameters are embedded in the 3 nibbles o2..o0. The 6 MSBs indicate **half** of the address offset counted in 16-bit words where the read out of the SCH data shall start. The 6 LSBs indicate **half** of the number of 16-bit words that are to be transmitted by the MAS 3506D.

Example:

If 4 words starting with SCH-word 10 shall be read out the command parameters o2..o0 have to be set to:

Table 3–9: SCH-command example

11	10	9	8	7	6	5	4	3	2	1	0
o2				o1				o0			
0	0	0	1	0	1	0	0	0	0	1	0
5						2					
5 means offset of (10 16-bit-words)/2						2 means amount of (4 16-bit-words)/2					

Thus the command sequence that is to be sent to the MAS 3506D is:

<3a	device write (MAS 3506D I^2C-address)
68	data write
81 42>	code 8_{hex}, 4 words from offset word 10

The data read sequence is then initialized by

<3a	DW (MAS 3506D write address)
69	data read
<3b	DR (MAS 3506D read address)

Then the MAS 3506D will send the SCH-values

dd dd	SCH10.h, SCH10.l
dd dd	SCH11.h, SCH11.l
dd dd	SCH12.h, SCH12.l
dd dd >	SCH13.h, SCH13.l

where SCHx.h/l refers to the high/low part of the xth word of the SCH.

Common Parameters with Command-Code 8_{hex}

Often the four nibbles defining start address and amount to be transmitted (8_{hex}, o2, o1, o0) may have the following values:

– `80 04`: Read 16 bytes (= 8 words, 6 LSBs = 4) from the beginning (offset = 0, 6 MSBs = 0) of the SCH (i.e. everything from the beginning up to ADF2)

– `81 01`: Read 4 bytes (= 2 words, 6 LSBs = 1) starting at 16 bytes (= 8 words, 6 MSBs = 4) offset (i.e. one Service Component Control Field SCCF)

– `81 05`: Read 20 bytes (= 10 words, 6 LSBs = 5) starting at 16 bytes (= 8 words, 6 MSBs = 4) offset (i.e. 5 Service Component Control Fields SCCF)

3.3.6. Write Register (Code 9_{hex})

S	DW	W	A	data_write	A	**9**,r1	A	r0,d4	W	A	
						d3,d2	A	d1,d0	W	A	P

The controller writes the 20-bit value (**d** = d4,d3,d2,d1,d0) into the MAS 3506D register (**r** = r1,r0). A list of registers needed for control purposes is given in Table 3–10 on page 20.

Example: Writing the value 81234_{hex} into the register with the number aa_{hex}:

`<3a 68 9a a8 12 34>`

3.3.7. Write Memory (Codes A_{hex} and B_{hex})

The memory areas D0 and D1 can be written by using the codes a_{hex} and b_{hex}, respectively.

S	DW	W	A	data_write	A	**a**,0	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	
....repeat for n data values....											
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	P

With the *Write D0/D1 Memory* command n 20-bit memory cells in D0 can be initialized with new data.

Example: Write 80234_{hex} to D1:456 has the following I^2C protocol:

```
<3a 68 b0 00        write D1 memory
     00 01          1 word to write
     04 56          start address
     00 08          value = 80234hex
     02 34>
```

3.3.8. Read Register (Code D_{hex})

1) send command

S	DW	W	A	data_write	A	**d**,r1	A	r0,0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A		
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P

The MAS 3506D has an address space of 256 DSP-registers. Some of the registers (**r** = r1,r0 in the figure above) are direct control inputs for various hardware blocks, others control the internal program flow. In Table 3–10, the registers of interest are described in detail. In contrast to memory cells, registers cannot be accessed as a block but must always be addressed individually.

Example:
Read the content of the register $c8_{hex}$:

```
<3a 68 dc 80>              define register
<3a 69 <3b xx xd dd dd >   and read
```

3.3.9. Read Memory (Codes E_{hex} and F_{hex})

The MAS 3506D has 2 memory areas called D0 and D1 using the codes e_{hex} and f_{hex} for their read commands, respectively.

1) send command (Read D0)

S	DW	W	A	data_write	A	**e**,0	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A		
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	
....repeat for n data values....											
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P

The *Read D0/D1 Memory* command gives the controller access to all 20 bits of the memory cells of the MAS 3506D. The telegram for reading 3 words starting at location D1:100 is

```
<3a 68 f0 00 00 03 01 00>
<3a 69 <3b xx xd dd dd
           xx xd dd dd xx xd dd dd >
```

3.3.10.Default Read

S	DW	W	A	data_read	A	S	DR	W	A			
							d3,d2	A	d1,d0	W	N	P

The *Default Read* command immediately returns the lower 16 bits of the main status cell (“Status”) of the MAS 3506D and may be used to poll the processor status. The meaning of the returned bits is given in the description of control memory cell D1:7ee in Table 3–11 on page 23.

3.4. Control Registers

The registers displayed in the following table can be read and written via I^2C commands described (see Section 3.3.6. and Section 3.3.8.).

Note! Registers not given in the tables must not be written.

Table 3–10: Control Registers

<table>
<tr><th>Address (hex)</th><th>R/W</th><th colspan="3">Function</th><th>Default (hex)</th><th>Name</th></tr>
<tr><td rowspan="5">8e</td><td rowspan="5">W</td><td colspan="3">DC/DC-Converter Frequency and Voltage
The I^2C protocol is working only if the processor is active (WSEN = 1). However, the setting for the DCCF register will remain active if the WSEN line is deasserted.</td><td rowspan="5">08000</td><td rowspan="5">DCCF</td></tr>
<tr><td colspan="3">DC/DC-Converter Frequency
The frequency is controlled with bits 13...10 and 8.</td></tr>
<tr><td>Setting
bit [13:10]</td><td>Frequency/kHz
bit [8] = 0</td><td>Frequency/kHz
bit [8] = 1</td></tr>
<tr><td>11 11
11 10
11 01
11 00
10 11
10 10
10 01
10 00
01 11
01 10
01 01
01 00
00 11
00 10
00 01
00 00</td><td>156
160
163
167
171
175
179
184
188
194
199
204
210
216
223
230</td><td>128
245
253
263
272
283
295
307
320
335
351
368
387
409
433
460</td></tr>
<tr><td colspan="3">The divider for the CLKI input is determined by the content of the DCCF register. This register allows 32 settings of the DC/DC converter clock frequency f_{dc}:

$$f_{SW} = \left.\frac{f_{CKLI}}{2 \cdot (m+n)}\right|_{n \in \{0,15\},\, m \in \{16,32\}}$$ (EQ 1)

In order to reduce interference noise in AM-reception, the oscillator frequency may be adjusted in 16 steps in order to allow the system controller to select a base frequency that does not interfere with an other application. The following algorithm may be used to select an appropriate value for DCCF:</td></tr>
</table>

Table 3–10: Control Registers, continued

Address (hex)	R/W	Function	Default (hex)	Name
8e continued		(see below)		DCCF continued

```
int selectfrequency(double fstation) {
    double fq,fdiv;
    double fqmax = 0;
    int imax = 0;
    for (int i=0;i<16;i++) {
        fdiv = 14725000/(2*(32+i));
        fq = fstation/fdiv;
        fq = fabs(fq-floor(fq)-0.5)*fdiv;
        if (fq > fqmax) imax = i;
    }
    return imax;
}
```

Modifications to this algorithm are applicable. It may be useful to finish this procedure if fqmax reaches a certain minimum value, or a preprocessed table for all possible AM-carrier frequencies may be stored in ROM for the controller.

DC/DC-Converter Voltage

The output voltage is selected with bits 16...14 and 9. There is a threshold between the output voltage of the DC/DC converter and the internal voltage monitor. The PUP signal becomes inactive when the output drops below the monitor voltage.

Setting bit [16:14] and [9]	DC/DC-Converter Output Voltage/V	Internal Monitor Voltage/V
1 11 0	3.57	3.38
1 10 0	3.46	3.27
1 01 0	3.35	3.16
1 00 0	3.25	3.06
0 11 0	3.14	2.95
0 10 0	3.04	2.85
0 01 0	2.94	2.75
0 00 0	2.83	2.64
1 11 1	2.73	2.54
1 10 1	2.63	2.44
1 01 1	2.52	2.33
1 00 1	2.42	2.23
0 11 1	2.32	2.13
0 10 1	2.22	2.03
0 01 1	2.12	1.93
0 00 1	2.02	1.82

Table 3–10: Control Registers, continued

Address (hex)	R/W	Function	Default (hex)	Name
c8	R	**PIO-Register** The PIO-register is used to monitor the actual status of the PIO-pins for both, PIO-output and PIO-input lines. Bit 0 of the PIO register corresponds to pin PI0, bit 1 to PI1 etc. Due to the latency of the MAS 3506D only slow events (>1 ms) can be monitored. Please also refer to Section 4.6.3.2. bit [19] BC-FRAME-TOGGLE Output level toggles with each BC-frame, t_{frame} = 432 ms bit [18] $\overline{\text{BCENABLE}}$ 0 use SID*, SII*, SIC* 1 use SID, SII, SIC bit [13] BC-FRAME-SYNC 0 cleared after SCH-read operation 1 start of new frame bit [12] BC-SYNC 0 unsynchronized 1 synchronized to BC bit [8] Decoding-ERROR 0 no error 1 error or sync lost bit [4] MPEG-FRAME-SYNC 0 cleared after anciliary data were read 1 sync to a new MPEG-frame bit [3] AUD-SW This bit may be used to monitor a signal from the headphone jack that indicates switching between headphone and loudspeaker mode. bit [2:0] These three free input lines return the state logic level of the respective PIO-pins. They may be used as a port expansion of the controller.		PIO

3.5. Control and Status Memory

The memory cells given in the following sections may be read (Section 3.3.9.) or written (Section 3.3.7.) in order to observe or control the operation of the MAS 3506D.

Note! Memory cells not given in the tables must not be written.

Table 3–11: Control and status memory cells

Address (hex)	R/W	Function	Default	Name
D1:7ee	R	**Main Status Indicator of the BC-Decoder** The Status cell returns global status information about the World-Space decoder. Its value is also returned by the *'Default Read'* command as described in Section 3.3.10. bit [15:12] BRI Bit Rate Index 0 Reserved 1...8 n*16 kbit/s bit [11:8] NSC Zero-based number of available Service Components 0 1 SC available ... ... 7 8 SCs available bit [7:4] reserved bit [3] MCRC MPEG CRC Error 0 no CRC-error in the last BC-frame 1 CRC-error occured in the last BC-frame bit [2] MFS MPEG frame sync indication 0 no MPEG synchronisation 1 MPEG synchronisation bit [1] BCS Broadcast Channel frame sync indication 0 no BC synchronisation 1 BC synchronisation While the signals MPEG-FRAME-SYNC and BC-FRAME-SYNC in the PIO-register $c8_{hex}$ rise with the beginning of each frame, the signals MFS and BFS are stable as long as a valid bitstream is received. bit [0] S Synchronized state 0 not in synchronized state (e.g. no bitstream) 1 MAS 3506D is synchronized and decoding		Status

Table 3–11: Control and status memory cells, continued

Address (hex)	R/W	Function	Default	Name
D1:7ef	R/W	**Service Component Selection (0..7) and Decoding Control** bit [15] OutputMute 0 normal operation 1 mute output bit [14] AutoScan Autoscan function 0 disable autoscan function 1 enable autoscan function, skip non-audio SCs bit [13] BCChange Broadcast Channel Change 0 cleared on SCH-rescynchronization 1 clears all previous SCH-information Setting this bit clears all previous SCH-information and thus prepares the MAS 3506D for a BC-change. This ensured the availability of the correct SCH-data for the new BC. bit [12] MPEGResync 0 allows resynchronization only after SCH-detection 1 MPEG-resynchronization enabled bit [11:3] reserved, set to 0 bit [2:0] SC Zero-based number of audio Service Component to be decoded 0 decode SC 1 ... 7 decode SC 8		NumSC
D1:7f0	R/W	**Counter for Broadcast Channel Frames** bit [15:0] BCCount Counter for the decoded Broadcast Channel frames The BCFrameCnt ist incremented by one for each successfully decoded BC-frame (432 ms) since reset. This address is writable, thus the controller may reset/preset the content at any time to an arbitrary value.		BCFrameCnt
D1:7f1	R/W	**Counter for MPEG Frames** bit [15:0] MPEGFrameCnt Counter for the decoded MPEG-frames The MPEGFrameCnt ist incremented by one for each successfully decoded MPEG-frame (24...72 ms) since reset. This address is writable for a reset/preset.		MPEG-FrameCnt

Table 3–11: Control and status memory cells, continued

Address (hex)	R/W	Function	Default	Name
D1:7f3	R	**System Error Indication** bit [10:0] ErrorCode Last error of WorldSpace decoding $1xx_{hex}$ Buffer problem, causes a firmware reset: 100_{hex} ErrorInputTimeOut: Input time-out 101_{hex} ErrorServicePreambleWrong: Service preamble wrong 102_{hex} ErrorBufferOverflow: Input buffer overflow 103_{hex} ErrorBufferUnderrun: Buffer underflow 104_{hex} ErrorOutputTimeout: Output time-out 105_{hex} ErrorBitrateIntexChanged: Bitrate index has changed 106_{hex} ErrorNoLayer3SyncNextFram: No synchronization found in input bitstream $2xx_{hex}$ BC-error, causes a BC-resynchronization: 100_{hex} ErrorSCToDecodeOutOfRange: SC to decode is not available 101_{hex} ErrorSCTypeWrong: SC has no audio $1ff_{hex}$ ErrorStartBCSync: The controller has indicated a BC-change (signal BCChange) $3xx_{hex}$ MPEG-error, causes an MPEG-resynchronization: 300_{hex} ErrorSCToDecodeUserChange: A new SC was selected 301_{hex} Error: 302_{hex} Error: 303_{hex} Error: Sampling rate changed If an error occurs during decoding of the Broadcast Channel bitstream a number describing the error will be copied into this memory cell. The content always keeps a value corresponding to the last detected error.		ErrorCode
D1:7f4	R/W	**Counter for All Decoding Errors** bit [15:0] ErrorCnt Counter for all decoding errors The ErrorCnt is incremented by one for each decoding error since reset. This address is writable for a reset/preset. This counter is valuable for long-time observations. For identification of the last error see D1:7f3		ErrorCnt

Table 3–11: Control and status memory cells, continued

Address (hex)	R/W	Function	Default	Name
D1:7f5	R	**Bits 12..16 of MPEG-Header** The MPEGStatus1 memory cell provides a direct copy of bits 16...12 of the acual MPEG-header. This cell will be updated imme-diatley after the MPEG-header has beed read from the bitstream. bit [12:8] Copy of bits 16...12 of the MPEG-header bit [12:11] MPEGID Bits 13 and 12 of the MPEG-header 00 MPEG 2.5 01 reserved 10 MPEG 2 11 MPEG 1 bit [10:9] Layer Bits 11 and 10 of the MPEG-header 00 reserved 01 Layer 1* 10 Layer 2* 11 Layer 3 bit [8] Protection 0 CRC-protected 1 no CRC bit [7] reserved bit [6:2] private bits bit [1] CRC Error 0 no error 1 a CRC-error has occured bit [0] Invalid Frame 0 normal operation 1 an invalid frame has occured		MPEGStatus1

Table 3–11: Control and status memory cells, continued

<table>
<tr><th>Address (hex)</th><th>R/W</th><th>Function</th><th>Default</th><th>Name</th></tr>
<tr><td>D1:7f6</td><td>R</td><td>Bit 32...17 of MPEG-Header
The MPEGStatus2 memory cell provides a direct copy of bits 32...17 of the acual MPEG-header. This cell will be updated immediately after the MPEG-header has beed read from the bitstream.
<table>
<tr><td></td><td>MPEG 1
Layer 3</td><td>MPEG 2
Layer 3</td><td>MPEG 2.5
Layer 3</td></tr>
<tr><td>bit[15:12]</td><td colspan="3">Datarate in kbit/s</td></tr>
<tr><td>0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111</td><td>free
32
40
48
56
64
80
96
112
128
160*
192*
224*
256*
320*
reserved</td><td>free
8
16
24
32
40
48
56
64
80
96
112
128
144*
160*
reserved</td><td>free
8
16
24
32
40
48
56
64
80
96
112
128
144*
160*
reserved</td></tr>
<tr><td>bit[11:10]</td><td colspan="3">Sampling frequency/kHz</td></tr>
<tr><td>00
01
10
11</td><td>44.1*
48
32
reserved</td><td>22.05*
24
16
reserved</td><td>11.025*
12
8
reserved</td></tr>
</table>
bit[9] padding bit
bit[8] private bit
bit[7:6] Mode
00 stereo
01 joint stereo
10 dual channel
11 reserved
bit[5:4] Joint stereo: Mode extension
intensity stereo ms_stereo
00 off off
01 on off
10 off on
11 on on
bit[3] Copyright
0 not protected
1 protected
bit[2] Original/Copy
0 copy
1 original</td><td></td><td>MPEGStatus2</td></tr>
</table>

Table 3–11: Control and status memory cells, continued

Address (hex)	R/W	Function	Default	Name
D1:7f6 continued		bit[1:0] Emphasis 00 none 01 50/15 µs 10 reserved 11 CCITT J.17		
D1:7f7	R/W	**Configures the Serial Audio Output Interface** bit [19:0] OutputConfig 0 generate 32-bit audio samples 16 generate 16-bit audio samples		OutputConfig
D1:7f8	R/W	**Left → Left Gain** bit [19:0] LL left → left gain (please refer to Sections 3.3.1. and 3.5.1.)	80000	LL
D1:7f9	R/W	**Left → Right Gain** bit [19:0] LR left → right gain	00000	LR
D1:7fa	R/W	**Right → Left Gain** bit [19:0] RL right → left gain	00000	RL
D1:7fb	R/W	**Right → Right Gain** bit [19:0] RR right → right gain	80000	RR
* Modes marked with an asterisk are not used in the WorldSpace system.				

3.5.1. Volume Matrix

The digital baseband volume matrix is used for controlling the digital gain as shown in Fig. 3–2. Table 3–12 shows the proposed settings for the four volume matrix coefficients for stereo, left, and right mono. The gain factors are given in fixed point notation as desribed in Section 3.3.1.

Table 3–12: Settings for the digital volume matrix

Memory location (hex)	D1: 7f8	D1: 7f9	D1: 7fa	D1: 7fb
Name	LL	LR	RL	RR
Stereo (default)	–1.0	0	0	–1.0
Mono left	–1.0	–1.0	0	0
Mono right	0	0	–1.0	–1.0

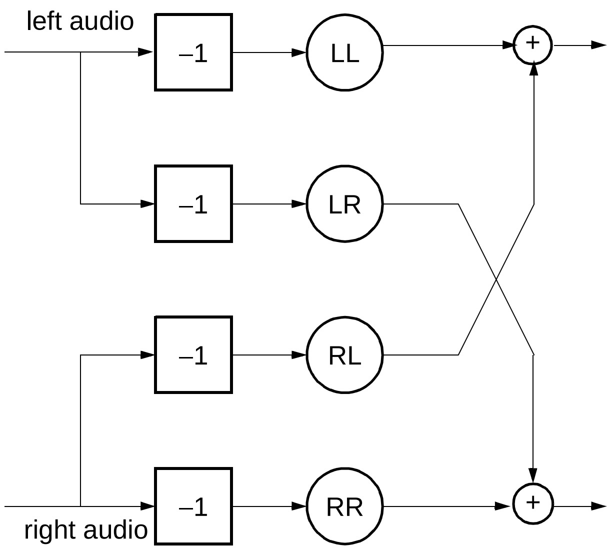


Fig. 3–2: Digital volume matrix

Table 3–13: Volume matrix conversion (dB into hexadecimal)

Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal	Volume (in dB)	Hexa decimal
0	80000	–20	F3333	–40	FEB85	–60	FFDF4	–80	FFFCC
–1	8DEB8	–21	F4979	–41	FEDBF	–61	FFE2D	–81	FFFD1
–2	9A537	–22	F5D52	–42	FEFBB	–62	FFE60	–82	FFFD6
–3	A5621	–23	F6F03	–43	FF180	–63	FFE8D	–83	FFFDB
–4	AF3CD	–24	F7EC8	–44	FF314	–64	FFEB5	–84	FFFDF
–5	B8053	–25	F8CD5	–45	FF47C	–65	FFED9	–85	FFFE3
–6	BFD92	–26	F995B	–46	FF5BC	–66	FFEF9	–86	FFFE6
–7	C6D31	–27	FA485	–47	FF6DA	–67	FFF16	–87	FFFE9
–8	CD0AD	–28	FAE78	–48	FF7D9	–68	FFF2F	–88	FFFEB
–9	D2958	–29	FB756	–49	FF8BC	–69	FFF46	–89	FFFED
–10	D785E	–30	FBF3D	–50	FF986	–70	FFF5A	–90	FFFEF
–11	DBECC	–31	FC648	–51	FFA3A	–71	FFF6C	–91	FFFF1
–12	DFD91	–32	FCC8E	–52	FFADB	–72	FFF7C	–92	FFFF3
–13	E3583	–33	FD227	–53	FFB6A	–73	FFF8B	–93	FFFF4
–14	E675F	–34	FD723	–54	FFBEA	–74	FFF97	–94	FFFF6
–15	E93CF	–35	FDB95	–55	FFC5C	–75	FFFA3	–95	FFFF7
–16	EBB6A	–36	FDF8B	–56	FFCC1	–76	FFFAD	–96	FFFF8
–17	EDEB6	–37	FE312	–57	FFD1B	–77	FFFB6	–97	FFFF9
–18	EFE2C	–38	FE638	–58	FFD6C	–78	FFFBE	–98	FFFF9
–19	F1A36	–39	FE905	–59	FFDB4	–79	FFFC5	–99	FFFFA

4. Specifications

4.1. Outline Dimensions

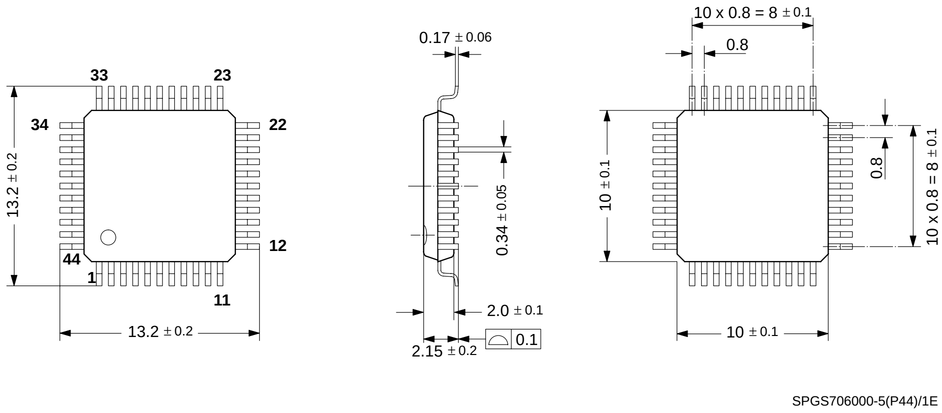


Fig. 4–1:
44-Pin Plastic Metric Quad Flat Package
(PMQFP44)
Weight approximately 0.4g
Dimensions in mm

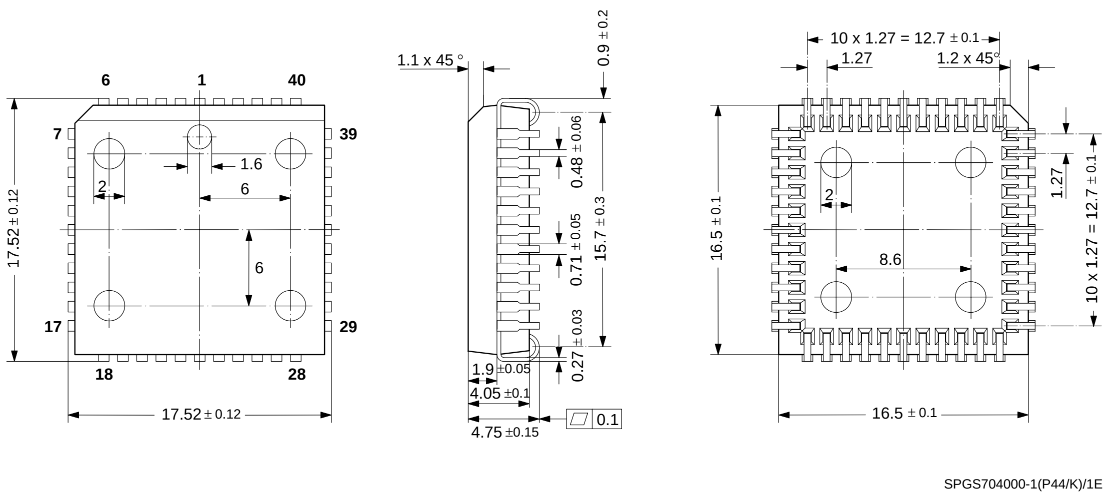


Fig. 4–2:
44-Pin Plastic Leaded Chip Carrier Package
(PLCC44)
Weight approximately 2.5 g
Dimensions in mm
Note: The PLCC44-package has limited availability

Caution: Start pin and orientation of pin numbering is different for PLCC and PMQFP-housings.

4.2. Pin Connections and Short Descriptions

NC	not connected, leave vacant	LV	if not used, leave vacant
X	obligatory, pin must be connected as described in application informations	VDD	connect to positive supply
		VSS	connect to ground

Pin No.		**Pin Name**	**Type**	**Connection**	**Short Description**
PMQFP 44-pin	**PLCC 44-pin**			**(If not used)**	
1	6	TE	I	VSS	Test enable
2	5	$\overline{\text{POR}}$	I	VDD	Reset , active low
3	4	I2CC	IO	X	I^2C clock line
4	3	I2CD	IO	X	I^2C data line
5	2	VDD	Supply	X	Positive supply for digital parts
6	1	VSS	Supply	X	Gound supply for digital parts
7	44	DCEN	I	VSS	Start and enable DC/DC converter
8	43	$\overline{\text{EOD}}$	O	LV	PIO end of DMA, active low
9	42	$\overline{\text{RTR}}$	O	LV	PIO ready to read, active low
10	41	$\overline{\text{RTW}}$	O	LV	PIO ready to write, active low
11	40	DCSG	Supply	VSS	DC converter transistor ground
12	39	DCSO	O	VSS	DC converter transistor open drain
13	38	VSENS	I	VDD	DC converter voltage sense
14	37	PR	I	VDD	PIO DMA request or Read/$\overline{\text{Write}}$
15	36	$\overline{\text{PCS}}$	I	VDD	PIO chip select , active low
16	35	PI19	O	LV	BC-Frame-Toggle
17	34	PI18	I	VSS	$\overline{\text{BCINENABLE}}$
18	33	PI17	I	VSS	PIO data [17], reserved
19	32	SIC*/PI16	I	X	PIO data[16] (SIC*)
20	31	SII*/PI15	I	VSS	PIO data[15] (SII*)
21	30	SID*/PI14	I	X	PIO data [14] (SID*)
22	29	PI13	O	LV	BC-FRAME-SYNC
23	28	PI12	O	LV	BC-SYNC
24	27	SOD/PI11	O	LV	Serial output data
25	26	SOI/PI10	O	LV	Serial ouput frame identification
26	25	SOC/PI9	O	LV	Serial output clock
27	24	PI8	O	LV	Decoding-error
28	23	XVDD	Supply	X	Positive supply of output buffers

Pin No.		Pin Name	Type	Connection	Short Description
PMQFP 44-pin	PLCC 44-pin			(If not used)	
29	22	XVSS	Supply	X	Ground of output buffers
30	21	SID/PI7	I	X	Serial input data
31	20	SII/PI6	I	VSS	Serial input frame identification
32	19	SIC/PI5	I	X	Serial input clock
33	18	PI4	O	LV	MPEG-frame sync
34	17	PI3	I	VSS	AUD-SW, information from head-phone jack
35	16	PI2	I	VSS	Reserved
36	15	PI1	I	VSS	Reserved
37	14	PI0	I	VSS	Reserved
38	13	CLKO	O	LV	Clock output (nominal 24.576 MHz)
39	12	PUP	O	LV	Power Up, i.e. status of voltage super-vision
40	11	WSEN	I	X	Enable DSP and DC/DC converter
41	10	WRDY	O	LV	If WSEN=0: Valid clock input at CLKI If WSEN=1: Clock synthesizer PLL locked
42	9	AVDD	Supply	VDD	Supply for analog circuits
43	8	CLKI	I	X	Clock input
44	7	AVSS	Supply	VSS	Ground supply for analog circuits

4.3. Pin Descriptions

4.3.1. Power Supply Pins

Connection of all power supply pins is mandatory for the function of the MAS 3506D.

VDD SUPPLY
VSS SUPPLY

The VDD/VSS pair is internally connected with all digital modules of the MAS 3506D.

XVDD SUPPLY
XVSS SUPPLY

The XVDD/XVSS pins are the supply lines for the pin output buffers.

AVDD SUPPLY
AVSS SUPPLY

The AVDD/AVSS pair is internally connected with the analog blocks of the MAS 3506D, i.e. clock synthesizer and supply voltage supervision circuits.

4.3.2. DC/DC Converter Pins

DCEN DC/DC ENABLE IN

The DCEN input signal starts and enables the DC/DC converter operation.

DCSG SUPPLY

The DC converter Signal Ground pin is used as a basepoint for the internal switching transistor of the DC/DC converter. It must always be connected to ground.

DCSO OUT

DCSO is an open drain output and should be connected with external circuitry (inductor/diode) to start the DC/DC converter. When the DC/DC converter is not used, it has to be connected to VSS.

VSENS IN

The VSENS pin is the input for the DC/DC converter feedback loop. It must be connected directly with the Schottky diode and the capacitor as shown in Fig. 2–5 on page 10.
When the DC/DC converter is not used, it has to be connected to VDD.

4.3.3. Control Lines

I2CC SCL IN/OUT
I2CD SDA IN/OUT

Standard I^2C control lines. Normally there are pull-up resistors from each line to VDD.

4.3.4. Parallel Interface Control Lines

PR IN
PCS IN
RTR OUT
RTW OUT
EOD OUT

PIO handshake lines. Their use depends on the actual firmware on the MAS 3506D. Usage of these lines in the standard WorldSpace configuration is not planned.

4.3.5. Parallel Interface Data Lines

General purpose Parallel IO pins. The information of the input and output signals may also be read from Register $c8_{hex}$ (please refer to Table 3–10 in Section Section 3.4. on page 20).

PI19 BC-FRAME-TOGGLE OUT

The BC-FRAME-TOGGLE output toggles its state after each correctly decoded Broadcast Channel Frame (432 ms). This pin can be used for monitor the proper function of the system.

PI18 $\overline{\text{BCINENABLE}}$ IN

PI18 is used as input pin to sense the status of the $\overline{\text{BCINENABLE}}$ line at the WorldSpace connector. On low input level the alternative BC-input lines SIC*, SII* and SID* are activated and SIC, SII, SID are deactivated.

PI17 RESERVED IN/OUT
PI16 SIC* IN
PI15 SII* IN
PI14 SID* IN

The SIC*, SID*, and SII* may be configured as alternative serial input lines in order to support alternative serial digital sources. SID* (PI14) is used as Broadcast Channel data input from the Broadcast Channel I/O interface.

PI13 BC-FRAME-SYNC OUT

The BC-FRAME-SYNC is reset after POR and set to ‘1’ after each correctly decoded SCH. It will only be cleared if the controller reads out SCH information from the MAS 3506D.

PI12 BC-SYNC OUT

The BC-SYNC is set, if the MAS 3506D is in the state of proper decoding of the Broadcast Channel bit-stream.

PI8 DECODING-ERROR OUT

The Decoding-Error pin is activated, if during decoding of the Broadcast Channel, the MPEG frame an error occurs or if no input bitstream is applied.

PI4 MPEG-FRAME-SYNC IN

The MPEG-FRAME-SYNC signal indicates that an MPEG header has been decoded properly and the internal MPEG decoder is in a synchronized state. The MPEG-FRAME-SYNC signal is inactive after Power-On Reset and will be activated when a valid MPEG Layer 3 header has been recognized. The signal will be cleared if the ancillary data information is read out by the controller via I^2C interface.

PI3 AUD-SW IN

The AUD-SW input may sense the headphone jack and deposit its information in Bit 3 of register $c8_{hex}$ (please refer to Table 3–10 on page 20.) This way the controller can get the information weather a loud-speaker or a headphone should be supplied and can set the BAS_INVR bit in DRD 3515A’s register GLB_CONFIG accordingly.

PI2 RESERVED IN
PI1 RESERVED IN
PI0 RESERVED IN

4.3.6. Voltage Supervision And Other Functions

CLKI IN
CLKO OUT

CLKI and CLKO are the input and output clock lines to be connected to the DRD 3515A. CLKI expects 14.725 MHz, CLKO delivers 24.576 MHz synchronous to the audio data stream.

PUP POWER UP OUT

The PUP output indicates that the power supply voltage exceeds its minimal level (software adjustable).

WSEN DSP ENABLE IN

WSEN enables DSP and DC/DC-converter operation. It must also be set to activate the control interface e.g. to reprogram the DC/DC-converter.

WRDY OUT

WRDY has two functionalities depending on the state of the WSEN signal.

If WSEN = 0, it indicates that a valid clock has been recognized at the CLKI clock input.

If WSEN = 1, the WRDY output will be set to ‘0’ until the internal clock synthesizer has locked to the incoming audio data stream, and thus, the CLKO clock output signal is valid.

4.3.7. Serial Input Interface

SID IN
SII IN
SIC IN

Data, Frame Indication and Clock line of the serial input interface. The SII line should be connected with VSS in the standard WorldSpace mode. The SID and SIC lines are used for the Broadcast Channel input.

4.3.8. Serial Output Interface

SOD **OUT**
SOI **OUT**
SOC **OUT**

Data, Frame Indication and Clock line of the serial audio output interface (I^2S). The SOC line can be deactivated, if only the DRD 3515A D/A converter is connected. The SOI indicates, whether the left or the right audio sample is transmitted. In the default setting a left audio sample always corresponds to SOI = low.

4.3.9. Miscellaneous

$\overline{\text{POR}}$ **IN**

The Power-On Reset pin is used to reset the digital parts of the MAS 3506D.

TE **IN**

The TE pin is for production test only and must be connected with VSS in all applications.

4.4. Pin Configuration

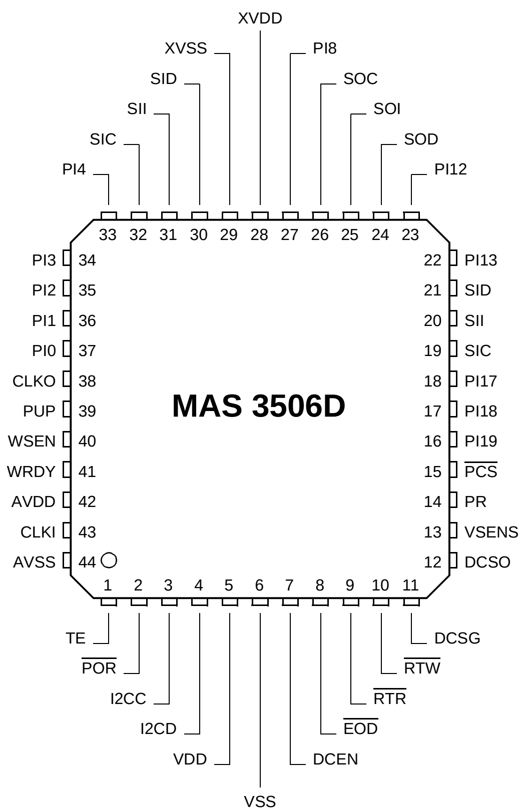


Fig. 4–3: PMQFP44 package

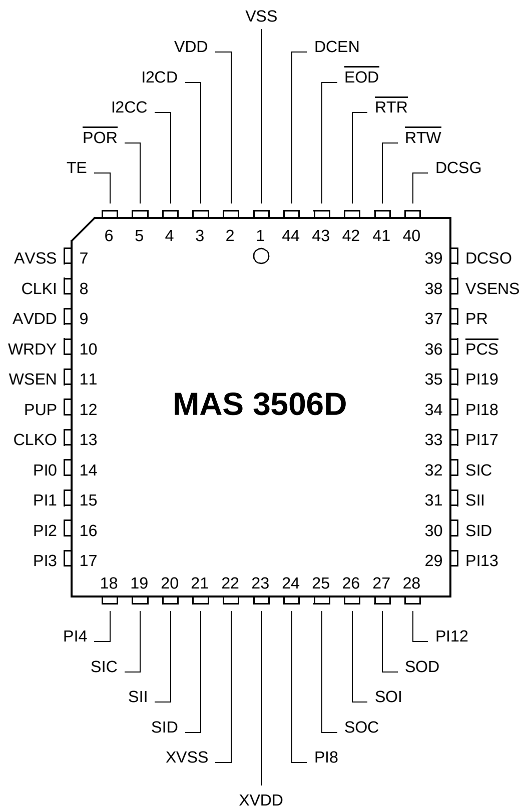


Fig. 4–4: PLCC44 package

4.5. Internal Pin Circuits

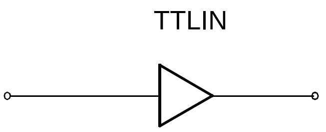


Fig. 4–5: Input pins $\overline{\text{PCS}}$, PR

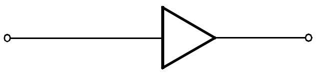


Fig. 4–6: Input pin TE, DCEN

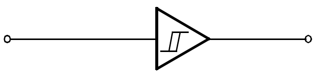


Fig. 4–7: Input pins WSEN, $\overline{\text{POR}}$

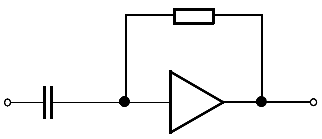


Fig. 4–8: Input pin CLKI

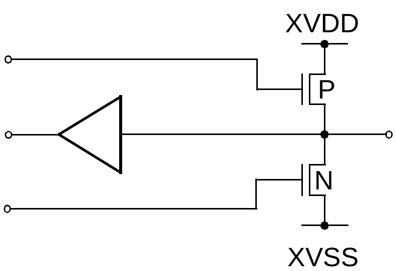


Fig. 4–9: Input/Output pins PI0...PI4, PI8, SOC, SOI, SOD, PI12...PI19

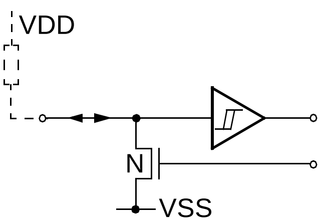


Fig. 4–10: Input/Output pins I2CC, I2CD

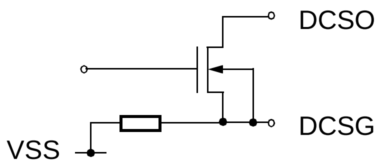


Fig. 4–11: Input/Output pins DCSO, DCSG

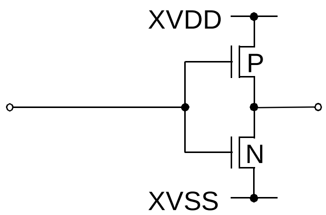


Fig. 4–12: Output pins WRDY, $\overline{\text{RTW}}$, $\overline{\text{EOD}}$, $\overline{\text{RTR}}$, CLKO, PUP

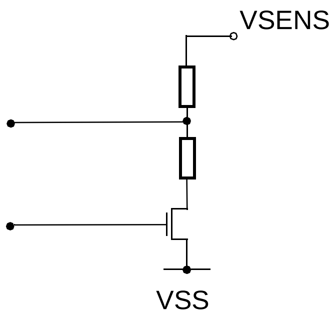


Fig. 4–13: Input pin VSENS

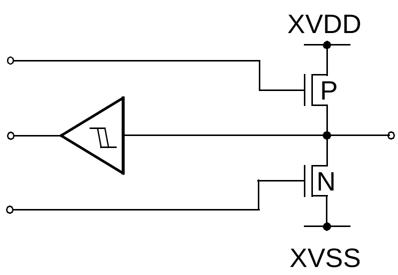


Fig. 4–14: Input/Output pins SIC, SII, SID

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient operating temperature		–40	85	°C
T_S	Storage temperature		–40	125	°C
P_{MAX}	Power dissipation	VDD, XVDD, AVDD		600	mW
V_{SUP}	Supply voltage	VDD, XVDD, AVDD		5.5	V
V_{Idig}	Input voltage, all digital inputs		–0.3	V_{SUP} +0.3	V
I_{Idig}	Input current, all digital inputs		–20	+20	mA
I_{Out}	Current, all digital output			0.5	A
I_{OutDC}	Current	DCSO		1.5	A
V_{II2C}	Input voltage, I^2C-Pins	I2CC, I2CC	–0.3	5.5	V

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient temperature range		–40		85	°C
V_{SUP}	Supply voltage	VDD, XVDD, AVDD	2.7	3.0	3.6	V
Reference Frequency Generation						
CLK_F	Clock frequency	CLKI		14.725		MHz
CLK_{I_V}	Clock input voltage		0		V_{SUP}	V
CLK_{Amp}	Clock amplitude		0.5			V_{pp}

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Levels						
I_{IL27}	Input low voltage at V_{SUP} = 2.7 V ... 3.6 V	$\overline{\text{POR}}$ I2CC, I2CD, DCEN, WSEN			0.4	V
I_{IH36}	Input high voltage at V_{SUP} = 2.7 V ... 3.6 V		1.8			V
I_{IH33}	Input high voltage at V_{SUP} = 2.7 V ... 3.3 V		1.7			V
I_{IH30}	Input high voltage at V_{SUP} = 2.7 V ... 3.0 V		1.6			V
I_{ILD}	Input low voltage	PI<i>[1], SII, SIC, SID, PR, PCS, TE,			0.4	V
I_{IHD}	Input high voltage		$V_{SUP}-0.5$			V
T_{rf}	Rise/fall time of digital inputs	PI<i>, SII, SIC, SID, PR, PCS, CLKI			10	ns
D_{cycle}	Duty cycle of digital clock inputs	SIC, CLKI	40	50	60	%
DC-DC converter external circuitry						
C_1	Blocking capacitor (< 100 mΩ ESR)[2]	VSENS, DCSG		330		µF
V_F	Schottky diode forward voltage[3]	DCSO, VSENS		0.35		V
L	Inductance of ferrite ring core coil[4]	DCSO		22		µH

[1] i = 0 to 4, 8 , 12 to 19
[2] Sanyo Oscon 6SA330M (distributed by Endrich Bauelemente, D-72202 Nagold-Iselshausen)
[3] ZETEX ZMCS1000 (distributed by ZETEX, D-81673 München), standard Schottky 1N5817
[4] C8 R/4L, SDS0604 (distributed by Endrich Bauelemente, see above)

4.6.3. Characteristics

at T = T_A, V_{SUP} = 2.7 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 3.5 V, CLK_F = 14.725 MHz, duty cycle = 50%

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage							
I_{SUP}	Current consumption	VDD, XVDD, AVDD		32		mA	2.7 V, sampling frequency ≥ 32kHz
				17		mA	2.7 V, sampling frequency ≤ 24 kHz
				11		mA	2.7 V, sampling frequency ≤ 12 kHz
Digital Outputs and Inputs							
V_{DOL}	Output low voltage	SOI[1], SOC[1], SOD[1], $\overline{EOD}$, $\overline{RTR}$, RTW, WRDY, PUP, CLKO PI<i>			0.3	V	I_{load} = 6mA
V_{DIH}	Output high voltage		V_{SUP}– 0.3			V	I_{load} = 6mA
Z_{DigI}	Input impedance	PI<i>, SII, SIC, SID, PR, PCS, CLKI			7	pF	
I_{DLeak}	Digital input leakage current		–1		1	µA	0 V < V_{pin} < V_{SUP}

[1] in low impedance mode

4.6.3.1. I^{2}C Characteristics

at T = T_A, V_{SUP} =2.7 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 3.0 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{ON}	Output resistance	I2CC, I2CD			60	Ω	I_{load} = 5 mA, V_{SUP} = 2.7 V
f_{I2C}	I^{2}C bus frequency	I2CC			400	kHz	
t_{I2C1}	I^{2}C Start condition setup time	I2CC, I2CD	300			ns	
t_{I2C2}	I^{2}C Stop condition setup time	I2CC, I2CD	300			ns	
t_{I2C3}	I^{2}C clock low pulse time	I2CC	1250			ns	
t_{I2C4}	I^{2}C clock high pulse time	I2CC	1250			ns	
t_{I2C5}	I^{2}C data hold time before rising edge of clock	I2CC	80			ns	
t_{I2C6}	I^{2}C data hold time after falling edge of clock	I2CC	80			ns	
V_{I2COL}	I^{2}C output low voltage	I2CC, I2CD			0.3	V	I_{LOAD} = 5 mA
I_{I2COH}	I^{2}C output high leakage current	I2CC, I2CD			1	uA	V_{I2CH} = 3.6 V
t_{I2COL1}	I^{2}C data output hold time after falling edge of clock	I2CC, I2CD	20			ns	
t_{I2COL2}	I^{2}C data output setup time before rising edge of clock	I2CC, I2CD	250			ns	f_{I2C} = 400kHz
t_W	Wait time	I2CC, I2CD	0	0.5	4	ms	

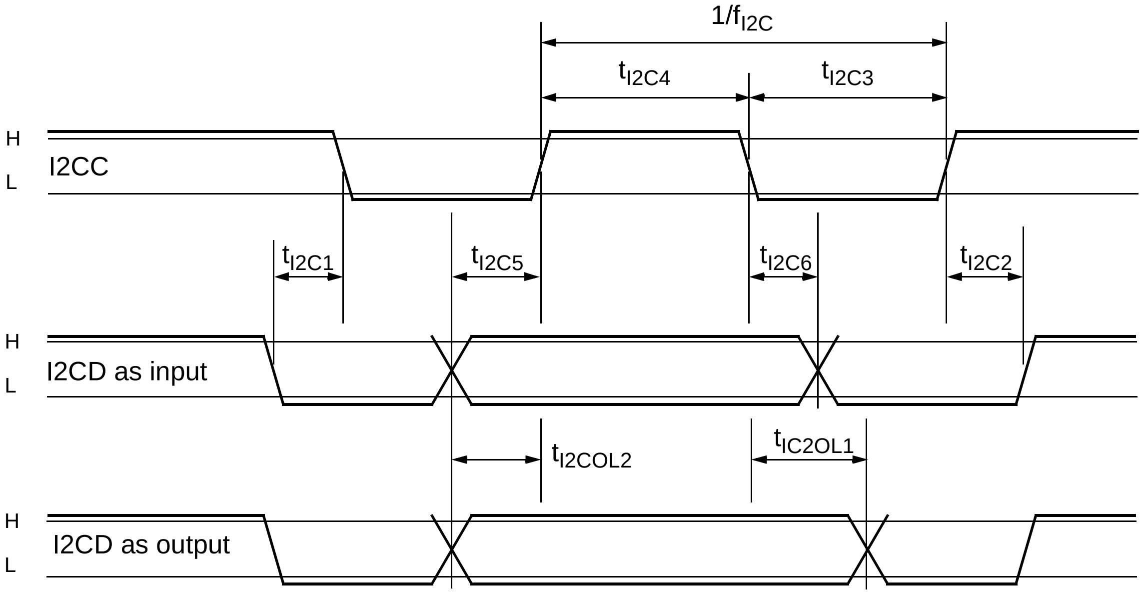


Fig. 4–15: I^{2}C timing diagram

4.6.3.2. Timing of PIO-Signals

Table 4–1: PIO Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{BCTP}	BC-frame toggle time	PI19		432		ms	

Behavior of the FRAME signals

The BC-FRAME-TOGGLE toggles its level from ’1’ to ’0’ and vice-versa every 432 ms. The BC-FRAME-SYNC signal is set to ’1’ after the internal decoding process for the Service Control Header has been finished for one frame. The signal could be used as an interrupt input for the controller that triggers the read out of the Service Control Header. As soon as the MAS 3506D has recognized the corresponding read command for the SCH, the BC-FRAME-SYNC is reset before sending the first data word. The time t_{read} depends on the response time of the controller. This behavior reduces the possibility of not recognizing the BC-FRAME-SYNC active state, if no controller interrupt line is available for this purpose.

A similar behavior is implemented for MPEG-FRAME-SYNC signal. However the frame period is restricted to the MPEG frame length, the reset is initiated by issuing a ’Read Ancillary MPEG Data’ command.

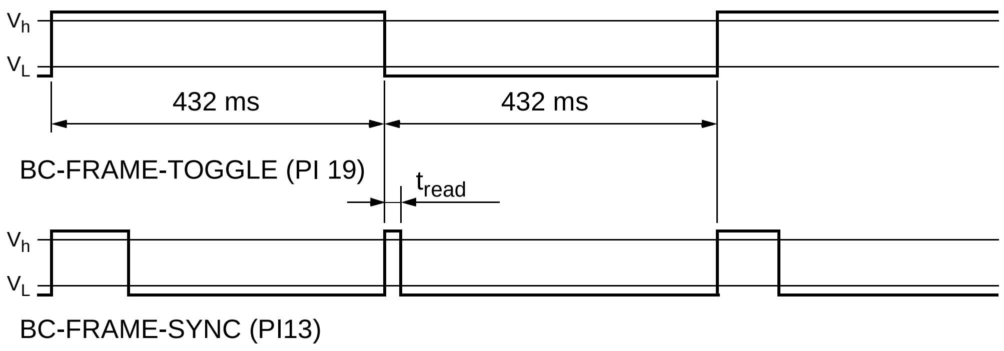


Fig. 4–16: Schematic timing of BC-FRAME signals

4.6.3.3. I²S Bus Characteristics – SDI

at T = T_A, V_{SUP} = 2.7 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 3.0 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I²S clock input clock period	SIC	480			ns	multimedia mode, mean data rate < 150 kbit/s
t_{SIIDS}	I²S data setuptime before falling edge of clock	SIC, SID	50		t_{SICLK}-100	ns	
t_{SIIDH}	I²S data hold time	SID	50			ns	
t_{bw}	Burst wait time	SIC, SID	480				

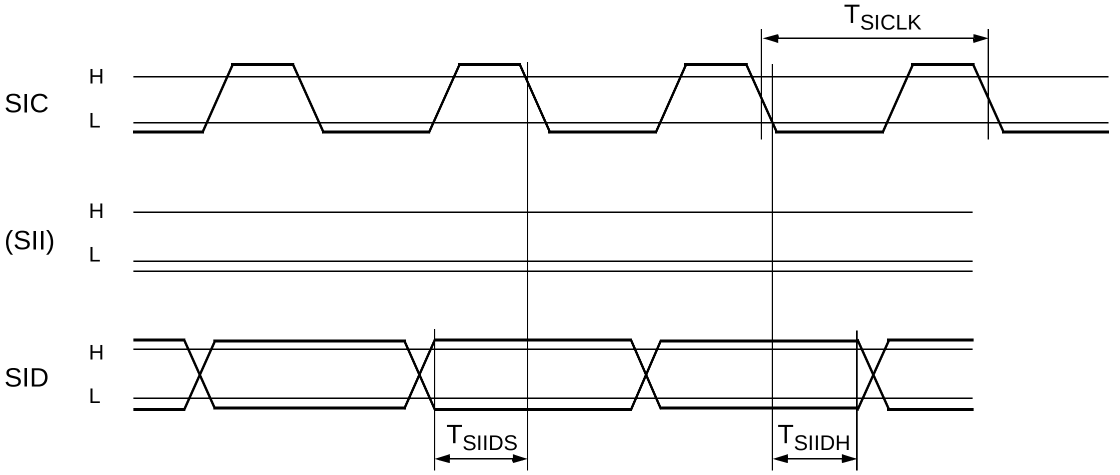


Fig. 4–17: Serial input

4.6.3.4. I²S Characteristics – SDO

at $T = T_A$, V_{SUP} = 2.7 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 3.0 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SOCLK}	I²S clock output period	SOC		325		ns	48 kHz Stereo 32 bit/sample
t_{SOISS}	I²S wordstrobe delay time after falling edge of clock	SOC, SOI	0			ns	
t_{SOODC}	I²S data delay time after falling edge of clock	SOC, SOD	0			ns	

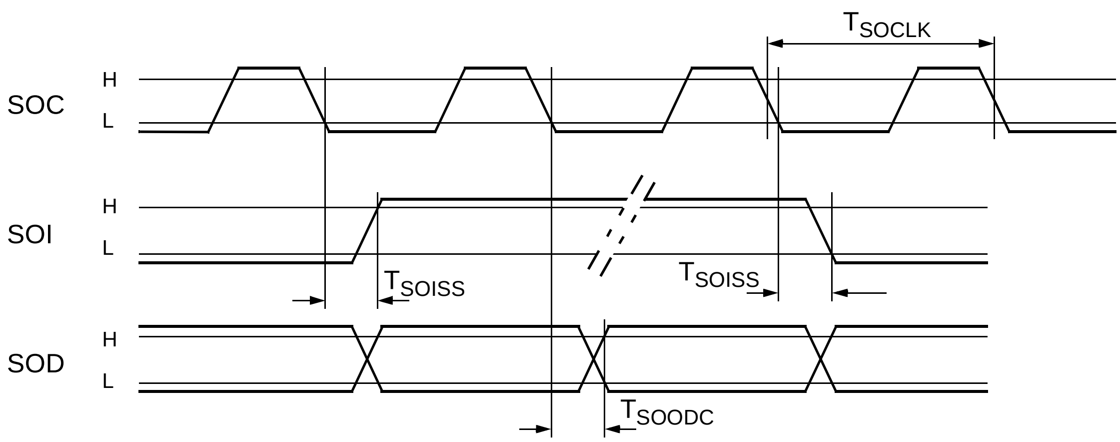


Fig. 4–18: Serial output

4.6.3.5. Firmware Characteristics

at $T = T_A$, V_{SUP} = 2.7 to 3.6 V, typ. values at T_A = 27°C, V_{SUP} = 3.0 V, CLK_F = 14.725 MHz, duty cycle = 50 %

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Synchronization Times						
t_{bcsync}	Synchronization on Broadcast Channel		216	432	ms	
$t_{mpgsync}$	Synchronization on MPEG bit streams		12..36	72	ms	f_s = 32 kHz, MPEG 2.5
Time constants						
t_{bcloop}	Buffer controlled loop time constant (see Fig. 2–2 on page 8)	5	8	10	s	step response
t_{anc}	Validity of ancillary data after rising edge of MPEG-FRAME-SYNC signal	6			ms	
t_{SCH}	Validity of SCH-data after rising edge of BC-FRAME-SYNC signal	400			ms	
Ranges						
PLLRange	Tracking range of sampling clock recovery PLL	–200		200	ppm	

4.6.4. DC/DC Converter Characteristics

at T = T_A, V_{SUP} = 3.0 V, CLK_F = 14.725 MHz, f_{sw} = 230 kHz, typ. values at T_A = +27 °C.
Unless otherwise noted: V_{OUT} = 3.0 V, V_{IN} = 1.2 V

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN1}	Minimum start-up input voltage	1)		0.9	1.1	V	I_{LOAD} = 0 mA DCCF = $08000 (Reset)
V_{IN2}	Minimum operating input voltage	1)		0.6	0.9	V	I_{LOAD} = 55 mA, DCCF = $08000 (Reset)
				1.3	1.8	V	I_{LOAD} = 250 mA, DCCF = $08000 (Reset)
V_{OUT}	Output voltage range Bits 16..14, Bit 9 of DCCF Register (hex): 1C000 18000 14000 10000 0C000 08000 04000 00000 1C200 18200 14200 10200 0C200 08200 04200 00200	VSENS		 3.567 3.460 3.354 3.248 3.144 3.039 2.935 2.831 2.729 2.625 2.524 2.422 2.321 2.219 2.118 2.017		V	VIN = 1.2 V ILOAD = 50 mA
V_{OTOL}	Output voltage tolerance	VSENS	–3.6		3.6	%	I_{LOAD} = 50 mA T_j = 27 °C V_{IN} = 1.2 V
I_{LOAD1}	Output current	VSENS			150	mA	V_{IN} = 0.9...1,5 V
I_{LOAD2}					250	mA	V_{IN} = 1.8...3.0 V
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line regulation	VSENS		0.35		%/V	I_{LOAD} = 50 mA
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line regulation	VSENS		0.7		%/V	I_{LOAD} = 250 mA, V_{OUT} = 3.5 V, V_{IN} = 2.4 V
dV_{OUT}/V_{OUT}	Load regulation	VSENS		–0.5		%	I_{LOAD} = 50...150 mA
dV_{OUT}/V_{OUT}	Load regulation	VSENS		–0.5		%	I_{LOAD} = 50...250 mA, V_{OUT} = 3.5 V, V_{IN} = 2.4 V

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
h_{max}	Maximum efficiency			90		%	V_{IN} = 3.0 V, V_{OUT} = 3.5 V
I_{SUPPLY}	Supply current	VSENS		1.1	5	mA	V_{IN} = 3.0 V, I_{LOAD} = 0, includ. switch current
$I_{L,MAX}$	Inductor current limit	DCSO, DCSG		1.0	1.4	A	
R_{ON}	Switch on-resistance	DCSO, DCSG		0.4		Ω	
I_{LEAK}	Switch leakage current	DCSO, DCSG		0.1	1	µA	T_j = 27 °C, converter = off; I_{LOAD} = 0 µA
f_{SW}	Switch frequency	DCSO, DCSG	156	230	460	kHz	Depending on DCCF
t_{START}	Start-up zime asserting to PUP	DCEN, PUP		8		ms	V_{IN} = 1.0 V, I_{LOAD} = 1 mA, PUPLIM = 010 (Reset)
$f_{STARTUP}$	VSENSE	DCSO		250		kHz	VSENS < 1.9 V

[1)] All measurements are made with a C8 R/4L 20 µH, 25 mΩ ferrite ring-core coil, Zetex ZLMCS1000 Schottky diode, and Sanyo/Oscon 6SA330M 330 µF, 25 mΩ ESR capacitors at input and output.

4.6.5. Typical Performance Characteristics

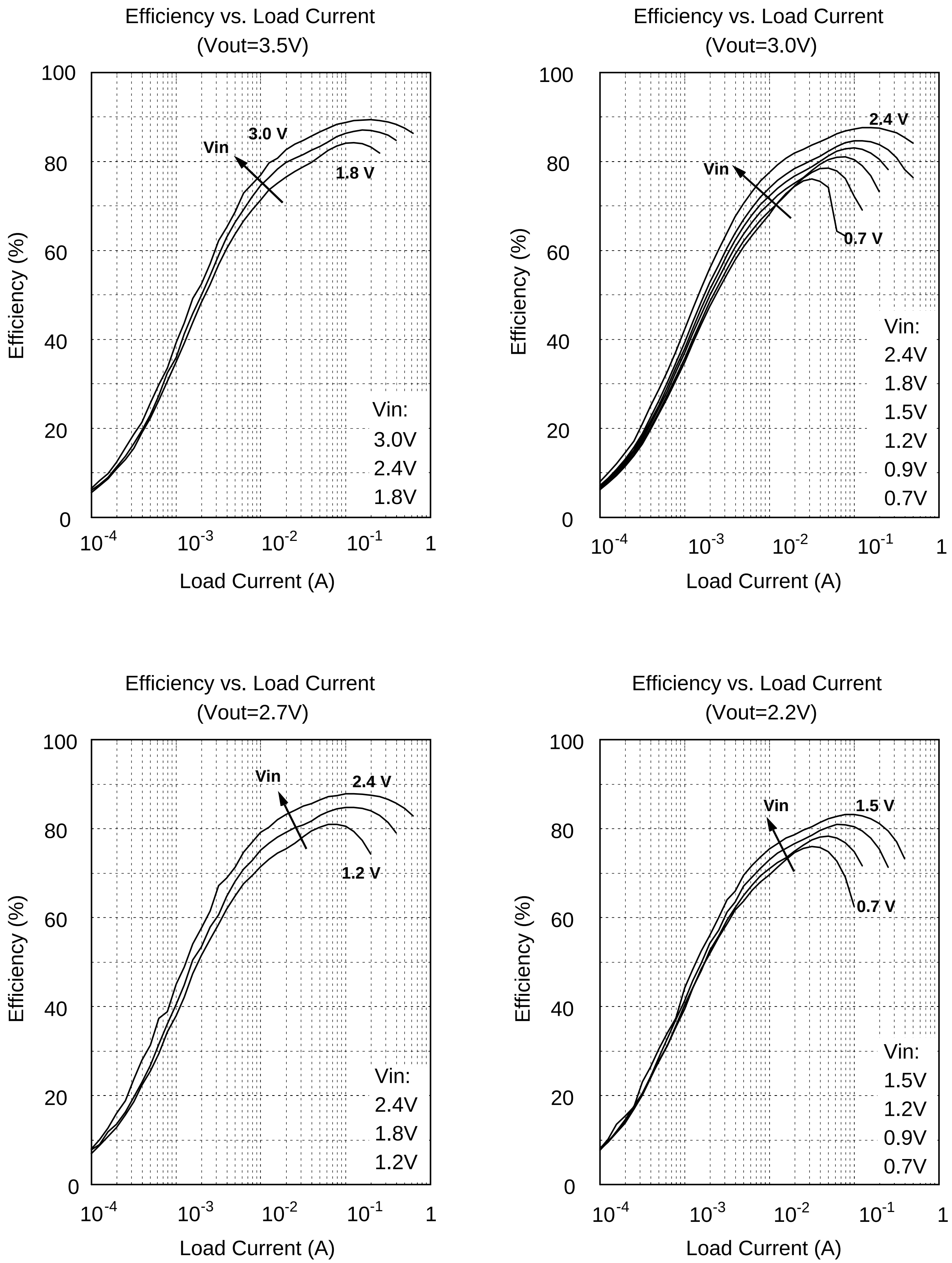


Fig. 4–19: Efficiency vs. Load Current

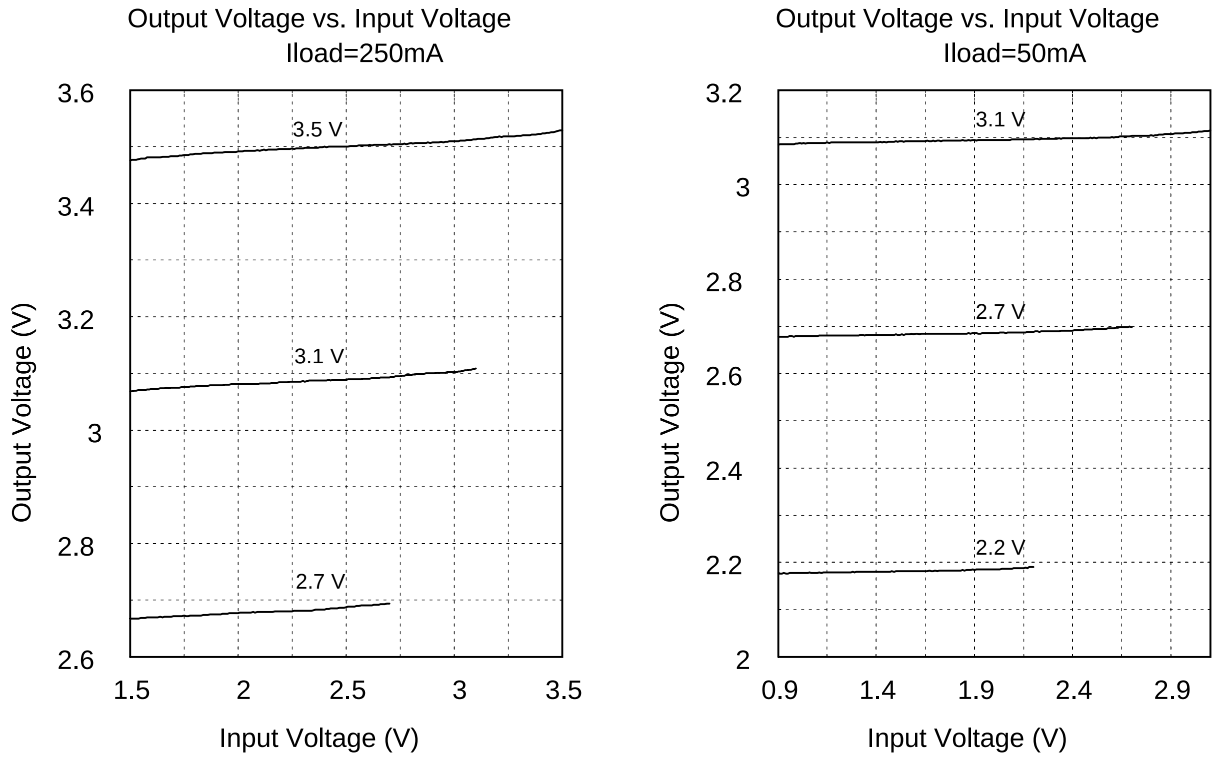


Fig. 4–20: Output Voltage vs. Input Voltage

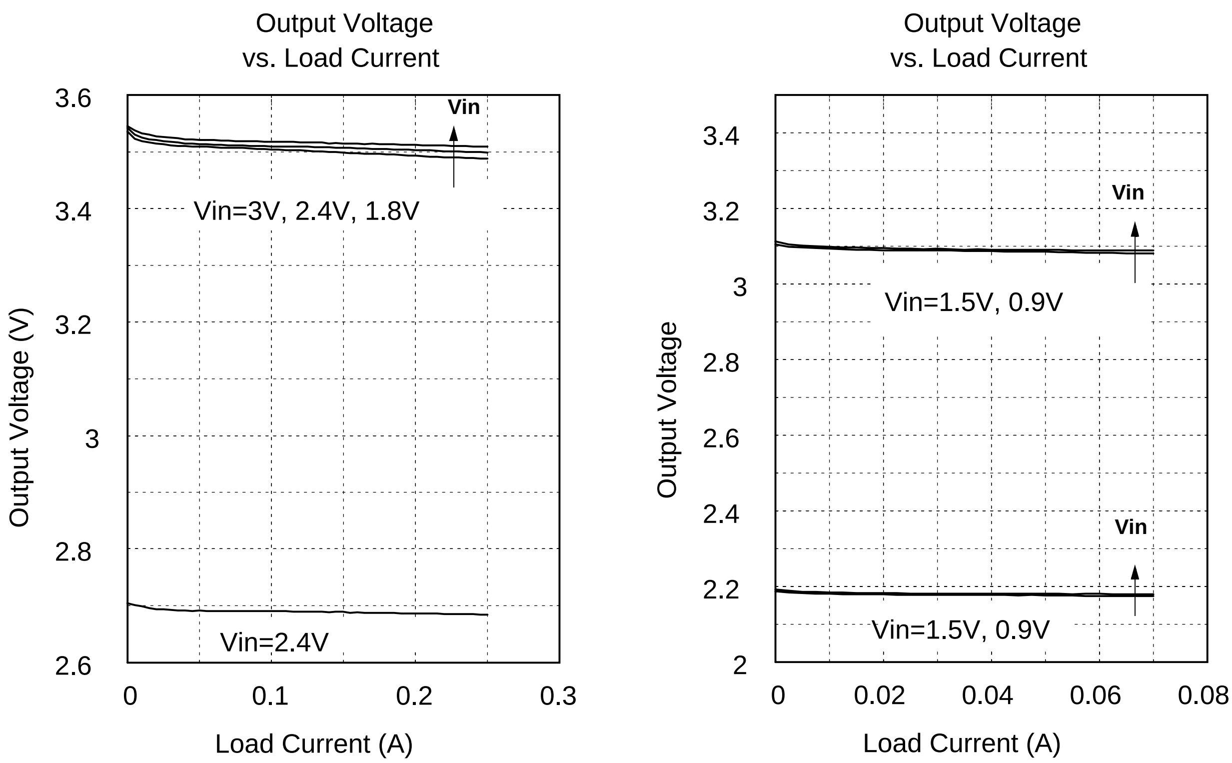


Fig. 4–21: Output Voltage vs. Load Current

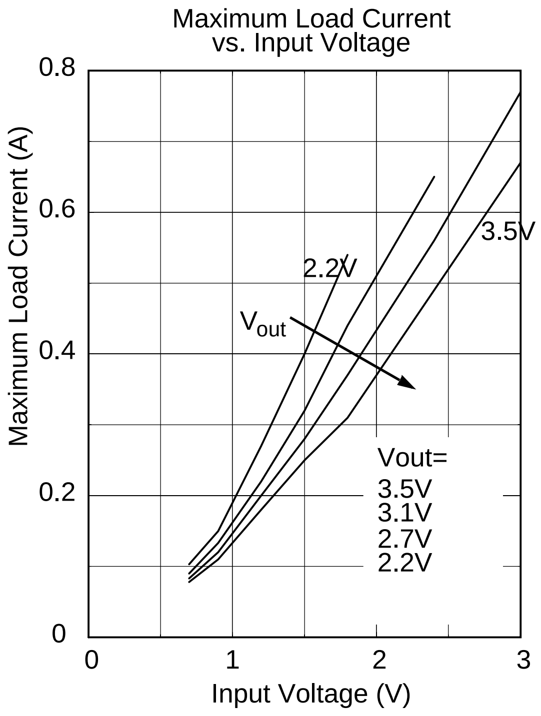


Fig. 4–22: Maximum Load Current vs. Input Voltage

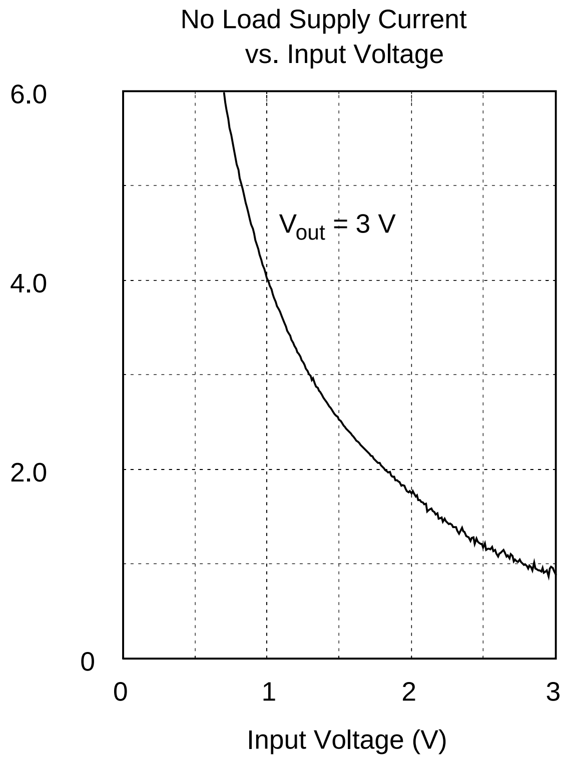
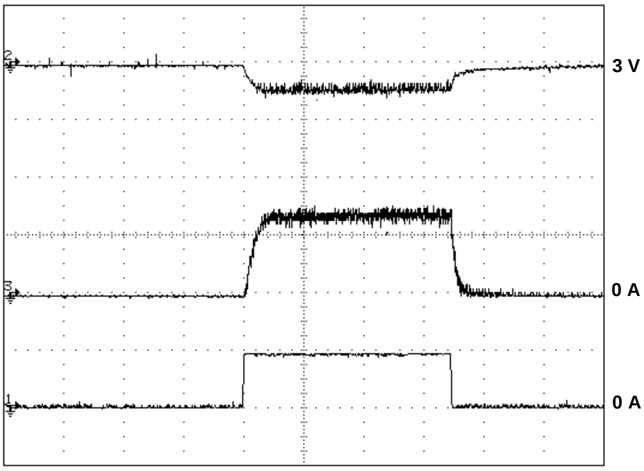


Fig. 4–23: No Load Supply Current vs. Input Voltage

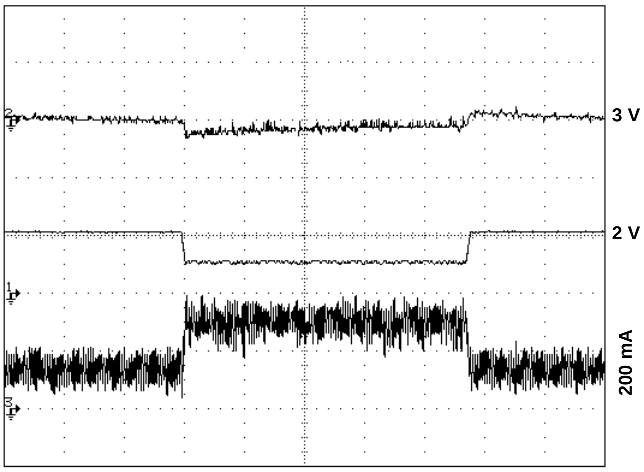


500.00 µs/Div

V_{in} = 1.2 V; V_{out} = 3 V

1	Load Current	200.0 mA/Div
2	Output Voltage	100.0 mV/Div / AC-coupled
3	Inductor Current	500.0 mA/Div

Fig. 4–24: Load Transient-Response

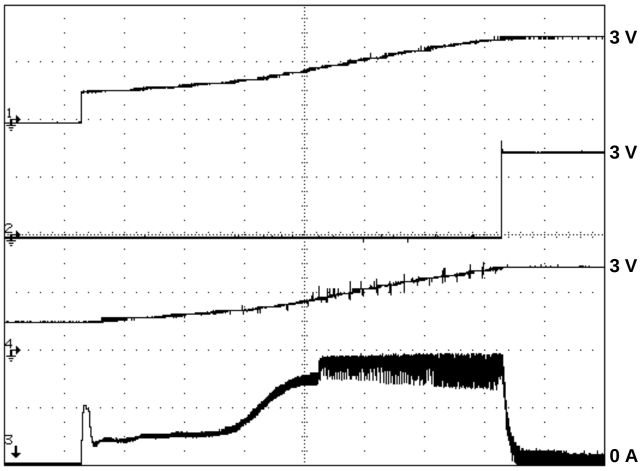


5.00 ms/Div

I_{load} = 100 mA; V_{out} = 3 V

1	V_{in}	2.000 V/Div
2	Output Voltage	50.00 mV/Div / AC-coupled
3	Inductor Current	200.0 mA/Div

Fig. 4–25: Line Transient-Response



500 µs/Div

V_{in} = 1 V; I_{load} = 0 mA

1	V (DCEN)	2.000 V/Div
2	V (PUP)	2.000 V/Div
3	Inductor Current	500.0 mA/Div
4	Output Voltage	2.000 V/Div

Fig. 4–26: Startup Waveform

5. Data Sheet History

1. Preliminary data sheet: “MAS 3506D WorldSpace Broadcast Channel Audio Decoder, July 25, 2001, 6251-433-1PD. First release of the preliminary data sheet.

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