Section 18 Electrical Characteristics

18.1 Absolute Maximum Ratings

Table 18-1 lists the absolute maximum ratings.

Table 18-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage (except port 7)	V_{IN}	–0.3 to V_{CC} +0.3	V
Input voltage (port 7)	V_{IN}	–0.3 to AV_{CC} +0.3	V
Reference voltage	V_{REF}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
Storage temperature	T_{stg}	Wide-range specifications: –40 to +85	°C
		–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

18.2 Electrical Characteristics

18.2.1 DC Characteristics

Table 18-2 lists the DC characteristics. Table 18-3 lists the permissible output currents.

Table 18-2 DC Characteristics

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$, PB_0 to PB_3	V_T^-	1.0	—	—	V	
		V_T^+	—	—	V_{CC} × 0.7	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} × 0.7	—	V_{CC} + 0.3	V	
	Port 7		2.0	—	AV_{CC} + 0.3	V	
	Ports 4, 5, 6, 9, C, $P8_3$, $P8_4$, PB_4 to PB_7, D_{15} to D_8		2.0	—	V_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, ports 4, 5, 6, 7, 9, C, $P8_3$, $P8_4$, PB_4 to PB_7, D_{15} to D_8		–0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 μA
			3.5	—	—	V	I_{OH} = –1 mA

Note: * If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 18-2 DC Characteristics (cont)

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 5 and B, A_{19} to A_0		—	—	1.0	V	I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 2.6 mA
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD_2 to MD_0	$\lvert I_{IN} \rvert$	—	—	1.0	μA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	Port 7		—	—	1.0	μA	V_{IN} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 4, 5, 6, 8 to C, A_{19} to A_0, D_{15} to D_8	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	$\overline{RESO}$		—	—	10.0	μA	V_{IN} = 0.5 to V_{CC} – 0.5 V
Input pull-up current	Ports 4 and 5	$-I_P$	50	—	300	μA	V_{IN} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V, f = 1 MHz, T_a = 25°C
	All input pins except NMI		—	—	15		
Current dissipation*2	Normal operation	I_{CC}	—	35	55	mA	f = 10 MHz
			—	40	65	mA	f = 12 MHz
			—	50	80	mA	f = 16 MHz
	Sleep mode		—	25	40	mA	f = 10 MHz
			—	30	45	mA	f = 12 MHz
			—	35	60	mA	f = 16 MHz
	Standby mode*3		—	0.01	5.0	μA	T_a ≤ 50°C
			—	—	20.0	μA	50°C < T_a

Notes: 1. If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IHmin} = V_{CC} – 0.5 V and V_{ILmax} = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for V_{RAM} ≤ V_{CC} < 4.5 V, V_{IHmin} = V_{CC} × 0.9, and V_{ILmax} = 0.3 V.

Table 18-2 DC Characteristics (cont)

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	μA	
Reference current	During A/D conversion	AI_{CC}	—	0.3	0.6	mA	V_{REF} = 5.0 V
	Idle		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5$ V and V_{ILmax} = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} < V_{CC} < 4.5$ V, $V_{IHmin} = V_{CC} \times 0.9$, and V_{ILmax} = 0.3 V.

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$, PB_0 to PB_3	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 4, 5, 6, 9, C, $P8_3$, $P8_4$, PB_4 to PB_7, D_{15} to D_8		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	

Note: * If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 18-2 DC Characteristics (cont)

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 4, 5, 6, 7, 9, C, $P8_3$, $P8_4$ PB_4 to PB_7, D_{15} to D_8		–0.3	—	$V_{CC} \times 0.2$	V	V_{CC} < 4.0 V
					0.8	V	V_{CC} = 4.0 to 5.5 V
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	I_{OH} = –200 μA
			$V_{CC} - 1.0$	—	—	V	$V_{CC} \leq 4.5$ V I_{OH} = –1 mA.
			3.5	—	—	V	4.5 V < $V_{CC} \leq 5.5$ V I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 5 and B, A_{19} to A_0		—	—	1.0	V	$V_{CC} \leq 4$ V I_{OL} = 8 mA, 4 V < $V_{CC} \leq 5.5$ V I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 2.6 mA
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD_2 to MD_0	$\lvert I_{IN} \rvert$	—	—	1.0	μA	V_{IN} = 0.5 to $V_{CC} - 0.5$ V
	Port 7		—	—	1.0	μA	V_{IN} = 0.5 to $AV_{CC} - 0.5$ V
Three-state leakage current (off state)	Ports 4, 5, 6, 8 to C, A_{19} to A_0, D_{15} to D_8	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{IN} = 0.5 to $V_{CC} - 0.5$ V
	$\overline{RESO}$		—	—	10.0	μA	V_{IN} = 0.5 to $V_{CC} - 0.5$ V
Input pull-up current	Ports 4 and 5	$-I_P$	10	—	300	μA	V_{CC} = 2.7 V to 5.5 V, V_{IN} = 0 V

Note: * If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 18-2 DC Characteristics (cont)

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V f = 1 MHz T_a = 25°C
	All input pins except NMI		—	—	15		
Current dissipation*2	Normal operation	I_{CC}*4	—	30 (5.0 V)	36.2 (5.5 V)	mA	f = 8 MHz
	Sleep mode		—	20 (5.0 V)	27.4 (5.5 V)	mA	f = 8 MHz
	Standby mode*3		—	0.01	5.0	μA	T_a ≤ 50°C
			—	—	20.0	μA	50°C < T_a
Analog power supply current	During A/D conversion	AI_{CC}	—	1.0	2.0	mA	AV_{CC} = 3.0 V
			—	1.2	—	mA	AV_{CC} = 5.0 V
	Idle		—	0.01	5.0	μA	
Reference current	During A/D conversion	AI_{CC}	—	0.2	0.4	mA	V_{REF} = 3.0 V
			—	0.3	—	mA	V_{REF} = 5.0 V
	Idle		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D converter is not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5$ V and V_{ILmax} = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, $V_{IHmin} = V_{CC} \times 0.9$, and V_{ILmax} = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
I_{CCmax} = 1.0 (mA) + 0.8 (mA/MHz · V) × V_{CC} × f [normal mode]
I_{CCmax} = 1.0 (mA) + 0.6 (mA/MHz · V) × V_{CC} × f [sleep mode]

Table 18-2 DC Characteristics (cont)

Conditions: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC},
$V_{SS} = AV_{SS}$ = 0 V*1, T_a = –20°C to +75°C (normalspecification product),
T_a = –40°C to +85°C (extended temperature range specification product)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port A, $P8_0$ to $P8_2$, PB_0 to PB_3	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 4, 5, 6, 9, C, $P8_3$, $P8_4$, PB_4 to PB_7, D_{15} to D_8		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	V_{CC} < 4.0 V
	NMI, EXTAL, Ports 4, 5, 6, 7, 9, C, $P8_3$, $P8_4$, PB_4 to PB_7, D_{15} to D_8		–0.3	—	$V_{CC} \times 0.2$	V	
					0.8		V_{CC} = 4.0 to 5.5 V
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	I_{OH} = –200 μA
			$V_{CC} - 1.0$	—	—	V	$V_{CC} \leq 4.5$ V I_{OH} = –1 mA
			3.5	—	—	V	4.5 V < $V_{CC} \leq 5.5$ V I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 5 and B, A_{19} to A_0		—	—	1.0	V	$V_{CC} \leq 4.0$ V, I_{OL} = 8 mA, 4.0 V< $V_{CC} \leq 5.5$V, I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 2.6 mA
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD_2 to MD_0	$\lvert I_{IN} \rvert$	—	—	1.0	μA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	Port 7		—	—	1.0	μA	V_{IN} = 0.5 to AV_{CC} – 0.5 V

Table 18-2 DC Characteristics (cont)

Conditions: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC},
$V_{SS} = AV_{SS}$ = 0 V*1, T_a = –20°C to +75°C (normalspecification product),
T_a = –40°C to +85°C (extended temperature range specification product)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Ports 4, 5, 6, 8 to C, A_{19} to A_0, D_{15} to D_8	$\|I_{TSI}\|$	—	—	1.0	μA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	$\overline{RESO}$		—	—	10.0	μA	
Input pull -up current	Ports 4 and 5	$-I_P$	10	—	300	μA	V_{CC} = 3.0 V to 5.5 V, V_{IN} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V
	All input pins except NMI		—	—	15	pF	f = 1MHz T_a = 25°C
Current dissipation*2	Normal operation	I_{CC}*4	—	38 (5.0 V)	45 (5.5 V)	mA	f = 10 MHz
	Sleep		—	27 (5.0 V)	34 (5.5 V)	mA	f = 10 MHz
	Standby*3-[		—	0.01	5.0	μA	$T_a \leq$ 50°C
			—	—	20.0		50°C < T_a
Analog power supply	During A/D conversion	AI_{CC}	—	1.0	2.0	mA	AV_{CC} = 3.0 V
			—	1.2	—		AV_{CC} = 5.0 V
	A/D conversion standby		—	0.01	5.0	μA	
Reference power supply current	During A/D conversion	AI_{CC}	—	0.2	0.4	mA	V_{REF} = 3.0 V
			—	0.3	—		V_{REF} = 5.0 V
	A/D conversion standby		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. When the A/D converter is not used, do not leave the AV_{CC}, V_{REF}, and AV_{SS} pins open. Connect the AV_{CC} and V_{REF} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. The current dissipation value is the value when all output pins are unloaded and the on-chip pull-up MOS is off under the following conditions: V_{IH} min = V_{CC} to 0.5 V, V_{IL} max = 0.5 V.

3. When $V_{RAM} \leq V_{CC}$ < 3.0 V, the value is for the case where V_{IH}min = V_{CC} × 0.9, and V_{IL}max = 0.3 V.

4. I_{CC} is dependent upon V_{CC} and f in accordance with the following formulas.
I_{CC}max = 1.0 (mA) + 0.8 (mA/MHz · V) × V_{CC} × f [normal mode]
I_{CC}max = 1.0 (mA) + 0.6 (mA/MHz · V) × V_{CC} × f [sleep mode]

Table 18-3 Permissible Output Currents

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 5 and B, A_{19} to A_0	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 32 pins including ports 5 and B and A_{19} to A_0	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	I_{OH}	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 18-3.
2. When driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 18-1 and 18-2.

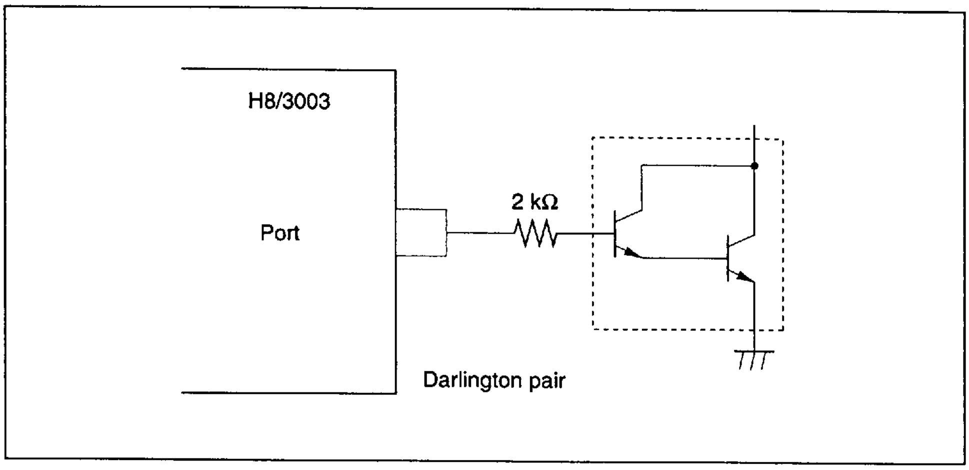


Figure 18-1 Darlington Pair Drive Circuit (Example)

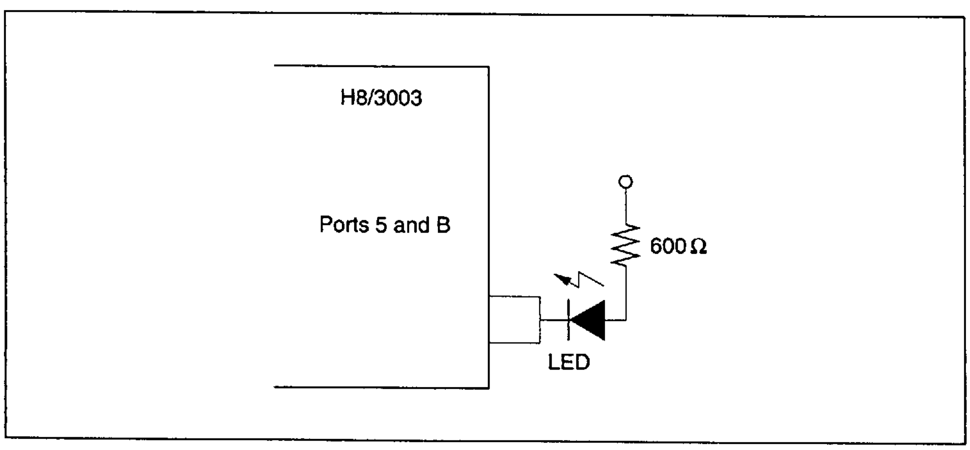


Figure 18-2 LED Drive Circuit (Example)

18.2.2 AC Characteristics

Bus timing parameters are listed in table 18-4. Control signal timing parameters are listed in table 18-5. Refresh controller bus timing parameters are listed in table 18-6. Timing parameters of the on-chip supporting modules are listed in table 18-7.

Table 18-4 Bus Timing

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C			
		8 MHz		10 MHz		16 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Clock cycle time	t_{CYC}	125	500	100	500	62.5	500	ns	Figure 18-4, Figure 18-5
Clock low pulse width	t_{CL}	40	—	30	—	20	—		
Clock high pulse width	t_{CH}	40	—	30	—	20	—		
Clock rise time	t_{CR}	—	20	—	15	—	10		
Clock fall time	t_{CF}	—	20	—	15	—	10		
Address delay time	t_{AD}	—	60	—	50	—	30		
Address hold time	t_{AH}	25	—	20	—	10	—		
Address strobe delay time	t_{ASD}	—	60	—	40	—	30		
Write strobe delay time	t_{WSD}	—	60	—	50	—	30		
Strobe delay time	t_{SD}	—	60	—	50	—	30		
Write data strobe pulse width 1	t_{WSW1}*	85	—	60	—	35	—		
Write data strobe pulse width 2	t_{WSW2}*	150	—	110	—	65	—		
Address setup time 1	t_{AS1}	20	—	15	—	10	—		
Address setup time 2	t_{AS2}	80	—	65	—	40	—		
Read data setup time	t_{RDS}	50	—	35	—	20	—		
Read data hold time	t_{RDH}	0	—	0	—	0	—		

Table 18-4 Bus Timing (cont)

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C			
		8 MHz		10 MHz		16 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Write data delay time	t_{WDD}	—	75	—	75	—	60	ns	Figure 18-4, Figure 18-5
Write data setup time 1	t_{WDS1}	60	—	65	—	35	—		
Write data setup time 2	t_{WDS2}	15	—	10	—	5	—		
Write data hold time	t_{WDH}	25	—	20	—	20	—		
Read data access time 1	t_{ACC1}*	—	110	—	100	—	55		
Read data access time 2	t_{ACC2}*	—	230	—	200	—	115		
Read data access time 3	t_{ACC3}*	—	55	—	50	—	25		
Read data access time 4	t_{ACC4}*	—	160	—	150	—	85		
Precharge time	t_{PCH}*	85	—	60	—	40	—		
Wait setup time	t_{WTS}	40	—	40	—	25	—	ns	Figure 18-6
Wait hold time	t_{WTH}	10	—	10	—	5	—		
Bus request setup ime	t_{BRQS}	40	—	40	—	40	—	ns	Figure 18-18
Bus acknowledge delay time 1	t_{BACD1}	—	60	—	50	—	30		
Bus acknowledge delay time 2	t_{BACD2}	—	60	—	50	—	30		
Bus-floating time	t_{BZD}	—	70	—	70	—	40		

Note is on next page.

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{cyc} - 78$ (ns)
$t_{ACC2} = 2.5 \times t_{cyc} - 83$ (ns)
$t_{ACC3} = 1.0 \times t_{cyc} - 70$ (ns)
$t_{ACC4} = 2.0 \times t_{cyc} - 90$ (ns)
$t_{WSW1} = 1.0 \times t_{cyc} - 40$ (ns)
$t_{WSW2} = 1.5 \times t_{cyc} - 38$ (ns)
$t_{PCH} = 1.0 \times t_{cyc} - 40$ (ns)

At 10 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{cyc} - 50$ (ns)
$t_{ACC2} = 2.5 \times t_{cyc} - 50$ (ns)
$t_{ACC3} = 1.0 \times t_{cyc} - 50$ (ns)
$t_{ACC4} = 2.0 \times t_{cyc} - 50$ (ns)
$t_{WSW1} = 1.0 \times t_{cyc} - 40$ (ns)
$t_{WSW2} = 1.5 \times t_{cyc} - 40$ (ns)
$t_{PCH} = 1.0 \times t_{cyc} - 40$ (ns)

At 16 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{cyc} - 39$ (ns)
$t_{ACC2} = 2.5 \times t_{cyc} - 41$ (ns)
$t_{ACC3} = 1.0 \times t_{cyc} - 38$ (ns)
$t_{ACC4} = 2.0 \times t_{cyc} - 40$ (ns)
$t_{WSW1} = 1.0 \times t_{cyc} - 28$ (ns)
$t_{WSW2} = 1.5 \times t_{cyc} - 28$ (ns)
$t_{PCH} = 1.0 \times t_{cyc} - 23$ (ns)

Table 18-5 Refresh Controller Bus Timing

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C			
		8 MHz		10 MHz		16 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RAS}$ delay time 1	t_{RAD1}	—	60	—	50	—	30	ns	Figure 18-7 to Figure 18-13
$\overline{RAS}$ delay time 2	t_{RAD2}	—	60	—	50	—	30		
$\overline{RAS}$ delay time 3	t_{RAD3}	—	60	—	50	—	30		
Row address hold time*	t_{RAH}	25	—	20	—	15	—		
$\overline{RAS}$ precharge time*	t_{RP}	85	—	70	—	40	—		
$\overline{CAS}$ to $\overline{RAS}$ precharge time*	t_{CRP}	85	—	70	—	40	—		
$\overline{CAS}$ pulse width	t_{CAS}	110	—	85	—	40	—		
$\overline{RAS}$ access time*	t_{RAC}	—	160	—	150	—	85		
Address access time	t_{AA}	—	105	—	75	—	55		
$\overline{CAS}$ access time	t_{CAC}	—	50	—	50	—	25		
Write data setup time 3	t_{WDS3}	75	—	50	—	40	—		
$\overline{CAS}$ setup time*	t_{CSR}	20	—	15	—	15	—		
Read strobe delay time	t_{RSD}	—	60	—	50	—	30		

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{cyc} - 38$ (ns) $\quad t_{CAC} = 1.0 \times t_{cyc} - 75$ (ns)

$t_{RAC} = 2.0 \times t_{cyc} - 90$ (ns) $\quad t_{CSR} = 0.5 \times t_{cyc} - 43$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 40$ (ns)

At 10 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{cyc} - 30$ (ns) $\quad t_{CAC} = 1.0 \times t_{cyc} - 50$ (ns)

$t_{RAC} = 2.0 \times t_{cyc} - 50$ (ns) $\quad t_{CSR} = 0.5 \times t_{cyc} - 35$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 30$ (ns)

At 16 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{cyc} - 16$ (ns) $\quad t_{CAC} = 1.0 \times t_{cyc} - 38$ (ns)

$t_{RAC} = 2.0 \times t_{cyc} - 40$ (ns) $\quad t_{CSR} = 0.5 \times t_{cyc} - 16$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 23$ (ns)

Table 18-6 Control Signal Timing

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C			
		8 MHz		10 MHz		16 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	200	—	ns	Figure 18-15
$\overline{RES}$ pulse width	t_{RESW}	10	—	10	—	10	—	tcyc	
$\overline{RESO}$ output delay time	t_{RESD}	—	100	—	100	—	100	ns	Figure 18-16
$\overline{RESO}$ output pulse width	t_{RESOW}	132	—	132	—	132	—	tcyc	
NMI setup time (NMI, $\overline{IRQ_7}$ to $\overline{IRQ_0}$)	t_{NMIS}	150	—	150	—	150	—	ns	Figure 18-17
NMI hold time (NMI, $\overline{IRQ_7}$ to $\overline{IRQ_0}$)	t_{NMIH}	10	—	10	—	10	—		
Interrupt pulse width (NMI, $\overline{IRQ_2}$ to $\overline{IRQ_0}$ when exiting software standby mode)	t_{NMIW}	200	—	200	—	200	—		
Clock oscillator settling time at reset (crystal)	t_{OSC1}	20	—	20	—	20	—	ms	Figure 18-19
Clock oscillator settling time in software standby (crystal)	t_{OSC2}	8	—	8	—	8	—		Figure 17-1

Table 18-7 Timing of On-Chip Supporting Modules

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

				Condition A		Condition B		Condition C			
				8 MHz		10 MHz		16 MHz			
Item			Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
DMAC	$\overline{DREQ}$ setup time		t_{DRQS}	40	—	30	—	30	—	ns	Figure 18-27
	$\overline{DREQ}$ hold time		t_{DRQH}	10	—	10	—	10	—		
	$\overline{TEND}$ delay time 1		t_{TED1}	—	100	—	50	—	50		Figure 18-25, Figure 18-26
	$\overline{TEND}$ delay time 2		t_{TED2}	—	100	—	50	—	50		
ITU	Timer output delay time		t_{TOCD}	—	100	—	100	—	100	ns	Figure 18-21
	Timer input setup time		t_{TICS}	50	—	50	—	50	—		
	Timer clock input setup time		t_{TCKS}	50	—	50	—	50	—		Figure 18-22
	Timer clock pulse width	Single edge	t_{TCKWH}	1.5	—	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TCKWL}	2.5	—	2.5	—	2.5	—		
SCI	Input clock cycle	Asyn-chronous	t_{Scyc}	4	—	4	—	4	—		Figure 18-23
		Syn-chronous	t_{Scyc}	6	—	6	—	6	—		
	Input clock rise time		t_{SCKR}	—	1.5	—	1.5	—	1.5		
	Input clock fall time		t_{SCKR}	—	1.5	—	1.5	—	1.5		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	

Table 18-7 Timing of On-Chip Supporting Modules (cont)

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

			Condition A		Condition B		Condition C			
			8 MHz		10 MHz		16 MHz			
Item		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
SCI	Transmit data delay time	t_{TXD}	—	100	—	100	—	100	ns	Figure 18-24
	Receive data setup time (synchronous)	t_{RXS}	100	—	100	—	100	—		
	Receive data hold time (synchronous)	t_{RXH}	100	—	100	—	100	—		
Ports and TPC	Output data delay time	t_{PWD}	—	100	—	100	—	100	ns	Figure 18-20
	Input data setup time (synchronous)	t_{PRS}	50	—	50	—	50	—		
	Input data hold time (synchronous)	t_{PRH}	50	—	50	—	50	—		

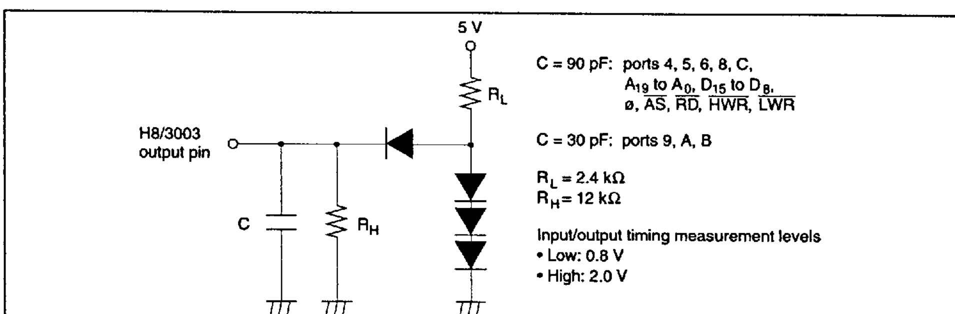


Figure 18-3 Output Load Circuit

18.2.3 A/D Conversion Characteristics

Table 18-8 lists the A/D conversion characteristics.

Table 18-8 A/D Converter Characteristics

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{REF} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

	Condition A			Condition B			Condition C			
	8 MHz			10 MHz			16 MHz			
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Resolution	10	10	10	10	10	10	10	10	10	bits
Conversion time	—	—	16.8	—	—	13.4	—	—	8.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*1	—	—	10*1	—	—	10*3	kΩ
	—	—	5*2	—	—	5*5	—	—	5*4	
Nonlinearity error	—	—	±6.0	—	—	±6.0	—	—	±3.0	LSB
Offset error	—	—	±4.0	—	—	±4.0	—	—	±2.0	LSB
Full-scale error	—	—	±4.0	—	—	±4.0	—	—	±2.0	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±8.0	—	—	±4.0	LSB

Notes: 1. The value is for 4.0 ≤ AV_{CC} ≤ 5.5.
2. The value is for 2.7 ≤ AV_{CC} < 4.0.
3. The value is for ø ≤ 12 MHz.
4. The value is for ø > 12 MHz.
5. The value is for 3.0 ≤ AV_{CC} < 4.0.

18.3 Operational Timing

This section shows timing diagrams.

18.3.1 Bus Timing

Bus timing is shown as follows:

- Basic bus cycle: two-state access

  Figure 18-4 shows the timing of the external two-state access cycle.

- Basic bus cycle: three-state access

  Figure 18-5 shows the timing of the external three-state access cycle.

- Basic bus cycle: three-state access with one wait state

  Figure 18-6 shows the timing of the external three-state access cycle with one wait state inserted.

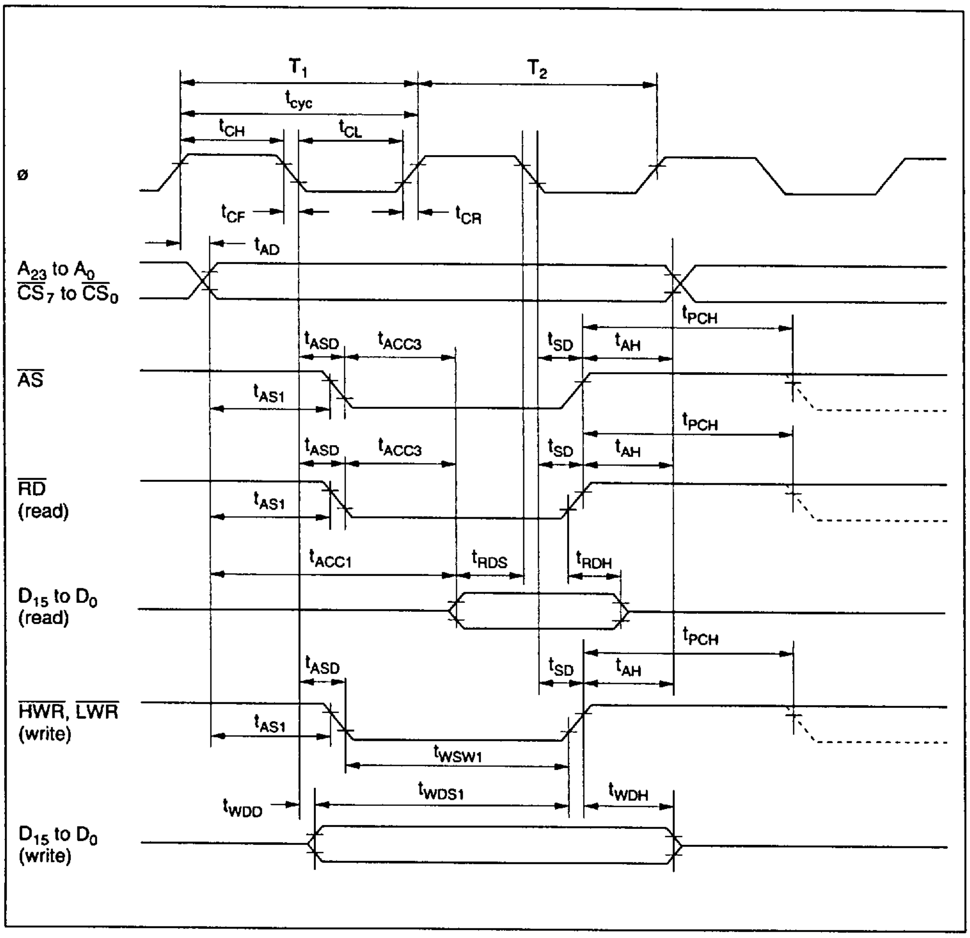


Figure 18-4 Basic Bus Cycle: Two-State Access

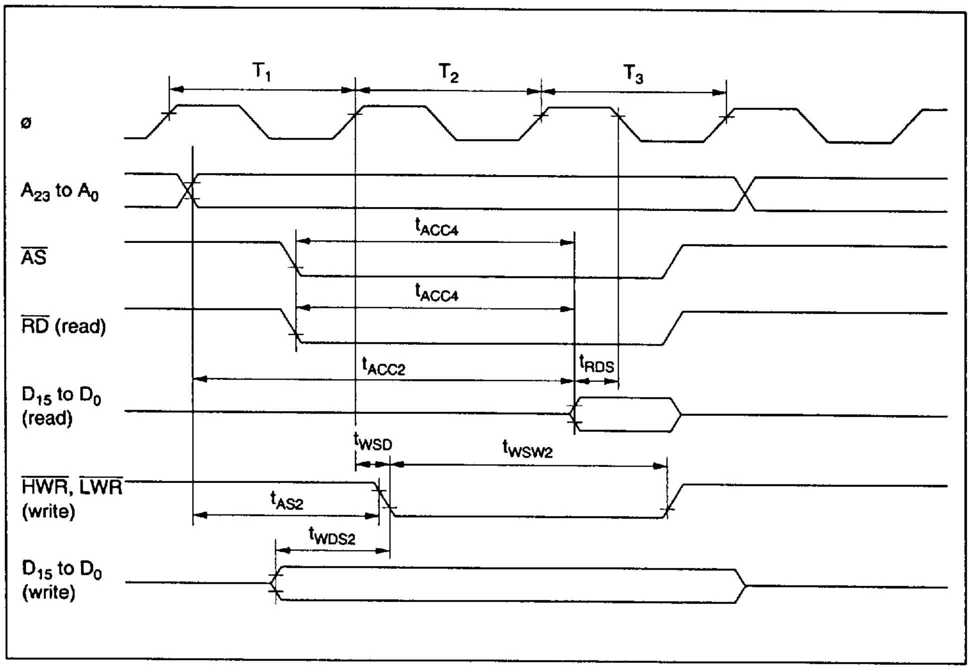


Figure 18-5 Basic Bus Cycle: Three-State Access

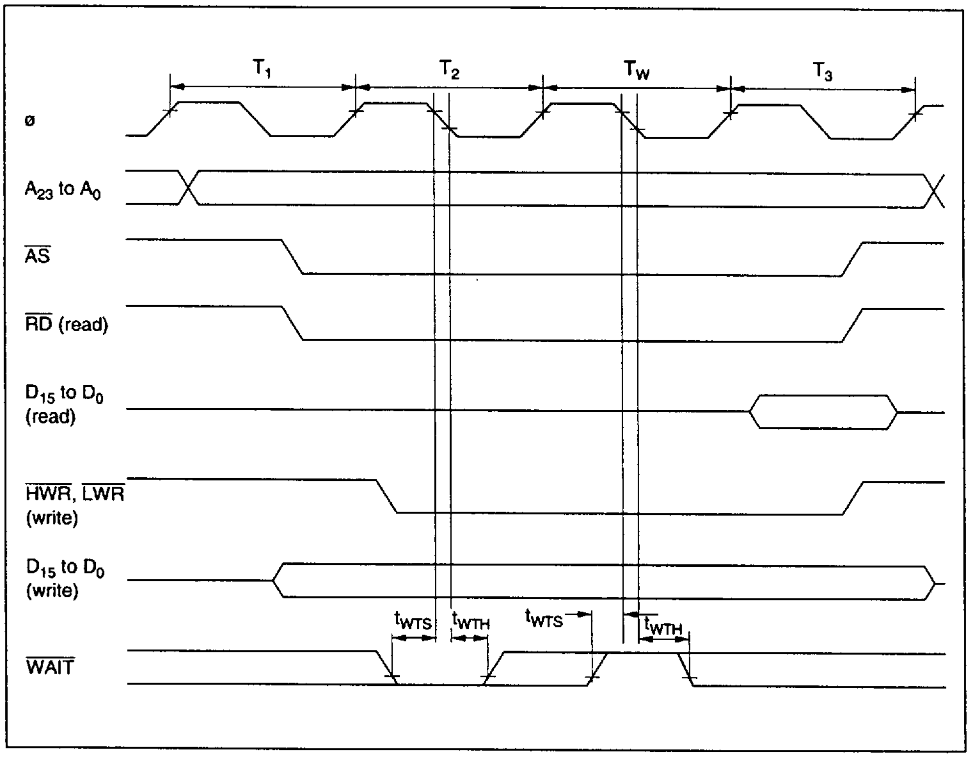


Figure 18-6 Basic Bus Cycle: Three-State Access with One Wait State

18.3.2 Refresh Controller Bus Timing

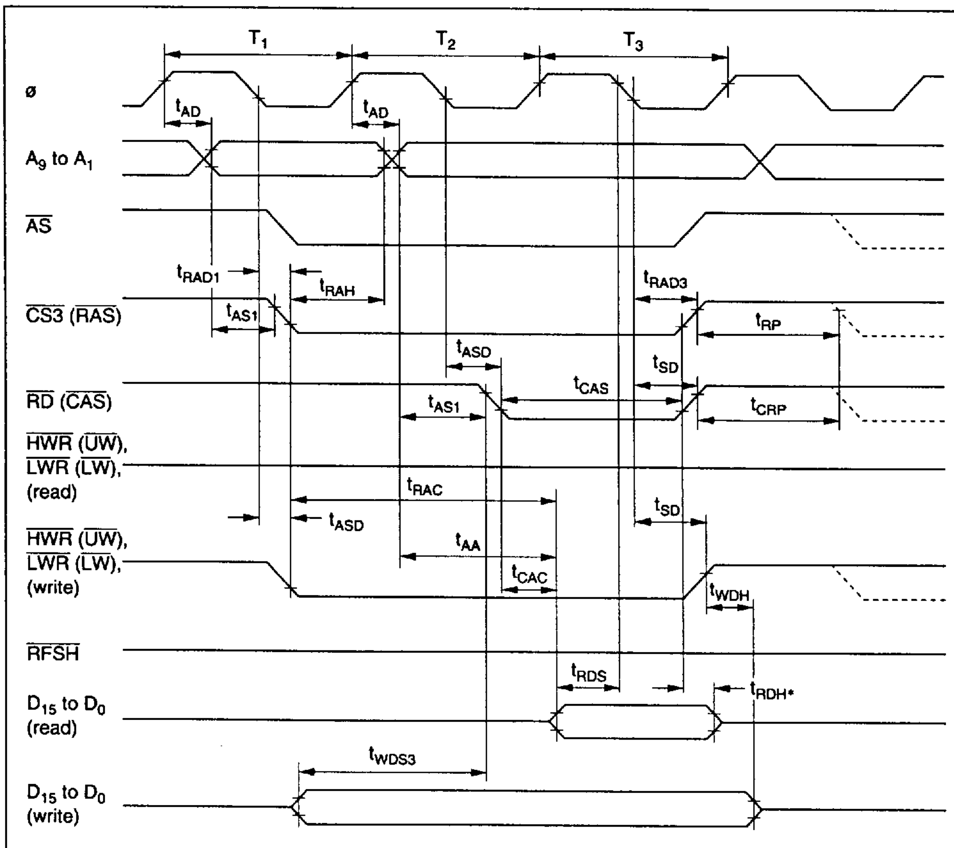
Refresh controller bus timing is shown as follows:

- DRAM bus timing

  Figures 18-7 to 18-12 show the DRAM bus timing in each operating mode.

- PSRAM bus timing

  Figures 18-13 and 18-14 show the pseudo-static RAM bus timing in each operating mode.



Note: * Stipulation from earliest $\overline{CS3}$ and $\overline{RD}$ negate timing.

Figure 18-7 DRAM Bus Timing (Read/Write): Three-State Access — 2$\overline{WE}$ Mode —

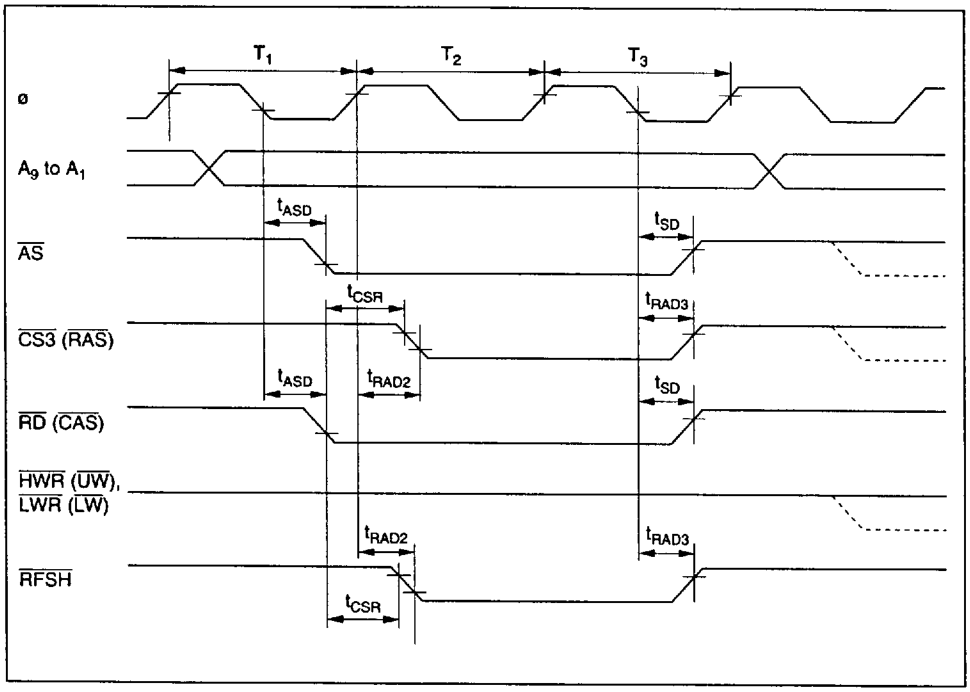


Figure 18-8 DRAM Bus Timing (Refresh Cycle): Three-State Access
— $2\overline{WE}$ Mode —

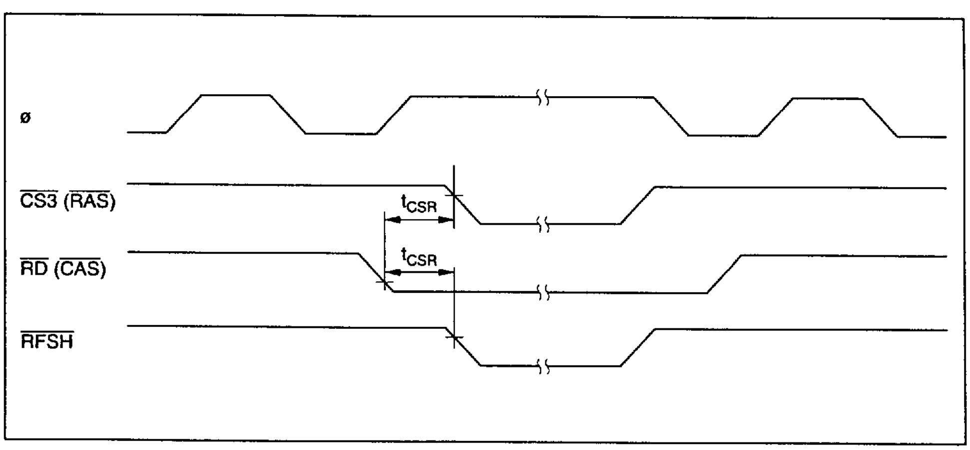
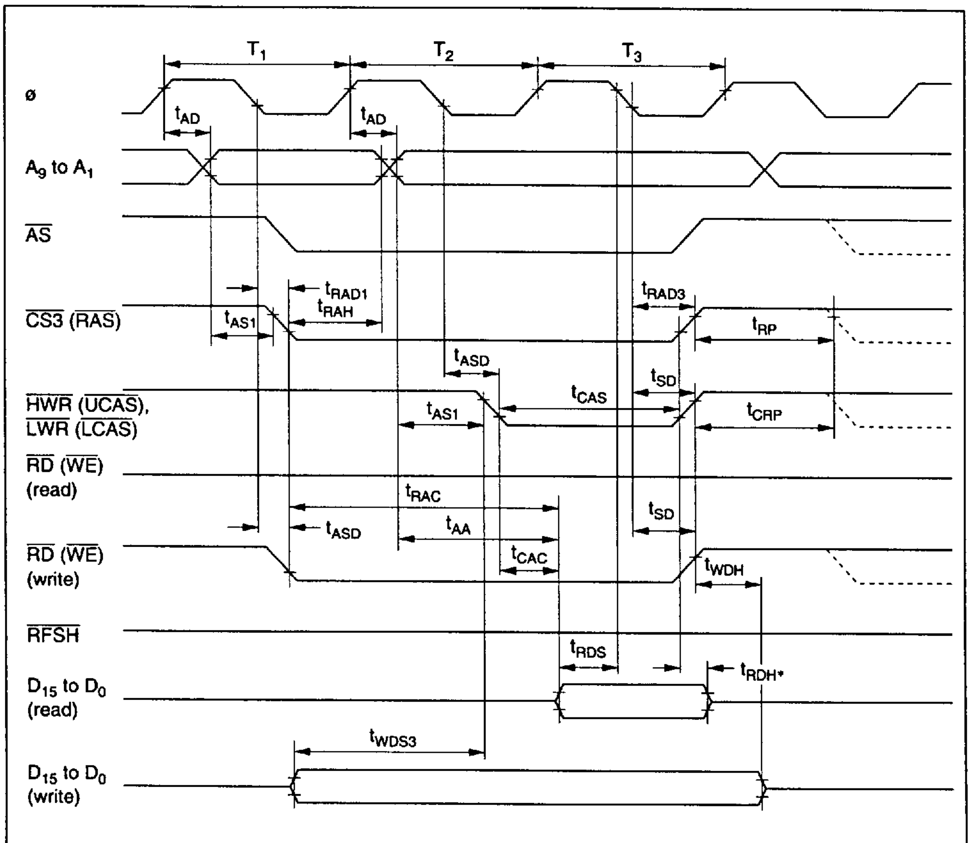


Figure 18-9 DRAM Bus Timing (Self-Refresh Mode)
— $2\overline{WE}$ Mode —



Note: * Stipulation from earliest $\overline{CS_3}$ and $\overline{RD}$ negate timing.

Figure 18-10 DRAM Bus Timing (Read/Write): Three-State Access — 2$\overline{CAS}$ Mode —

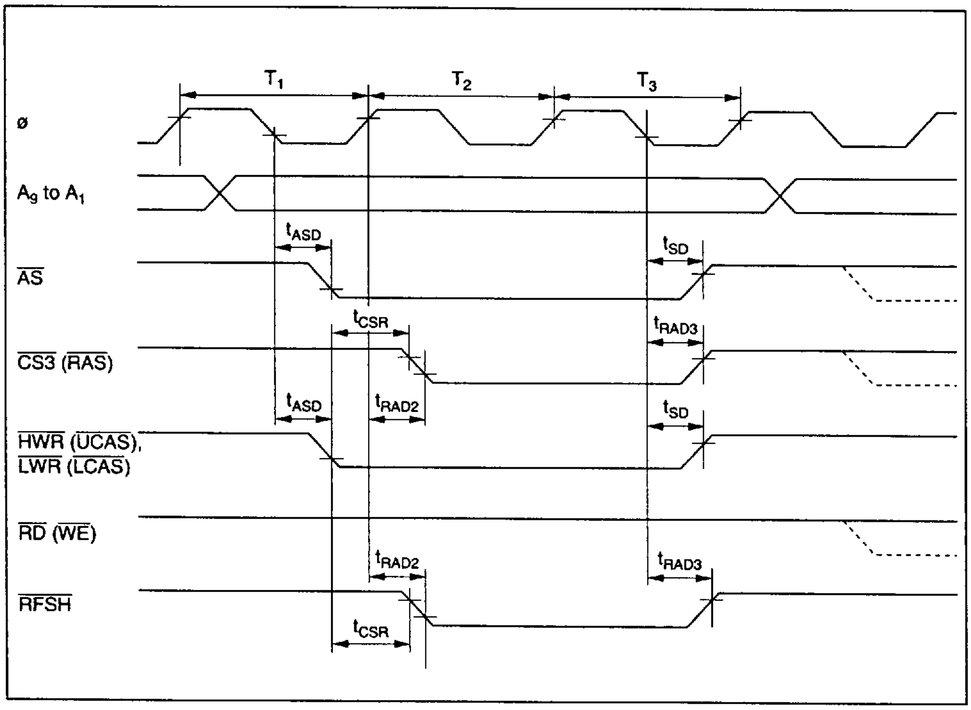


Figure 18-11 DRAM Bus Timing (Refresh Cycle): Three-State Access
— 2$\overline{\text{CAS}}$ Mode —

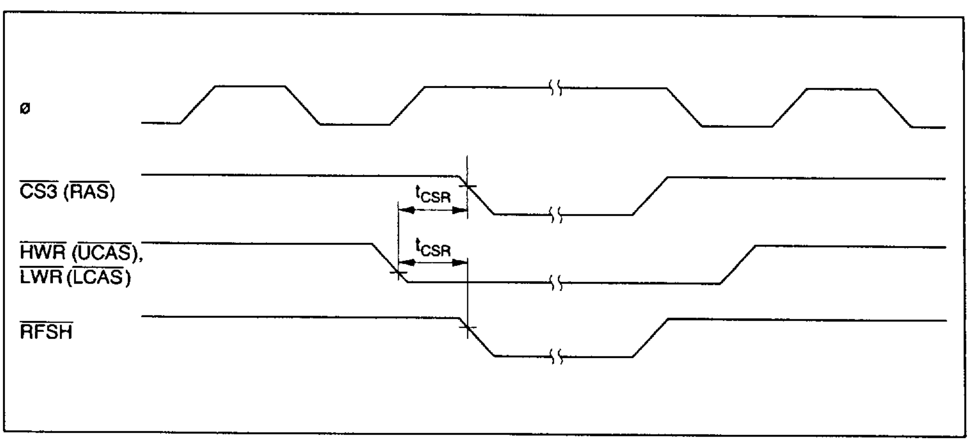


Figure 18-12 DRAM Bus Timing (Self-Refresh Mode)
— 2$\overline{\text{CAS}}$ Mode —

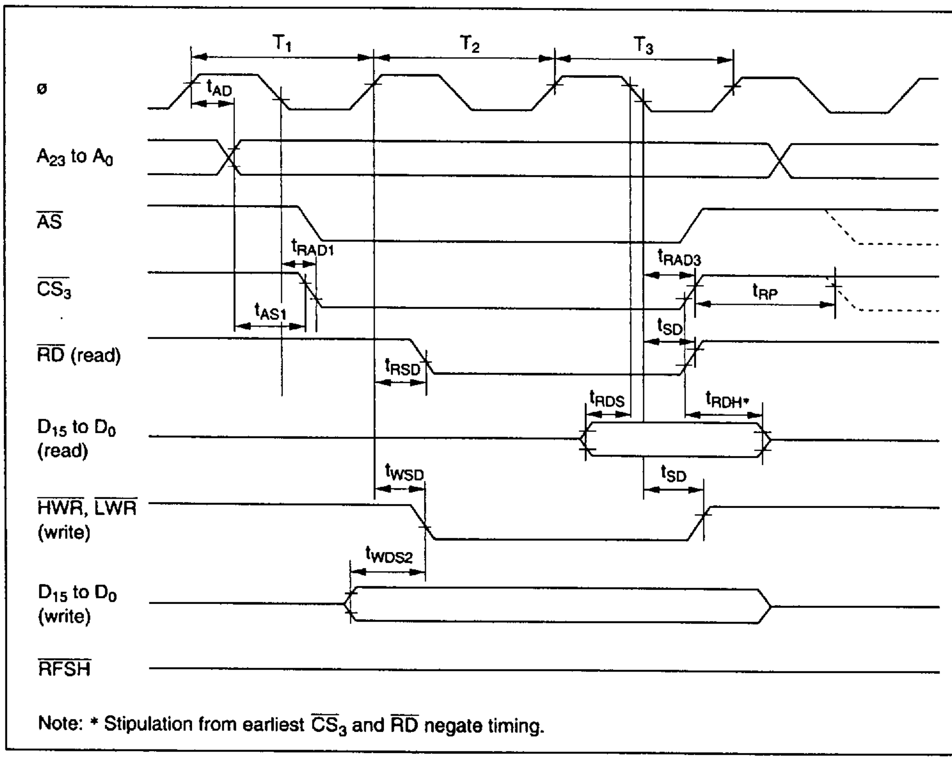


Figure 18-13 PSRAM Bus Timing (Read/Write): Three-State Access

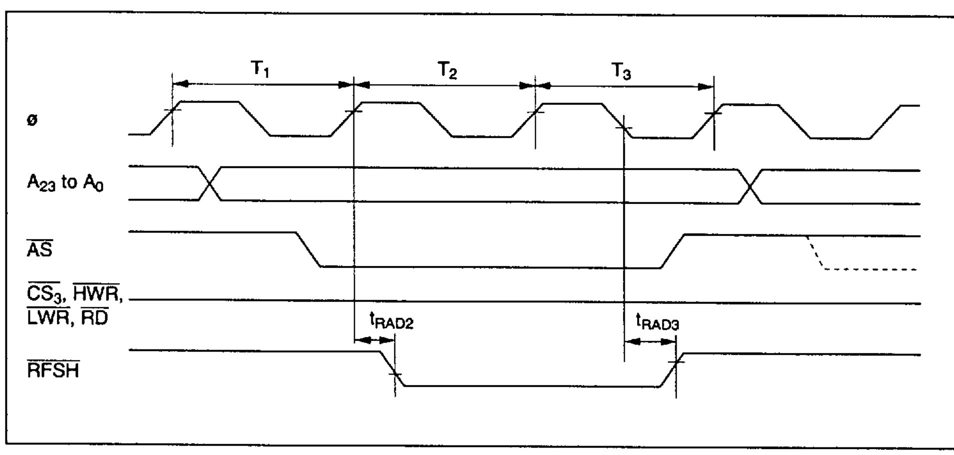


Figure 18-14 PSRAM Bus Timing (Refresh Cycle): Three-State Access

18.3.3 Control Signal Timing

Control signal timing is shown as follows:

- Reset input timing

  Figure 18-15 shows the reset input timing.

- Reset output timing

  Figure 18-16 shows the reset output timing.

- Interrupt input timing

  Figure 18-17 shows the input timing for NMI and $\overline{IRQ_7}$ to $\overline{IRQ_0}$.

- Bus-release mode timing

  Figure 18-18 shows the bus-release mode timing.

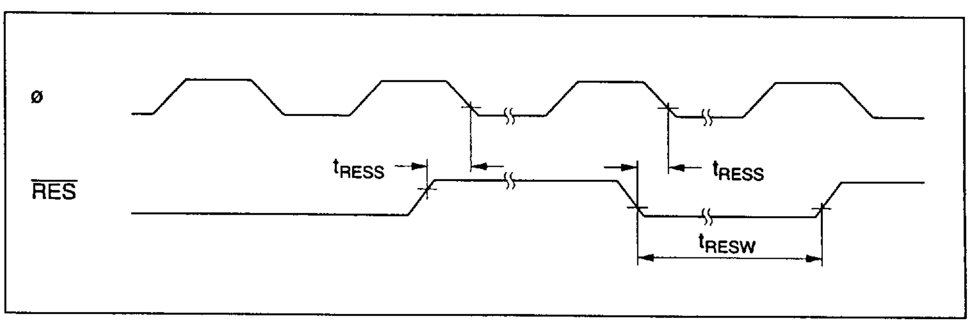


Figure 18-15 Reset Input Timing

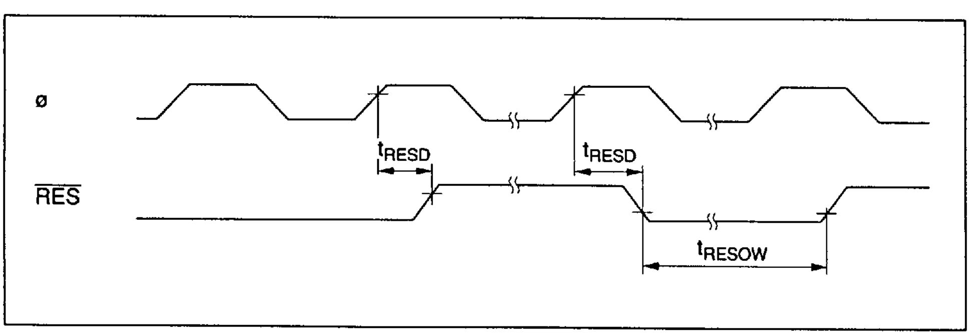


Figure 18-16 Reset Output Timing

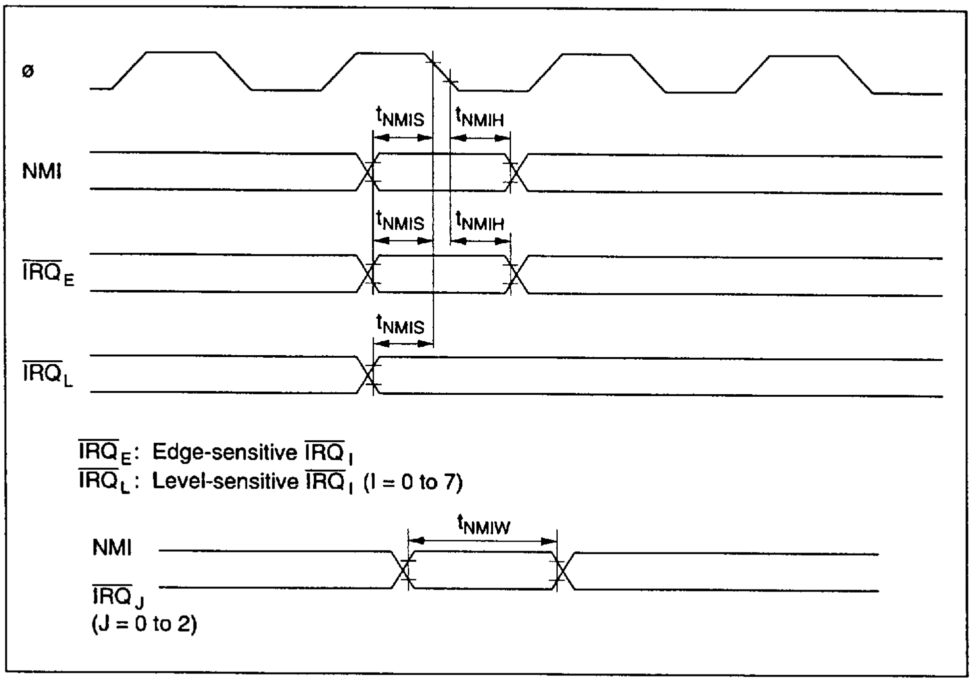


Figure 18-17 Interrupt Input Timing

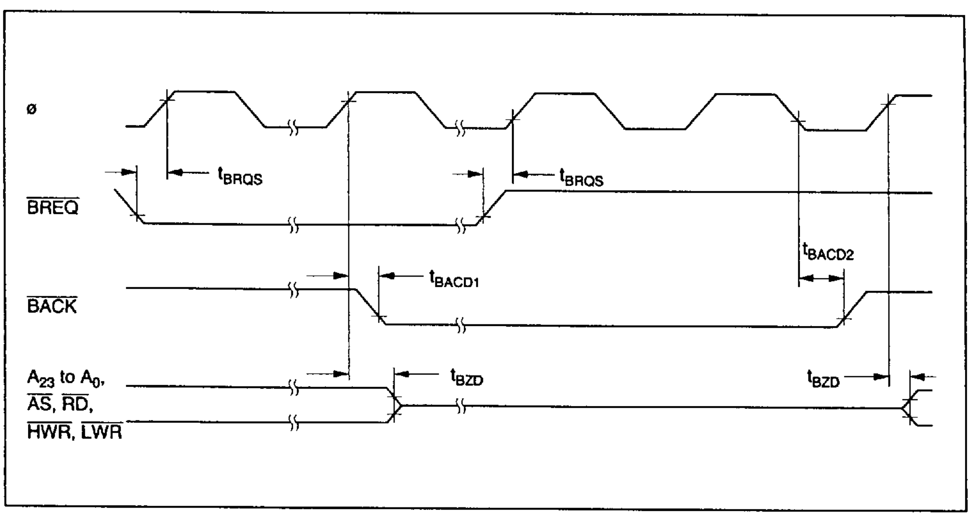


Figure 18-18 Bus-Release Mode Timing

18.3.4 Clock Timing

Clock timing is shown as follows:

- Oscillator settling timing

  Figure 18-19 shows the oscillator settling timing.

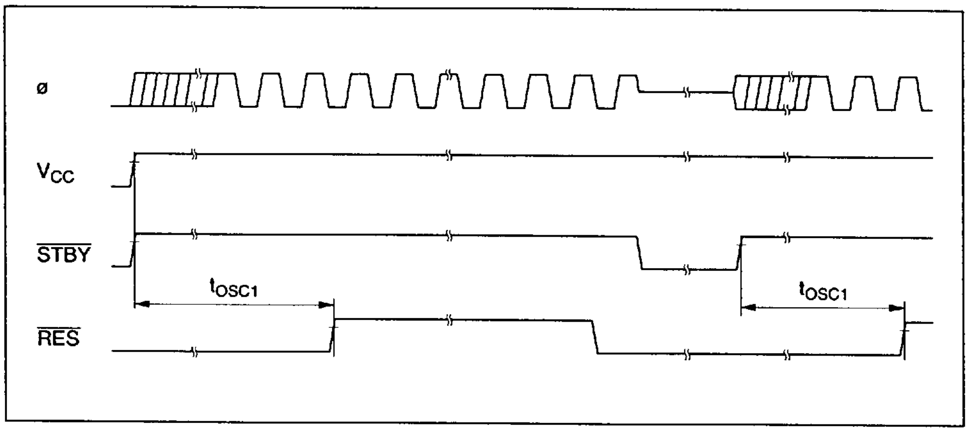


Figure 18-19 Oscillator Settling Timing

18.3.5 TPC and I/O Port Timing

TPC and I/O port timing is shown as follows.

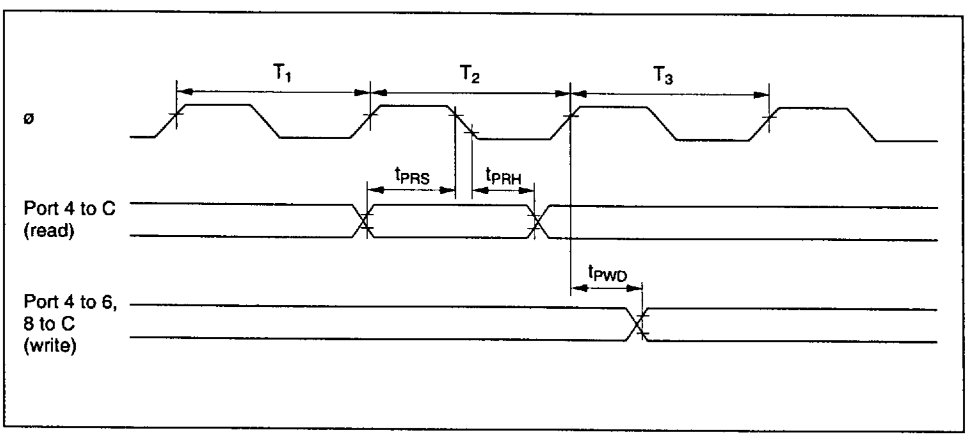


Figure 18-20 TPC and I/O Port Input/Output Timing

18.3.6 ITU Timing

ITU timing is shown as follows:

- ITU input/output timing

  Figure 18-21 shows the ITU input/output timing.

- ITU external clock input timing

  Figure 18-22 shows the ITU external clock input timing.

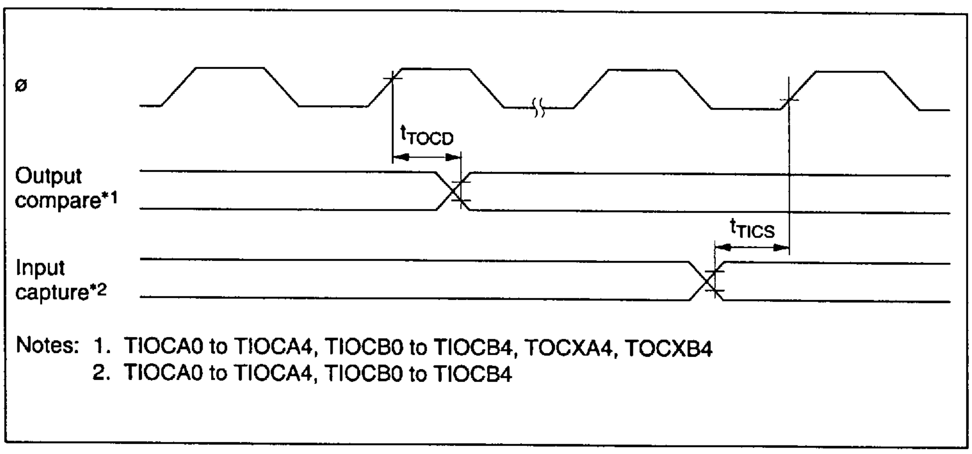


Figure 18-21 ITU Input/Output Timing

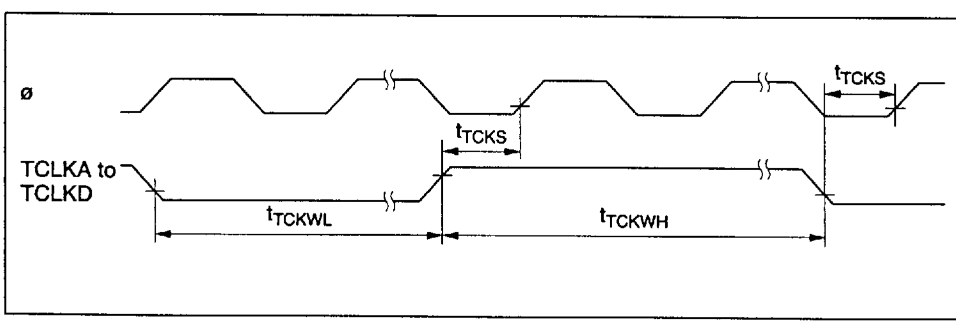


Figure 18-22 ITU Clock Input Timing

18.3.7 SCI Input/Output Timing

SCI timing is shown as follows:

- SCI input clock timing

  Figure 18-23 shows the SCI input clock timing.

- SCI input/output timing (synchronous mode)

  Figure 18-24 shows the SCI input/output timing in synchronous mode.

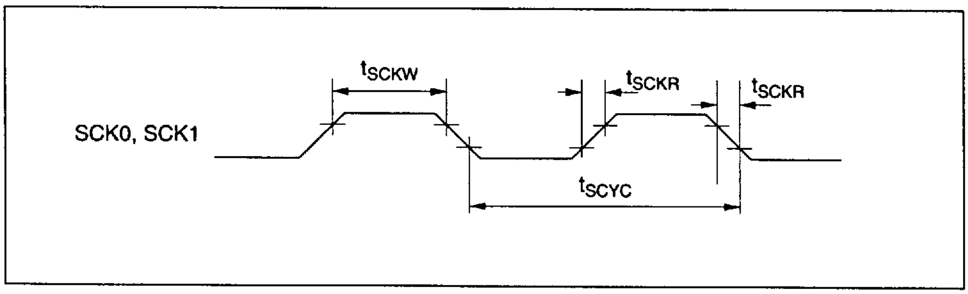


Figure 18-23 SCK Input Clock Timing

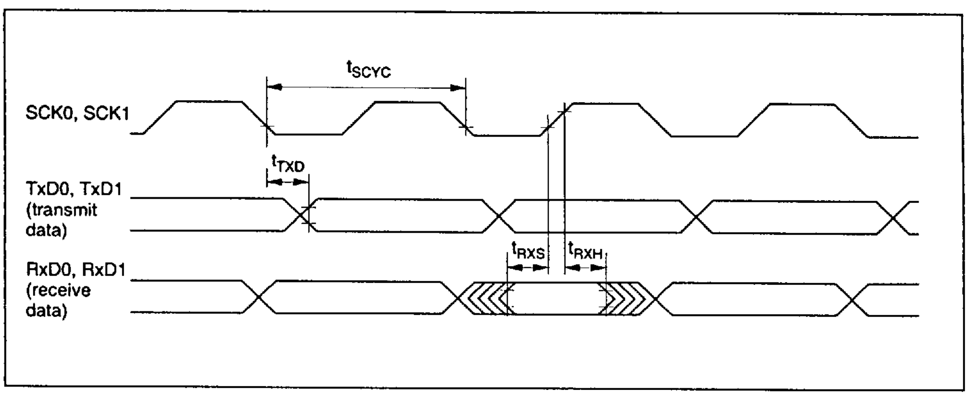


Figure 18-24 SCI Input/Output Timing in Synchronous Mode

18.3.8 DMAC Timing

DMAC timing is shown as follows.

- DMAC $\overline{\text{TEND}}$ output timing/2 state access

  Figure 18-25 shows the DMAC $\overline{\text{TEND}}$ output timing/2 state access

- DMAC $\overline{\text{TEND}}$ output timing/3 state access

  Figure 18-26 shows the DMAC $\overline{\text{TEND}}$ output timing/3 state access.

- DMAC $\overline{\text{DREQ}}$ input timing

  Figure 18-27 shows DMAC $\overline{\text{DREQ}}$ input timing.

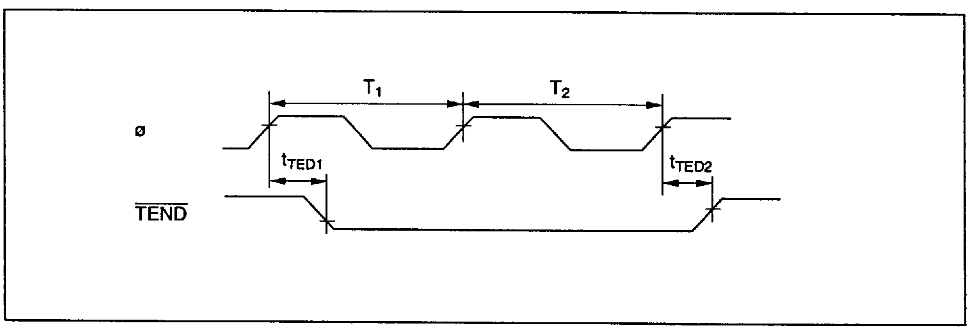


Figure 18-25 DMAC $\overline{\text{TEND}}$ Output Timing/2 State Access

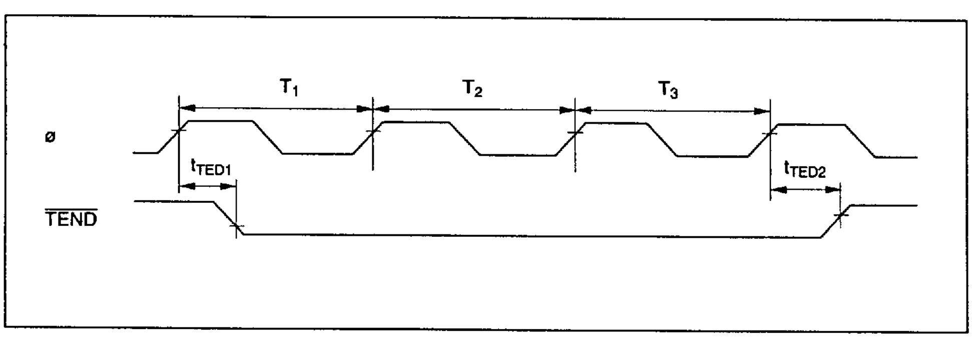


Figure 18-26 DMAC $\overline{\text{TEND}}$ Output Timing/3 State Access

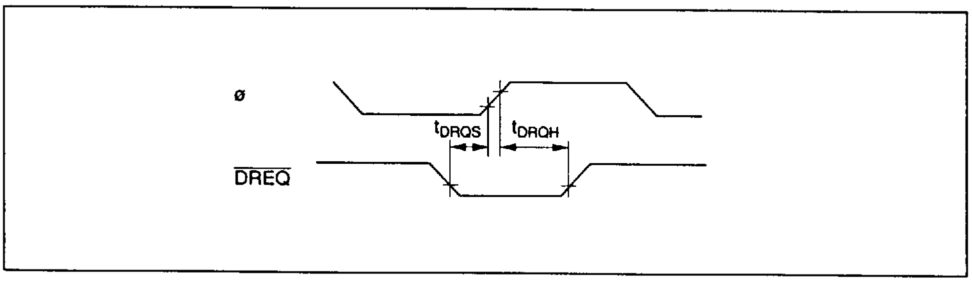


Figure 18-27 DMAC $\overline{\text{DREQ}}$ Input Timing