

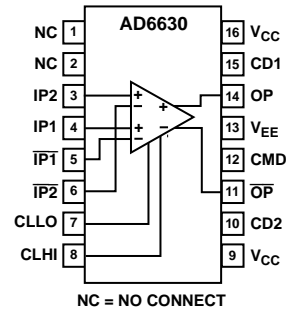
FEATURES

- 24 dB Gain
- 4 dB Noise Figure
- Easy Match to SAW Filters
- Output Limiter Adjustable +8.5 dBm to +12 dBm
- 700 MHz Bandwidth
- 10 V Single or Dual 5 V Power Supply
- 300 mW Power Dissipation

APPLICATIONS

- ADC IF Drive Amp
- Communications Receivers
- PCS/Cellular Base Stations
- GSM, CDMA, TDMA

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD6630 is an IF gain block designed to interface between SAW filters and differential input analog-to-digital converters. The AD6630 has a fixed gain of 24 dB and has been optimized for use with the AD6600 and AD6620 in digitizing narrowband IF carriers in the 70 MHz to 250 MHz range.

Taking advantage of the differential nature of SAW filters, the AD6630 has been designed as a differential in/differential out gain block. This architecture allows 100 dB of adjacent channel blocking using low cost SAW filters. The AD6630 provides output limiting for ADC and SAW protection with $<10^\circ$ phase variation in recovery from overdrive situations.

Designed for “narrow-band” cellular/PCS receivers, the high linearity and low noise performance of the AD6630 allows for implementation in a wide range of applications ranging from

GSM to CDMA to AMPS. The clamping circuitry also maintains the phase integrity of an overdriven signal. This allows phase demodulation of single carrier signals with an overrange signal.

While the AD6630 is optimized for use with the AD6600 Dual Channel, Gain Ranging ADC with RSSI, it can also be used in many other IF applications. The AD6630 is designed with an input impedance of 200 Ω and an output of 400 Ω . In the typical application shown below, these values match the real portion of a typical SAW filter. Other devices can be matched using standard matching network techniques.

The AD6630 is built using Analog Devices’ high speed complementary bipolar process. Units are available in a 300 mil SOIC (16 leads) plastic surface mount package and specified to operate over the industrial temperature range (-40°C to $+85^\circ\text{C}$).

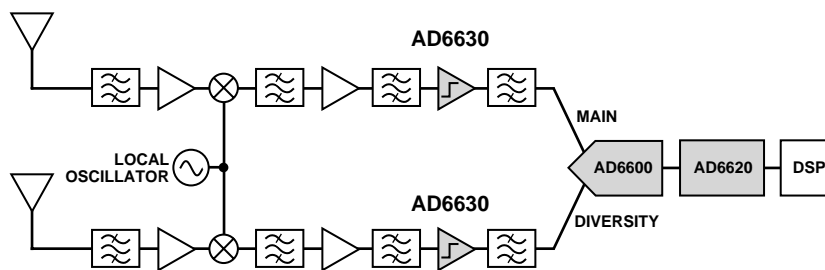


Figure 1. Reference Design

REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

AD6630—SPECIFICATIONS

NORMAL OPERATING CONDITIONS

| Parameter (Conditions) | Min | Typ | Max | Units |
|----------------------------------|-------|------|-------|-------|
| SINGLE SUPPLY VOLTAGE | 8.5 | | 10.5 | V |
| POSITIVE SUPPLY VOLTAGE | 4.25 | 5.0 | 5.25 | V |
| NEGATIVE SUPPLY VOLTAGE | -5.25 | -5.0 | -4.25 | V |
| AMBIENT TEMPERATURE | -40 | | +85 | °C |
| PACKAGE THERMAL RESISTANCE | | 80 | | °C/W |
| OPERATING FREQUENCY ¹ | 70 | | 250 | MHz |

DC SPECIFICATIONS

($T_{MIN} = -40^{\circ}\text{C}$, $T_{MAX} = +85^{\circ}\text{C}$. Output dc levels are nominally at V_M , where $V_M = V_{CC} + V_{EE} = [+5\text{ V} + (-5\text{ V})] = 0$. Inputs should be AC coupled.)

| Parameter | Temp | Test Level | Min | Typ | Max | Units |
|-----------------|------|------------|-------------|-----|-------------|-------|
| SUPPLY CURRENT | Full | II | | 30 | 48 | mA |
| OUTPUT DC LEVEL | Full | II | $V_M - 150$ | | $V_M + 150$ | mV |

AC SPECIFICATIONS

($T_{MIN} = -40^{\circ}\text{C}$, $T_{MAX} = +85^{\circ}\text{C}$. All AC production tests are performed at 5 MHz, 70 MHz and 250 MHz performance limits are correlated to 5 MHz testing based on characterization data.)

| Parameter ¹ | Temp | Test Level | Min | Typ | Max | Units |
|--|-------|------------|-----|------|------|-------|
| GAIN (POWER) @ 70 MHz | Full | II | 23 | 24 | 25 | dB |
| GAIN (POWER) @ 250 MHz | Full | II | 22 | 23 | 24 | dB |
| -3 dB BANDWIDTH | +25°C | V | | 700 | | MHz |
| OUTPUT REFERRED IP3 @ 70 MHz ² | Full | V | | 22 | | dBm |
| OUTPUT REFERRED IP3 @ 250 MHz ² | Full | V | | 19 | | dBm |
| OUTPUT REFERRED IP2 @ 70 MHz ² | Full | V | | 45 | | dBm |
| OUTPUT REFERRED IP2 @ 250 MHz ² | Full | V | | 45 | | dBm |
| OUTPUT REFERRED 1 dB COMPRESSION POINT @ 70 MHz LOW LEVEL CLAMP ³ | Full | II | 8.5 | | | dBm |
| OUTPUT REFERRED 1 dB COMPRESSION POINT @ 250 MHz LOW LEVEL CLAMP ³ | Full | II | 7.5 | | | dBm |
| OUTPUT REFERRED 1 dB COMPRESSION POINT @ 70 MHz HIGH LEVEL CLAMP ⁴ | Full | II | 11 | | | dBm |
| OUTPUT REFERRED 1 dB COMPRESSION POINT @ 250 MHz HIGH LEVEL CLAMP ⁴ | Full | II | 9 | | | dBm |
| OUTPUT SLEW RATE | +25°C | V | | 3700 | | V/μs |
| INPUT IMPEDANCE (REAL) | +25°C | V | | 200 | | Ω |
| INPUT CAPACITANCE | +25°C | V | | 2 | | pF |
| OUTPUT IMPEDANCE (REAL) | +25°C | V | | 400 | | Ω |
| OUTPUT CAPACITANCE | +25°C | V | | 2 | | pF |
| NOISE FIGURE | +25°C | V | | 4 | | dB |
| LOW LEVEL CLAMP MAXIMUM OUTPUT @ 70 MHz ^{3,5} | Full | IV | | 11 | 12.5 | dBm |
| HIGH LEVEL CLAMP MAXIMUM OUTPUT @ 70 MHz ^{4,5} | Full | IV | | 13.8 | 14.3 | dBm |
| LOW LEVEL CLAMP MAXIMUM OUTPUT @ 250 MHz ^{3,5} | Full | IV | | 9.25 | 10.6 | dBm |

| Parameter | Temp | Test Level | Min | Typ | Max | Units |
|---|-------|------------|-----|------|------|--------|
| HIGH LEVEL CLAMP MAXIMUM OUTPUT @ 250 MHz ^{4, 5} | Full | IV | | 11.2 | 12.2 | dBm |
| PHASE VARIATION ⁶ | +25°C | V | | 9 | | Degree |
| CMRR ⁷ | +25°C | V | | 50 | | dB |
| PSRR ⁸ | +25°C | V | | 30 | | dB |

NOTES

¹All specifications are valid across the operating frequency range when the source and load impedance are a conjugate match to the amplifier's input and output impedance.

²Test is for two tones separated by 1 MHz for IFs at 70 MHz and 250 MHz at -23 dBm per tone input.

³Low Level Clamp is selected by connecting pin CLLO to the negative supply, while pin CLHI is left floating. Clamping can be set at lower levels by connecting pin CLLO and CLHI to the negative supply through an external resistor.

⁴High Level Clamp is selected by connecting pin CLHI to the negative supply, while pin CLLO is left floating, this allows the maximum linear range of the device to be utilized.

⁵Output clamp levels are measured for hard clamping with a +3 dBm input level. Valid for a maximum input level of +8 dBm/200 Ω = 3.2 V p-p—differential.

⁶Measured as the change in output phase when the input level is changed from -53 dBm to +8 dBm (i.e., from linear operation to clamping).

⁷Ratio of the differential output signal (referenced to the input) to the common-mode input signal presented to all input pins.

⁸Ratio of signal on supply to differential output (<500 kHz).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

| Parameter | Min | Max | Units |
|-------------------------|-------|------|-------|
| Single Supply Voltage | -0.5 | 11.5 | V |
| Positive Supply Voltage | -0.5 | 5.75 | V |
| Negative Supply Voltage | -5.75 | 0.5 | V |
| Input Power | | +8 | dBm |
| Storage Temperature | -65 | +150 | °C |
| Junction Temperature | | +150 | °C |
| ESD Protection | 1 | | kV |

EXPLANATION OF TEST LEVELS

- I. 100% production tested.
- II. 100% production tested at +25°C, and guaranteed by design and analysis at temperature extremes.
- III. Sample tested only.
- IV. Parameter guaranteed by design and analysis.
- V. Parameter is typical value only.
- VI. 100% production tested at +25°C, and sample tested at temperature extremes.

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------|--------------------------|--------------------------------|----------------|
| AD6630AR | -40°C to +85°C (Ambient) | 16-Lead Wide Body SOIC | R-16 |
| AD6630AR-REEL | -40°C to +85°C (Ambient) | AD6630AR on 1000 PC Reel | |
| AD6630R/PCB | | Evaluation Board with AD6630AR | |

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6630 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

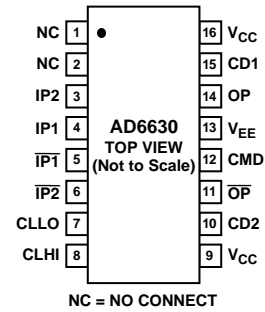


AD6630

PIN FUNCTION DESCRIPTION

| Pin No | Pin Name | Description |
|--------|------------------|-------------------------|
| 1, 2 | NC | No Connect |
| 3 | IP2 | Input |
| 4 | IP1 | Input |
| 5 | $\overline{IP1}$ | Input |
| 6 | $\overline{IP2}$ | Input |
| 7 | CLLO | Clamp Level Low Pin |
| 8 | CLHI | Clamp Level High Pin |
| 9 | V _{CC} | +V _{CC} Supply |
| 10 | CD2 | Clamp Decoupling |
| 11 | \overline{OP} | Output |
| 12 | CMD | DC Feedback Decoupling |
| 13 | V _{EE} | -V _{EE} Supply |
| 14 | OP | Output |
| 15 | CD1 | Clamp Decoupling |
| 16 | V _{CC} | +V _{CC} Supply |

PIN CONFIGURATION



Typical Performance Characteristics

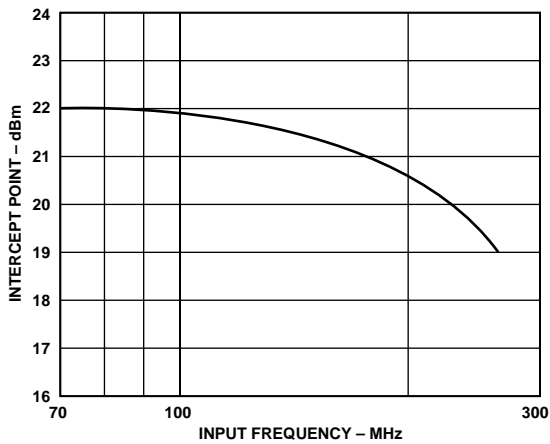


Figure 2. 3rd Order Intercept (IP3) vs. Frequency

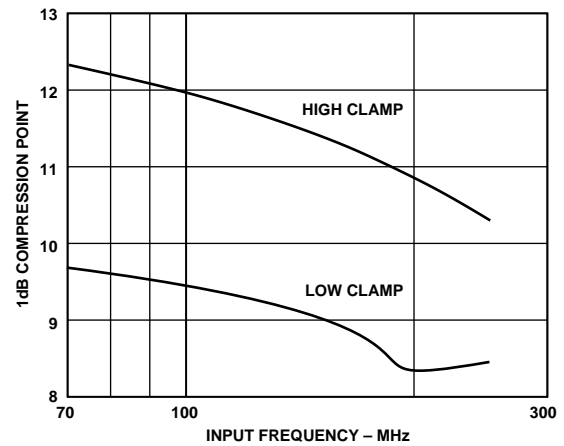


Figure 4. 1 dB Compression Point (Typical)

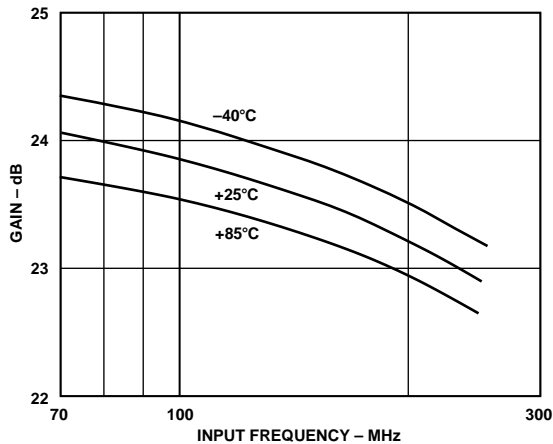


Figure 3. Gain vs. Frequency

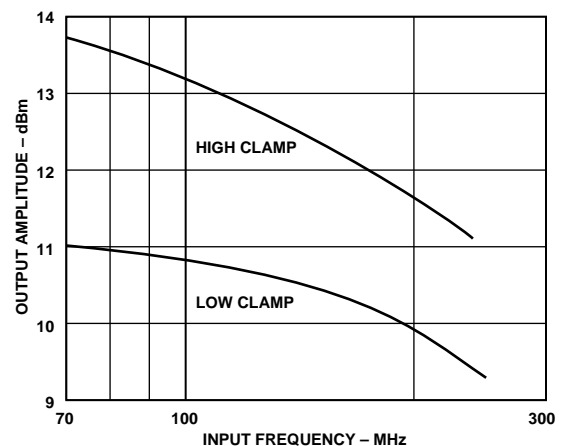


Figure 5. Clamp Level vs. Frequency

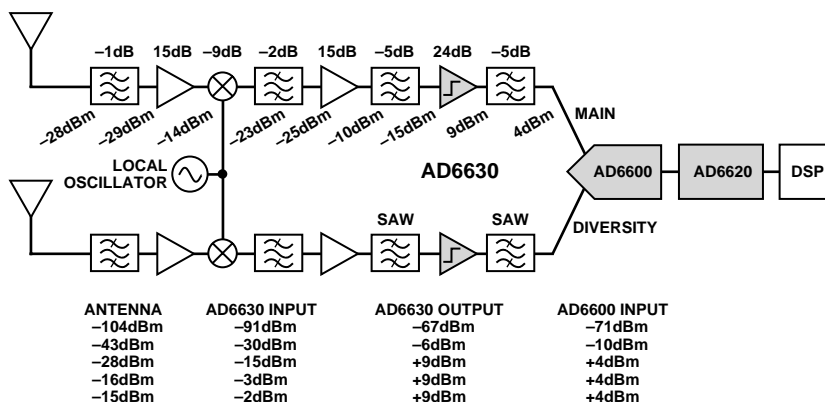


Figure 6. GSM Design Example

THEORY OF OPERATION

The AD6630 amplifier consists of two stages of gain. The first stage is differential. This differential amplifier provides good common-mode rejection to common-mode signals passed by the SAW filter. The second stage consists of matched current feedback amplifiers on each side of the differential pair. These amplifiers provide additional gain as well as output drive capability. Gain set resistors for these stages are internal to the device and cannot be changed, allowing fixed compensation for optimum performance.

Clamping levels for the device are normally set by tying CLLO or CLHI pins to the negative supply. This internally sets bias points that generate symmetric clamping levels. Clamping is achieved primarily in the output amplifiers. Additional input stage clamping is provided for additional protection. Clamping levels may be adjusted to lower levels as discussed below.

APPLICATIONS

The AD6630 provides several useful features to meet the needs of radio designers. The gain and low noise figure of the device make it perfect for providing interstage gain between differential SAW filters and/or analog-to-digital converters (ADC). Additionally, the on-board clamping circuitry provides protection for sensitive SAW filters or ADCs. The fast recovery of the clamp circuit permits demodulation of constant envelope modulated IF signals by preserving the phase response during clamping.

The following topics provide recommendations for using the AD6630 in narrowband, single carrier applications.

Adjusting Output Clamp Levels

Normally, the output clamp level is set by tying either CLLO or CLHI to ground or V_{EE} . It is possible to set the limit between 8.5 dBm and 12 dBm levels by selecting the appropriate external resistor.

To set to a different level, CLLO and CLHI should be tied together and then through a resistor to ground. The value of the resistor can be selected using the following equation.

$$R = \frac{14.4 - OUTPUT_{CLAMP} (dBm)}{0.0014}$$

This equation is derived from measured data at 170 MHz. Clamp levels vary with frequency, see Figure 5. Output clamp levels less than 8.5 dBm will result in damage to the clamp circuitry unless the absolute maximum input power is derated. Similarly, the output clamp level cannot be set higher than 12 dBm.

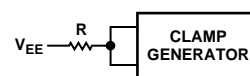


Figure 7. Clamp Level Resistor

Matching SAW Filters

The AD6630 is designed to easily match to SAW filters. SAW filters are largely capacitive in nature. Normally a conjugate match to the load is desired for maximum power transfer.

Another way to treat the problem is to make the SAW filter look purely resistive. If the SAW filter load looks resistive there is no lead or lag in the current vs. voltage. This may not preserve maximum power transfer, but maximum voltage swing will exist. All that is required to make the SAW filter input or output look real is a single inductor shunted across the input. When the correct value is used, the impedance of the SAW filter becomes real.

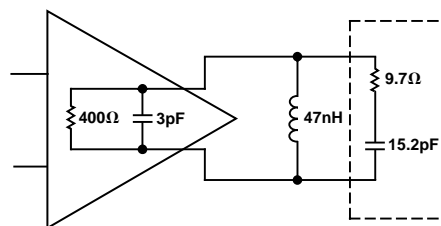


Figure 8. Saw Filter Model (170 MHz)

EVALUATION BOARD

Figures 9, 10 and 12 refer to the schematic and layout of the AD6630AR as used on Analog Devices' GSM Diversity Receiver Reference Design (only the IF section is shown). Figure 14 references the schematic of the stand-alone AD6630 evaluation board and uses a similar layout. The evaluation board uses center tapped transformers to convert the input to a differential signal and AD6630 outputs to a single connector to simplify evaluation. C8, C9 and L2 are optional reactive components to tune the load for a particular IF frequency if desired.

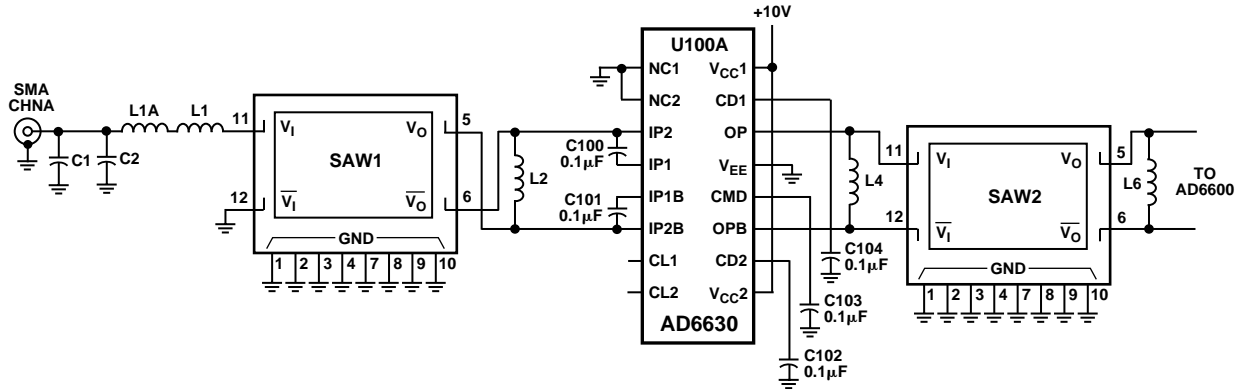


Figure 9. Reference Design Schematic (One Channel)

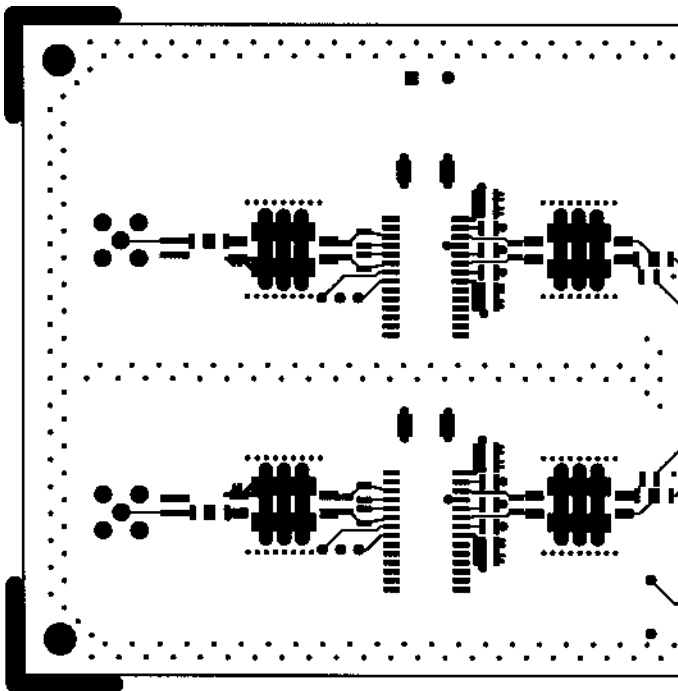


Figure 10. Reference Design PCB Layout

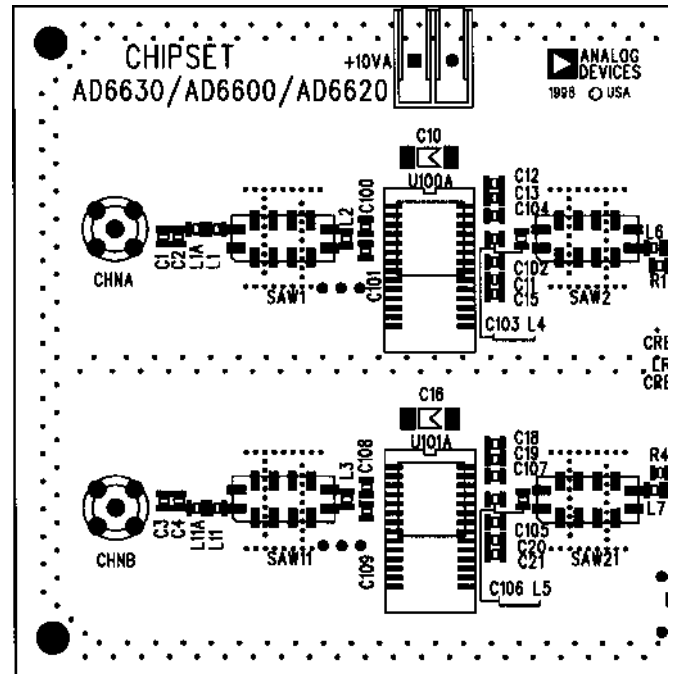


Figure 12. Reference Design Component Placement (Two Channels Shown)

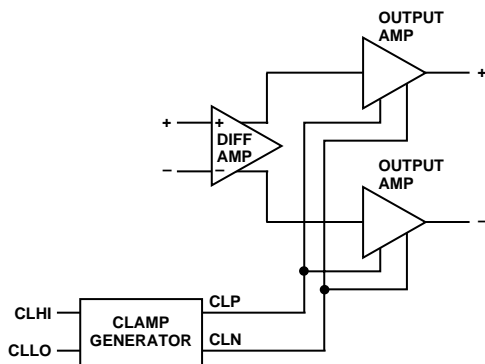


Figure 11. Functional Block Diagram

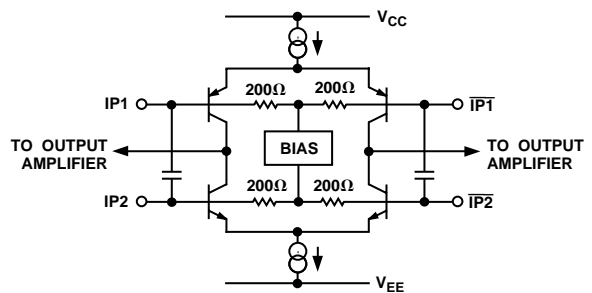


Figure 13. Equivalent Input Circuit

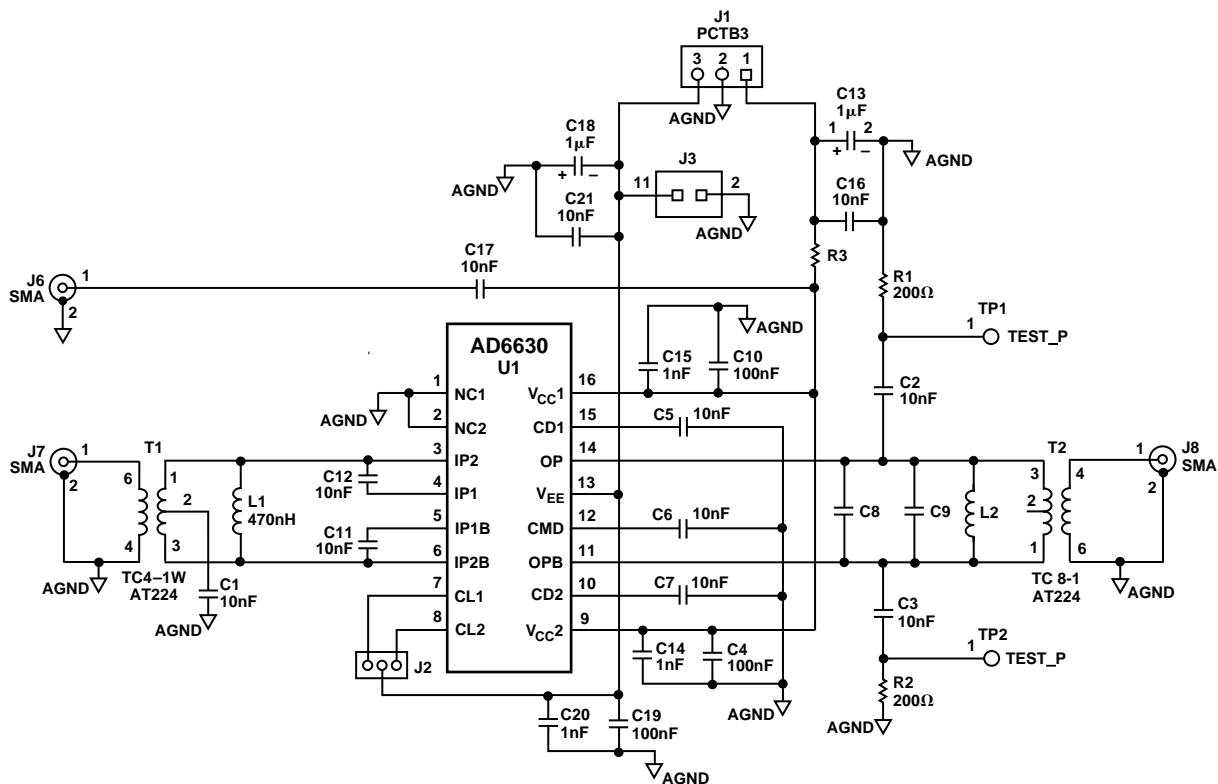


Figure 14. Evaluation Board Schematic

Table I. Typical S Parameters

| Frequency (MHz) | S_{11} | S_{12} | S_{21} | S_{22} |
|-----------------|----------------------------|---------------------------|---------------------------|----------------------------|
| 70 | $224.5 \angle -4.52^\circ$ | $-41.0 \angle -3.0^\circ$ | $24.1 \angle -8.8^\circ$ | $394.3 \angle -8.6^\circ$ |
| 170 | $264.8 \angle -32.9^\circ$ | $-31.4 \angle 0^\circ$ | $23.5 \angle -22.5^\circ$ | $382.4 \angle -21.9^\circ$ |
| 200 | $227.9 \angle -34.8^\circ$ | $-41.0 \angle -5^\circ$ | $23.2 \angle -26.4^\circ$ | $353.0 \angle -25.4^\circ$ |
| 250 | $209.5 \angle -36.2^\circ$ | $-40.6 \angle -2.3^\circ$ | $22.9 \angle -38.9^\circ$ | $328.9 \angle -29.2^\circ$ |

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Wide Body SOIC (R-16)

