

DATA SHEET

UMA1020M

Low-voltage dual frequency
synthesizer for radio telephones

Product specification
Supersedes data of November 1994
File under Integrated Circuits, IC03

1995 Jun 15

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at RF input frequencies up to 2.4 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. $V_{DD} = 3$ V and $V_{CC} = 5$ V for wider tuning range).

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 7-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------|--|--|------|------|------|--------------|
| V_{CC}, V_{DD} | supply voltage | $V_{CC} \geq V_{DD}$ | 2.7 | – | 5.5 | V |
| $I_{CC} + I_{DD}$ | principal synthesizer supply current | auxiliary synthesizer in power-down mode | – | 9.4 | – | mA |
| | principal and auxiliary synthesizer supply current | principal and auxiliary synthesizers ON | – | 12.1 | – | mA |
| I_{CCPD}, I_{DDPD} | current in power-down mode per supply | | – | 12 | – | μ A |
| f_{VCO} | principal input frequency | | 1700 | – | 2400 | MHz |
| f_{AI} | auxiliary input frequency | | 20 | – | 300 | MHz |
| f_{XTAL} | crystal reference input frequency | | 3 | – | 40 | MHz |
| f_{PPC} | principal phase comparator frequency | | – | 200 | – | kHz |
| f_{APC} | auxiliary phase comparator frequency | | – | 200 | – | kHz |
| T_{amb} | operating ambient temperature | | –30 | – | +85 | $^{\circ}$ C |

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ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| UMA1020M | SSOP20 | plastic shrink small outline package; 20 leads; body width 4.4 mm | SOT266-1 |

BLOCK DIAGRAM

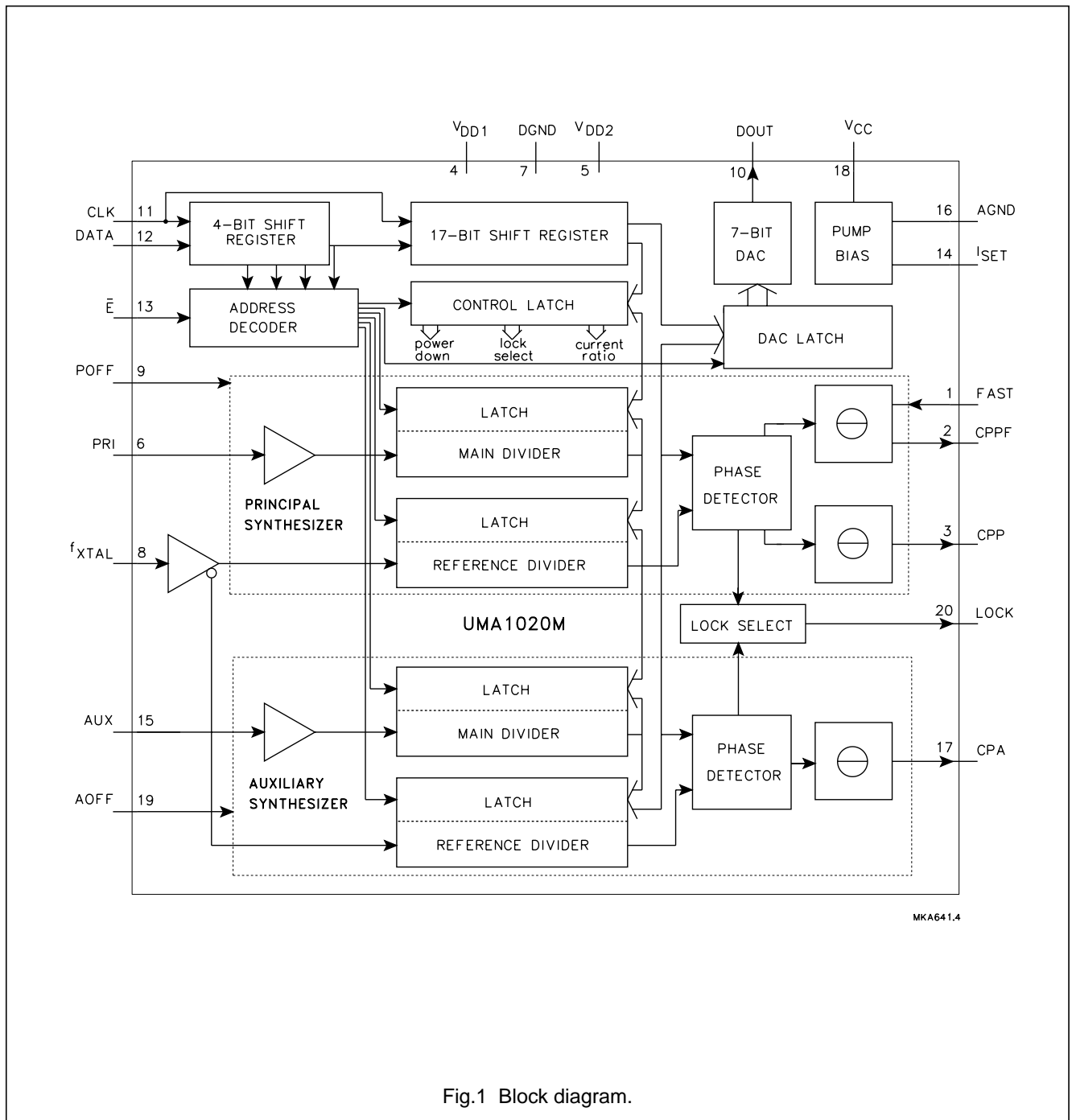


Fig.1 Block diagram.

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|-------------------|-----|--|
| FAST | 1 | control input to speed-up main synthesizer |
| CPPF | 2 | principal synthesizer speed-up charge-pump output |
| CPP | 3 | principal synthesizer normal charge-pump output |
| V _{DD1} | 4 | digital power supply 1 |
| V _{DD2} | 5 | digital power supply 2 |
| PRI | 6 | 2 GHz principal synthesizer frequency input |
| DGND | 7 | digital ground |
| f _{XTAL} | 8 | crystal frequency input from TCXO |
| POFF | 9 | principal synthesizer power-down input |
| DOUT | 10 | 7-bit digital-to-analog output |
| CLK | 11 | programming bus clock input |
| DATA | 12 | programming bus data input |
| \bar{E} | 13 | programming bus enable input (active LOW) |
| I _{SET} | 14 | regulator pin to set the charge-pump currents |
| AUX | 15 | auxiliary synthesizer frequency input |
| AGND | 16 | analog ground |
| CPA | 17 | auxiliary synthesizer charge-pump output |
| V _{CC} | 18 | supply for charge-pump and DAC circuits |
| AOFFF | 19 | auxiliary synthesizer power-down input |
| LOCK | 20 | in-lock detect output (main PLL); test mode output |

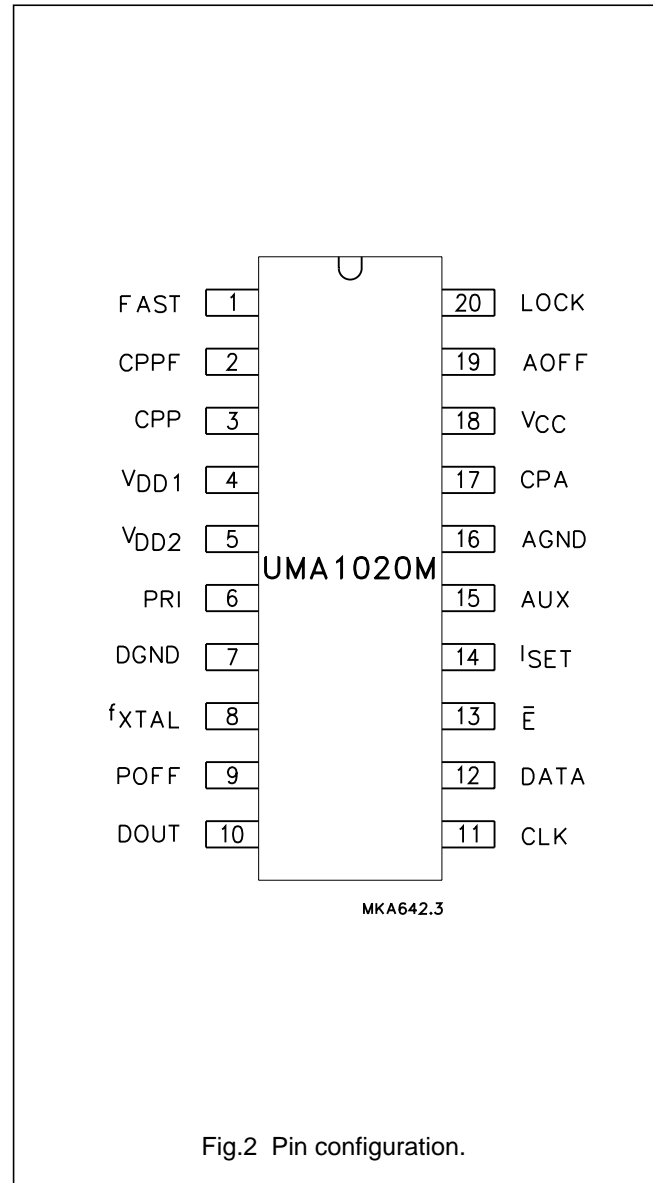


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a preamplifier to provide the clock to the first divider stage. The preamplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV to 180 mV (RMS), and at frequencies up to 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131071) allow a 2 MHz phase comparison frequency.

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The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μ A. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison, an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the principal reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and \bar{E} (enable). The data sent to the device is loaded in bursts framed by \bar{E} . Programming clock edges and their appropriate data bits are ignored until \bar{E} goes active LOW. The programmed information is loaded into the addressed latch when \bar{E} returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020M uses 6 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of \bar{E} . This produces an internal load pulse to store the data in one of the addressed latches. To ensure that the data is correctly loaded on first power-up, \bar{E} should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum \bar{E} pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

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Table 1 Format of programmed data

| LAST IN | | PROGRAMMING REGISTER BIT USAGE | | | | | | FIRST IN | |
|---------------|------|--------------------------------|------|-------|------------------|-------|--------|----------|--|
| p21 | p20 | p19 | p18 | p17 | p16 | ../.. | p2 | p1 | |
| ADD0 | ADD1 | ADD2 | ADD3 | DATA0 | DATA1 | ../.. | DATA15 | DATA16 | |
| LATCH ADDRESS | | | | LSB | DATA COEFFICIENT | | | MSB | |

Table 2 Bit allocation (note 1)

| FT | | REGISTER BIT ALLOCATION | | | | | | | | | | | | | | | | | | LT | | |
|--------------------------|------------------------------------|-------------------------|------|------------------------------------|------------|------|---|----|-----|-------|-----------|-----|-----|-----|-----|-----|---------|-----|-----|-----|---|--|
| p1 | p2 | p3 | p4 | p5 | p6 | p7 | p8 | p9 | p10 | p11 | p12 | p13 | p14 | p15 | p16 | p17 | p18 | p19 | p20 | p21 | | |
| dt16 | dt15 | dt14 | dt13 | dt12 | DATA FIELD | | | | | | | dt4 | dt3 | dt2 | dt1 | dt0 | ADDRESS | | | | | |
| TEST BITS ⁽²⁾ | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | |
| X | X | X | X | OLP | OLA | CR1 | CR0 | X | X | sPOFF | sAOFF | X | X | X | X | X | 0 | 0 | 0 | 1 | | |
| PM16 | PRINCIPAL MAIN DIVIDER COEFFICIENT | | | | | | | | | | | | | | | PM0 | 0 | 1 | 0 | 0 | | |
| X | X | X | X | X | X | PR10 | PRINCIPAL REFERENCE DIVIDER COEFFICIENT | | | | | | | PR0 | 0 | 1 | 0 | 1 | | | | |
| X | X | X | AM13 | AUXILIARY MAIN DIVIDER COEFFICIENT | | | | | | | | | | | AM0 | 0 | 1 | 1 | 0 | | | |
| X | X | X | X | X | X | AR10 | AUXILIARY REFERENCE DIVIDER COEFFICIENT | | | | | | | AR0 | 0 | 1 | 1 | 1 | | | | |
| X | X | X | X | X | X | X | X | X | 0 | DA6 | 7-BIT DAC | | | | DA0 | 1 | 0 | 0 | 0 | | | |

Notes

1. FT = first; LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register should not be programmed with any other value except all zeros for normal operation.

Table 3 Out-of-lock select

| OLP | OLA | OUT-OF-LOCK ON PIN 20 |
|-----|-----|------------------------------|
| 0 | 0 | output disabled |
| 0 | 1 | auxiliary phase error |
| 1 | 0 | principal phase error |
| 1 | 1 | both auxiliary and principal |

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Table 4 Fast and normal charge pumps current ratio (note 1)

| CR1 | CR0 | I _{CPA} | I _{CPP} | I _{CPPF} | I _{CPPF} : I _{CPP} |
|-----|-----|----------------------|----------------------|-----------------------|--------------------------------------|
| 0 | 0 | 4 × I _{SET} | 4 × I _{SET} | 16 × I _{SET} | 4 : 1 |
| 0 | 1 | 4 × I _{SET} | 4 × I _{SET} | 32 × I _{SET} | 8 : 1 |
| 1 | 0 | 4 × I _{SET} | 2 × I _{SET} | 24 × I _{SET} | 12 : 1 |
| 1 | 1 | 4 × I _{SET} | 2 × I _{SET} | 32 × I _{SET} | 16 : 1 |

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

| AOFF | POFF | FAST | PRINCIPAL DIVIDERS | AUXILIARY DIVIDERS | PUMP CPA | PUMP CPP | PUMP CPPF | DAC AND BIAS |
|------|------|------|--------------------|--------------------|----------|----------|-----------|--------------|
| 1 | 1 | X | OFF | OFF | OFF | OFF | OFF | OFF |
| 1 | 0 | 0 | ON | OFF | OFF | ON | OFF | ON |
| 1 | 0 | 1 | ON | OFF | OFF | ON | ON | ON |
| 0 | 1 | X | OFF | ON | ON | OFF | OFF | ON |
| 0 | 0 | 0 | ON | ON | ON | ON | OFF | ON |
| 0 | 0 | 1 | ON | ON | ON | ON | ON | ON |

Digital-to-analog converter

The 7-bits loaded via the bus into the appropriate latch drive a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $2 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The bandgap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 k Ω // 20 pF load.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5, POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down, the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|--------------------|---|------|----------------|------|
| V_{DD} | digital supply voltage | -0.3 | +5.5 | V |
| V_{CC} | analog supply voltage | -0.3 | +5.5 | V |
| ΔV_{CC-DD} | difference in voltage between V_{CC} and V_{DD} | -0.3 | +5.5 | V |
| V_n | voltage at pins 1, 6, 8 to 15, 19 and 20 | -0.3 | $V_{DD} + 0.3$ | V |
| $V_{2,3,17}$ | voltage at pins 2, 3 and 17 | -0.3 | $V_{CC} + 0.3$ | V |
| ΔV_{GND} | difference in voltage between AGND and DGND (these pins should be connected together) | -0.3 | +0.3 | V |
| P_{tot} | total power dissipation | - | 150 | mW |
| T_{stg} | storage temperature | -55 | +125 | °C |
| T_{amb} | operating ambient temperature | -30 | +85 | °C |
| T_j | maximum junction temperature | - | 95 | °C |

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient in free air | 120 | K/W |

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CHARACTERISTICS
 $V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|--|------|------|--------|------------|
| Supply; pins 4, 5 and 18 | | | | | | |
| V_{DD} | digital supply voltage | $V_{DD1} = V_{DD2}$ | 2.7 | – | 5.5 | V |
| V_{CC} | analog supply voltage | $V_{CC} \geq V_{DD}$ | 2.7 | – | 5.5 | V |
| I_{DD} | principal synthesizer digital supply current | $V_{DD} = 5.5$ V | – | 9 | 12.5 | mA |
| | auxiliary synthesizer digital supply current | $V_{DD} = 5.5$ V | – | 2.7 | 4.0 | mA |
| I_{CC} | charge pumps supply current | $V_{CC} = 5.5$ V; $R_{ext} = 12$ k Ω | – | 0.4 | 1.0 | mA |
| I_{CCPD}, I_{DDPD} | current in power-down mode per supply | logic levels 0 or V_{DD} | – | 12 | 50 | μ A |
| RF principal main divider input; pin 6 | | | | | | |
| f_{VCO} | RF input frequency | | 1700 | – | 2400 | MHz |
| $V_{6(rms)}$ | AC-coupled input signal level (RMS value) | $R_s = 50$ Ω ; 1.7 GHz < f_{VCO} < 2.0 GHz | 60 | – | 400 | mV |
| | | $R_s = 50$ Ω ; 2.0 GHz < f_{VCO} < 2.4 GHz | 60 | – | 180 | mV |
| Z_I | input impedance (real part) | $f_{VCO} = 2$ GHz | – | 300 | – | Ω |
| C_I | typical pin input capacitance | indicative, not tested | – | 2 | – | pF |
| R_{pm} | principal main divider ratio | | 512 | – | 131071 | |
| f_{PPCmax} | maximum principal phase comparator frequency | | – | 2000 | – | kHz |
| f_{PPCmin} | minimum principal phase comparator frequency | | – | 10 | – | kHz |
| Auxiliary main divider input; pin 15 | | | | | | |
| f_{AI} | input frequency | | 20 | – | 300 | MHz |
| $V_{15(rms)}$ | AC-coupled input signal level (RMS value) | $R_s = 50$ Ω ; 2.7 V < V_{DD} < 3.5 V | 50 | – | 500 | mV |
| | | $R_s = 50$ Ω ; 3.5 V < V_{DD} < 5.5 V | 100 | – | 500 | mV |
| Z_I | input impedance (real part) | $f_{AI} = 100$ MHz | – | 1 | – | k Ω |
| C_I | typical pin input capacitance | indicative, not tested | – | 2 | – | pF |
| R_{am} | auxiliary main divider ratio | | 64 | – | 16383 | |
| f_{APCmax} | maximum auxiliary phase comparator frequency | | – | 2000 | – | kHz |
| f_{APCmin} | minimum auxiliary phase comparator frequency | | – | 10 | – | kHz |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|--------------------------------|----------------------|--------------------|----------------------|---------------|
| Crystal reference dividers input; pin 8 | | | | | | |
| f_{XTAL} | input frequency range from crystal | | 5 | – | 40 | MHz |
| $V_{8(rms)}$ | sinusoidal input signal level (RMS value) | $V_{6(rms)} < 224 \text{ mV}$ | 50 | – | 500 | mV |
| | | $V_{6(rms)} > 224 \text{ mV}$ | 100 | – | 500 | mV |
| Z_I | input impedance (real part) | $f_{XTAL} = 30 \text{ MHz}$ | – | 2 | – | k Ω |
| C_I | typical pin input capacitance | indicative, not tested | – | 2 | – | pF |
| R_{pr} | principal reference division ratio | | 8 | – | 2047 | |
| R_{ar} | auxiliary reference division ratio | | 8 | – | 2047 | |
| Charge pump current setting resistor input; pin 14 | | | | | | |
| R_{ext} | external resistor from pin 14 to ground | | 12 | – | 60 | k Ω |
| V_{14} | regulated voltage at pin 14 | $R_{ext} = 12 \text{ k}\Omega$ | – | 1.15 | – | V |
| Charge pump outputs; pins 17, 3 and 2; $R_{ext} = 12 \text{ k}\Omega$ | | | | | | |
| I_{Ocp} | charge pump output current error | | –25 | – | +25 | % |
| I_{match} | sink-to-source current matching | V_{cp} in range | – | ± 5 | – | % |
| I_{Lcp} | charge pump off leakage current | $V_{cp} = \frac{1}{2}V_{CC}$ | –5 | ± 1 | +5 | nA |
| V_{cp} | charge pump voltage compliance | | 0.4 | – | $V_{CC} - 0.4$ | V |
| Interface logic input signal levels; pins 13, 12, 11 and 1 | | | | | | |
| V_{IH} | HIGH level input voltage | | $0.7V_{DD}$ | – | $V_{DD} + 0.3$ | V |
| V_{IL} | LOW level input voltage | | –0.3 | – | $0.3V_{DD}$ | V |
| I_{bias} | input bias current | logic 1 or logic 0 | –5 | – | +5 | μA |
| C_I | input capacitance | indicative, not tested | – | 2 | – | pF |
| DAC output signal levels; pin 10, $R_{ext} = 12$ to $24 \text{ k}\Omega$ | | | | | | |
| I_{DAC} | DAC full scale output current | | $1.5 \times I_{SET}$ | $2 \times I_{SET}$ | $2.5 \times I_{SET}$ | mA |
| V_{10} | output voltage compliance | all codes | 0 | – | $V_{DD} - 0.4$ | V |
| I_{10min} | minimum DAC current | 00 code | – | 2 | 5 | μA |
| I_{monot} | worst case monotonicity test: $\Delta I \times \frac{128}{2 \times I_{SET}}$ | note 1 | 0.1 | – | 1.9 | |
| Lock detect output signal; pin 20 open-drain output | | | | | | |
| V_{OL} | LOW level output voltage | $I_{sink} = 0.4 \text{ mA}$ | – | – | 0.4 | V |

Note

- ΔI is the change in DAC output current when making the code transitions: 3FH/40H or 1FH/20H.

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SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---------------------------------------|---------------------|------|------|------|
| Serial programming clock; CLK | | | | | |
| t_r | input rise time | – | 10 | 40 | ns |
| t_f | input fall time | – | 10 | 40 | ns |
| T_{cy} | clock period | 100 | – | – | ns |
| Enable programming; \bar{E} | | | | | |
| t_{START} | delay to rising clock edge | 40 | – | – | ns |
| t_{END} | delay from last falling clock edge | –20 | – | – | ns |
| t_W | minimum inactive pulse width | 4000 ⁽¹⁾ | – | – | ns |
| $t_{SU;\bar{E}}$ | enable set-up time to next clock edge | 20 | – | – | ns |
| Register serial input data; DATA | | | | | |
| $t_{SU;DAT}$ | input data to clock set-up time | 20 | – | – | ns |
| $t_{HD;DAT}$ | input data to clock hold time | 20 | – | – | ns |

Note

1. The minimum pulse width (t_W) can be smaller than 4 μs provided all the following conditions are satisfied:

- a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$
- b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$
- c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$

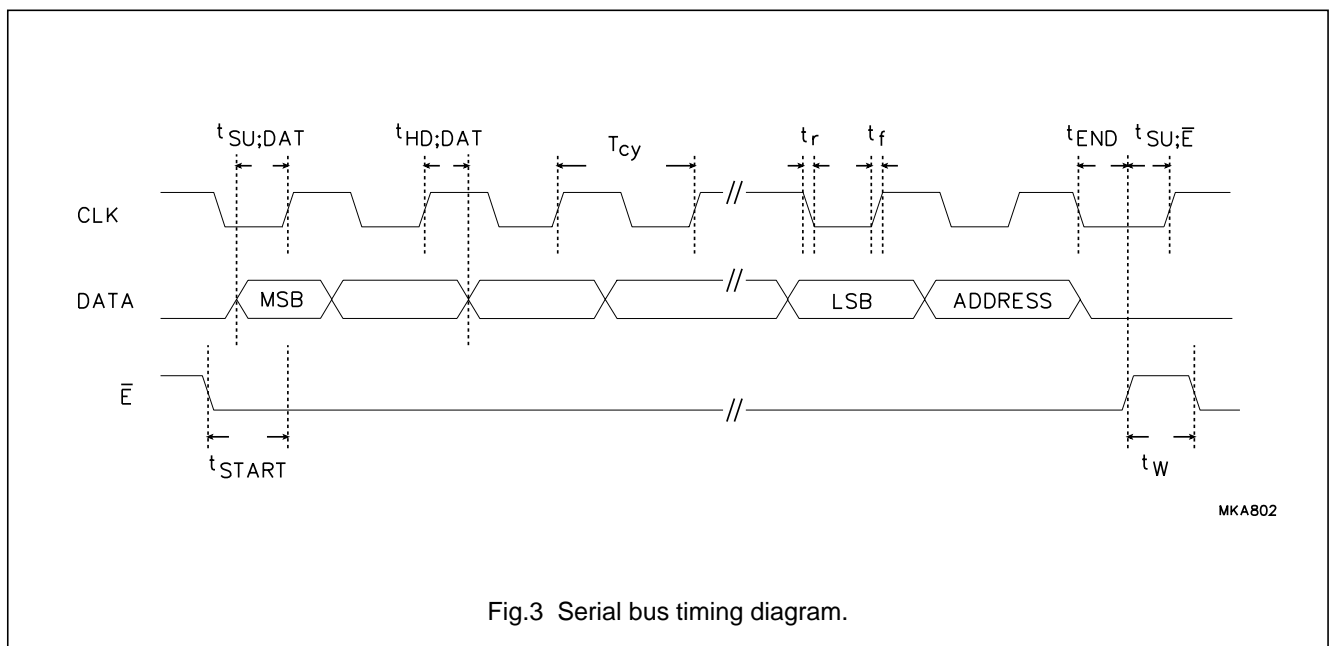


Fig.3 Serial bus timing diagram.

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APPLICATION INFORMATION

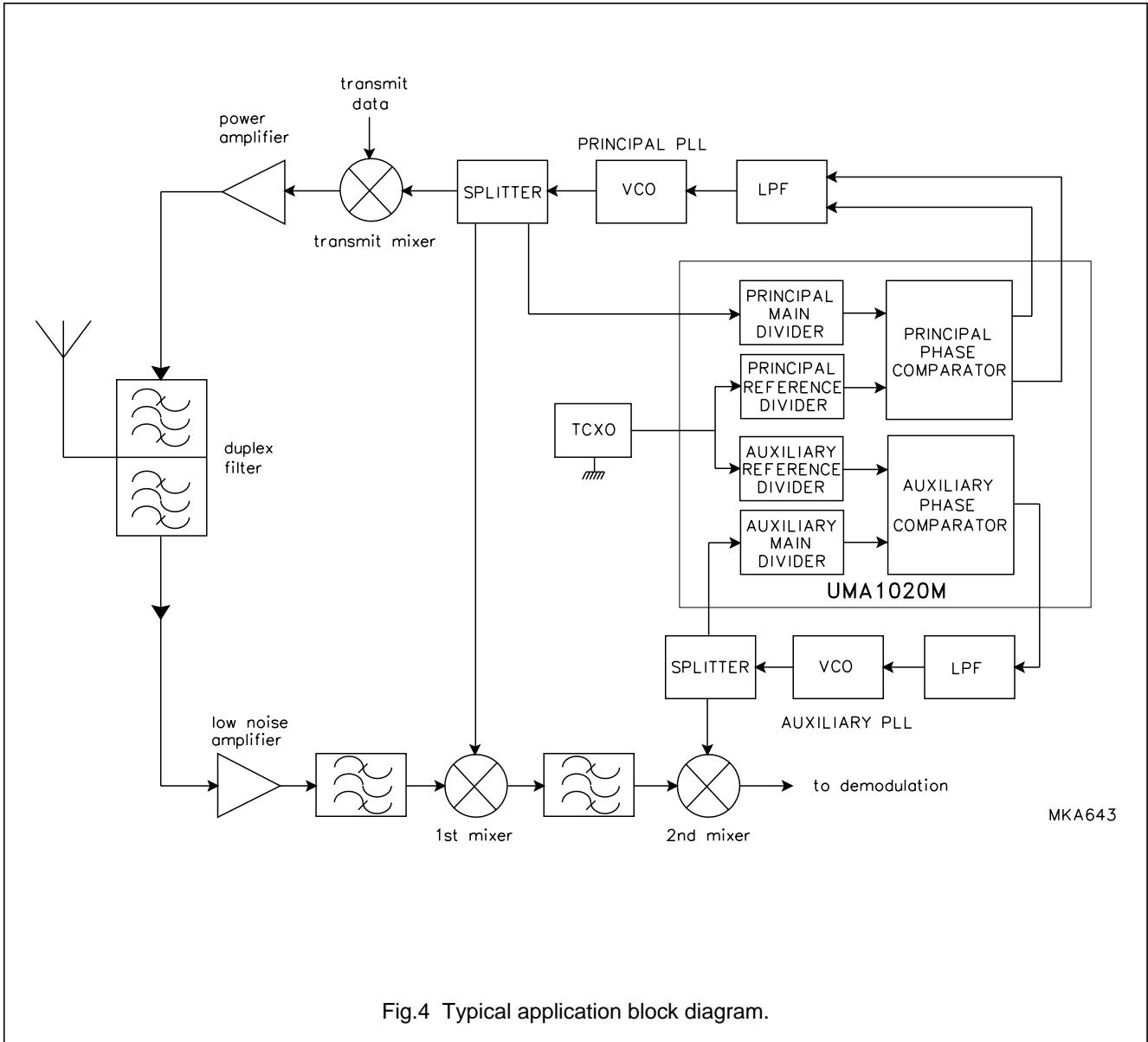


Fig.4 Typical application block diagram.

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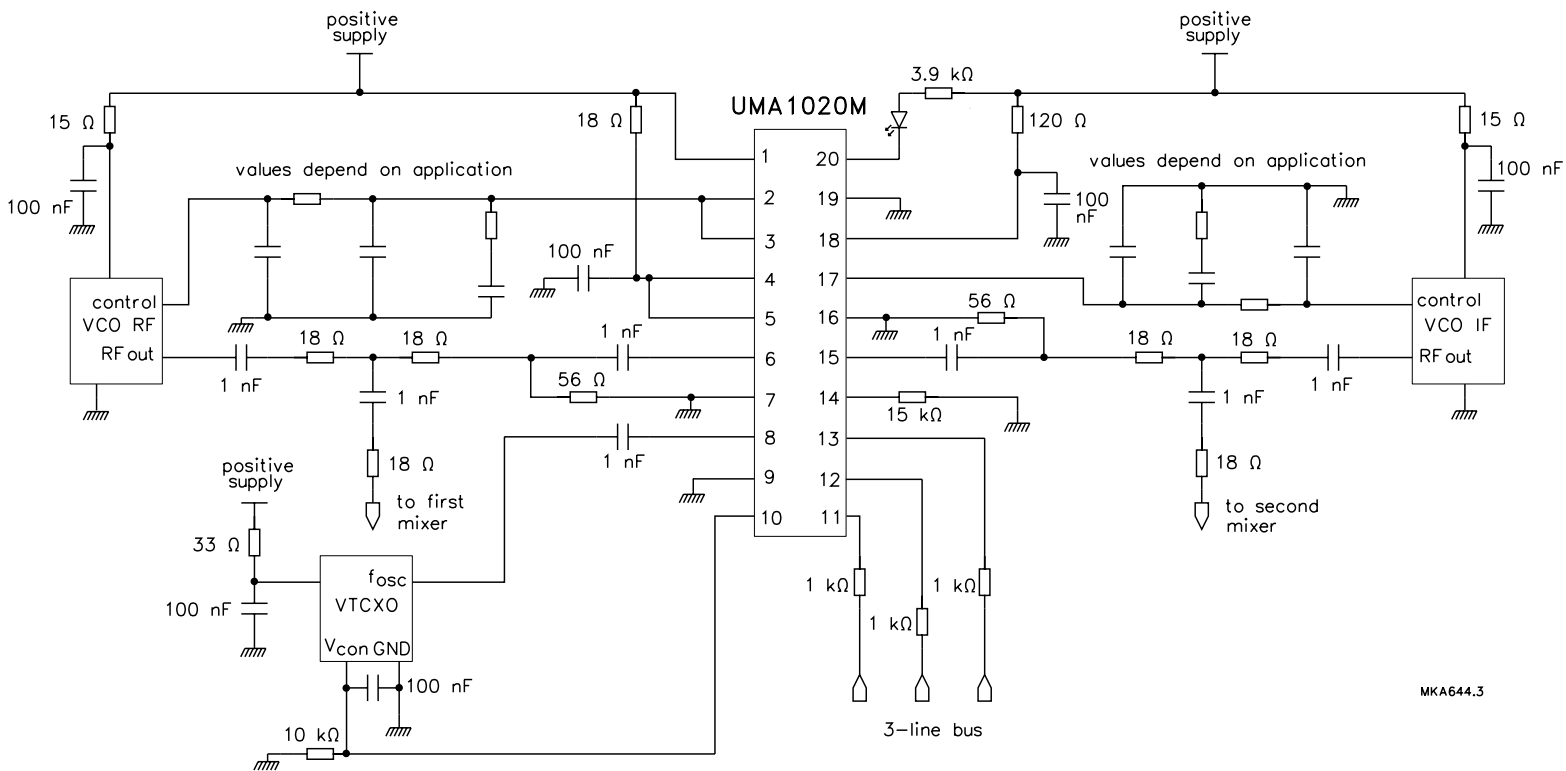


Fig.5 Typical test and application diagram.

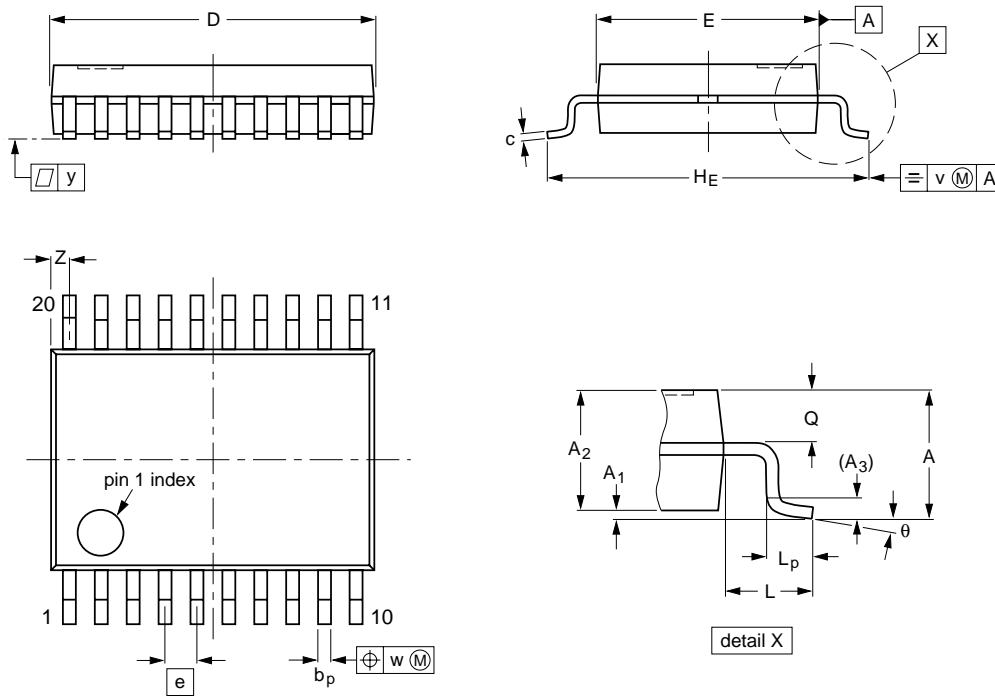
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PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|-----|----------------|--------------|-----|------|-----|------------------|-----------|
| mm | 1.5 | 0.15 0 | 1.4 1.2 | 0.25 | 0.32 0.20 | 0.20 0.13 | 6.6 6.4 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.45 | 0.65 0.45 | 0.2 | 0.13 | 0.1 | 0.48 0.18 | 10° 0° |

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT266-1 | | | | | | 90-04-05 95-02-25 |

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SOLDERING SO or SSOP

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

SSOP

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

METHOD (SO OR SSOP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at 270 to 320 °C.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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Low-voltage dual frequency
synthesizer for radio telephones

UMA1020M

NOTES

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NOTES

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