■ OVERVIEW

The SM8513 is an asynchronous/synchronous (ASYNC/SYNC) converter LSI fabricated using NPC's original molybdenum-gate CMOS technology and complies with ITU-T Recommendation V.14.

At various modem data communication speeds ranging from 600 bps to 19.2 Kbps, etc., the LSI converts a synchronous signal to asynchronous signal, and vice versa. The SM8513 allows mutual conversion between synchronous and asynchronous signals according to the 8, 9, 10 and 11-bit asynchronous signal character format. It also supports the basic signal speed range complying with ITU-T Recommendation V.14, optional extended signal speed range and halt signal automatic extension.

■ FEATURES

○ Compliance with ITU-T Recommendation V.14
  • Conversion from SYNC signal to ASYNC signal, and vice versa
  • Compatible with communication speeds ranging from 600 bps to 19.2 Kbps
  • Bypass mode for signals at speeds below 300 bps
    (SYNC/ASYNC signal conversion is not performed in the bypass mode.)
  • 8-bit to 11-bit ASYNC signal character format
  • Supports both basic signal speed range and extended signal speed range.
  • Supports automatic extension of halt signal.
○ A crystal or an external clock may be used as the system clock.
○ Single +5 V power supply
○ Available in two package types:
  • 16-pin plastic DIP (SM8513P)
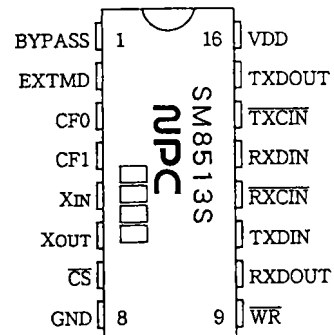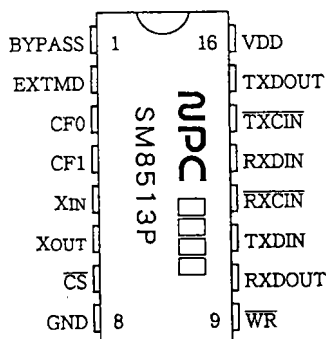 • 16-pin plastic SOP (SM8513S)

■ APPLICATION

  • Conversion of SYNC signal to ASYNC signal, and vice versa, between the modem and the terminal (compatible with 600, 1200, 2400, 4800, 7200, 9600, 14400, 19200 bps)
  • Protocol converters
  • Personal computers
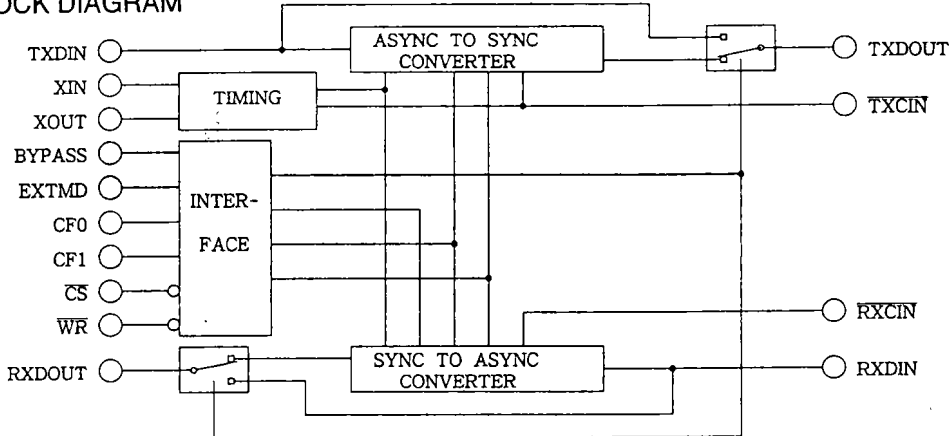 • Synchronous terminals

■ PINOUT   TOP VIEW

• 16-pin DIP

BYPASS	1		16	VDD
EXTMD		SM8513P		TXDOUT
CF0				$\overline{TXCIN}$
CF1				RXDIN
XIN				$\overline{RXCIN}$
XOUT				TXDIN
$\overline{CS}$				RXDOUT
GND	8		9	$\overline{WR}$

• 16-pin SOP

BYPASS	1		16	VDD
EXTMD		SM8513S		TXDOUT
CF0				$\overline{TXCIN}$
CF1				RXDIN
XIN				$\overline{RXCIN}$
XOUT				TXDIN
$\overline{CS}$				RXDOUT
GND	8		9	$\overline{WR}$

■ BLOCK DIAGRAM

■ PIN DESCRIPTION

No.	Name	Description

1	BYPASS	Bypass mode specification (interface register). Bring this pin High when the speed is 300 bps or less (may be more than 300 bps).
		    Lo: Normal mode
		    Hi: Bypass mode (no SYNC/ASYNC conversion)

2	EXTMD	Specifies the allowable speed fluctuation range (interface register). Set the allowable range of speed fluctuations at the time of ASYNC signal reception.
		    Lo: Basic signal speed range (+1.0% to -2.5%)
		    Hi: Extended signal speed range (+2.3% to -2.5%)

3/4	CF0/CF1	Character format selection (interface register). Set the character format (M) of the ASYNC signal. *: Actual processing: 1 stop bit + 8 data bits + 2 stop bits
5	XIN	Oscillation input. Connect a 11.0592 MHz crystal between XIN and XOUT or connect an external clock to XIN.
6	XOUT	Oscillation output

7	$\overline{CS}$	Chip select input
		<CPU in use>
		    Bring $\overline{CS}$ Low to write data in interface registers at pins 1 to 4. Connect decoded addresses from the CPU in normal operation.
		<CPU not in use>
		    Connect this pin to the ground.

8	GND	Ground

9	$\overline{WR}$	Write enable
		<CPU in use>
		    Data of pins 1 to 4 (interface registers) is input when the $\overline{CS}$ pin is active and the $\overline{WR}$ pin goes Low. The data is latched when $\overline{WR}$ goes from Low to High.
		<CPU not in use>
		    Connect this pin to the ground. The states of pin 1 to 4 become valid at the moment a change is made.

10	RXDOUT	ASYNC signal output
11	TXDIN	ASYNC signal input
12	$\overline{RXCIN}$	SYNC signal reception clock input
13	RXDIN	SYNC signal input
14	$\overline{TXCIN}$	SYNC signal transmission clock input
15	TXDOUT	SYNC signal output
16	VDD	+5 V supply voltage

Character format selection table (for pins 3/4):

CF1/CF0		Character format (M)	Start bit	Data bit	Stop bit	
Lo	Lo	8	1	6	1	
Lo	Hi	9	1	7	1	
Hi	Lo	10	1	8	1	
Hi	Hi	11	1	9	1	*

■ ABSOLUTE MAXIMUM RATINGS

$(V_{SS} = 0V)$

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.3 to 7.0	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Power dissipation	P_W	250	mW
Operating temperature	T_a	0 to +70	°C
Storage temperature	T_{STG}	-65 to +150	°C
Soldering temperature	T_{SLD}	255	°C
Soldering time	t_{SLD}	10	Sec

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	4.5 to 5.5	V
Operating temperature	T_a	0 to +70	°C
Crystal frequency	f_{XT}	11.0592±0.01%	MHz

■ DC CHARACTERISTICS

$(V_{DD} = 5 V \pm 10\%, T_a = 0$ to +70 °C, $f_{XT} = 11.0592$ MHz, $C_x = 10$ pF unless otherwise noted.)

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input voltage	Lo	V_{IL}			0.8	V	All input pins other than XIN
		V_{ILX}			$0.3V_{SS}$	V	XIN only
	Hi	V_{IH}	2.0			V	All input pins other than XIN
		V_{IHX}	$0.7V_{DD}$			V	XIN only
Output voltage	Lo	V_{OL}			0.1	V	All output pins other than XOUT $I_{OL}=20\mu A$, $V_{IN}=V_{HI}/V_{HL}$
					0.4	V	All output pins other than XOUT $I_{OL}=40mA$, $V_{IN}=V_{HI}/V_{HL}$
	Hi	V_{OH}	$V_{DD}-0.1$			V	All output pins other than XOUT $I_{OH}=20\mu A$, $V_{IN}=V_{HI}/V_{HL}$
			3.7			V	All output pins other than XOUT $I_{OL}=40mA$, $V_{IN}=V_{HI}/V_{HL}$
Output impedance		R_O		500		Ω	XOUT pin only
Input current		I_{IN}			10	μA	$V_{IN}=0V$ or V_{DD} All input pins other than XIN
				6		μA	$V_{IN}=0V$ or V_{DD} XIN pin only
Current consumption	In operation	I_{DD}		2	5	mA	All output pins OPEN All input pins LOW
	Not in operation	I_{DQ}		1		μA	All output pins 0 V XIN=V_{DD}

■ AC CHARACTERISTICS

(V_{DD} = 5 V ±10%, Ta = 0 to +70 °C, f_{XT} = 11.0592 MHz, Cx = 10 pF, $\overline{TXCIN}=\overline{RXCIN}=1200$bps, C_L=15pF*1)

| ITEM		SYMBOL	MIN	TYP		MAX	UNIT	CONDITION
Signal speed range		f_S		600 1200 2400 4800	7200 9600 14400 19200		bps	*3
Allowable speed fluctuation range		d_{FSSY}	-0.01			0.01	%	SYNC signal side
		d_{FSAY}	-2.5			1.0		ASYNC signal side/EXTMD=0
			-2.5			2.3		ASYNC signal side/EXTMD=1
Stop bit		t_{STOP}	0.875T					EXTMD=0, T=1/fS
			0.750T					EXTMD=1, T=1/fS
Data setup time		t_S	0				ns	See Figure 1 CPU interface.
Data hold time		t_H	20				ns	See Figure 1 CPU interface.
$\overline{WR}$ pulse width		t_{WW}	100				ns	See Figure 1 CPU interface.
$\overline{CS}$ pulse width		t_{WC}	140				ns	See Figure 1 CPU interface.
$\overline{CS}$ access time		t_A	20				ns	See Figure 1 CPU interface.
$\overline{CS}$ release time		t_R	20				ns	See Figure 1 CPU interface.
TXDOUT delay time		t_{DTX}				1	μs	See Figure 1 Normal mode.*3
RXDIN setup time		t_{SRX}	1				μs	See Figure 1 Normal mode.*3
RXDIN hold time		t_{HRX}	1				μs	See Figure 1 Normal mode.*3
TXDOUT	Delay time	t_{DX}				1	μs	Each data input. See Figure 1 Bypass mode.*4
RXDOUT	Delay time				M*2		bit	TXDIN to TXDOUT*3 See Figure 7.
	length				2M*2		bit	RXDIN to RXDOUT*3 See Figure 8.

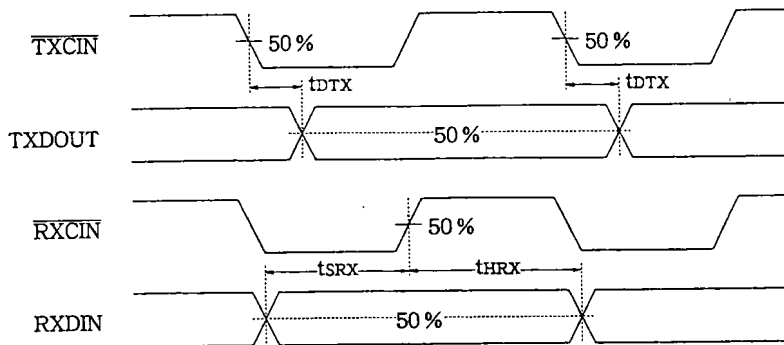*1: CL is the load capacity of TXDOUT/RXDOUT.
*2: M is the character format.
*3: BYPASS = 0
*4: BYPASS = 1

● CPU interface
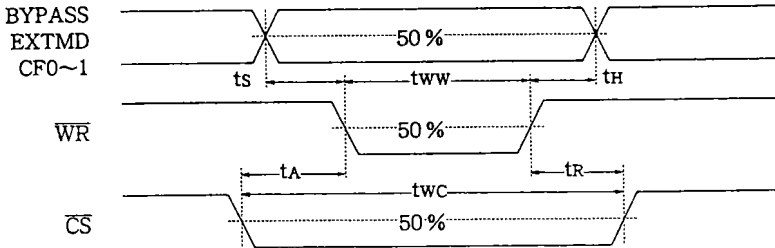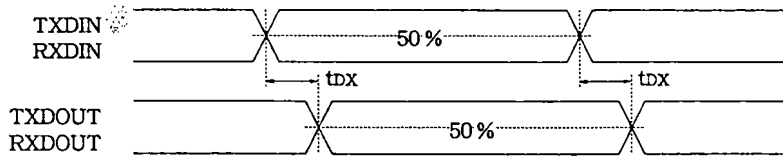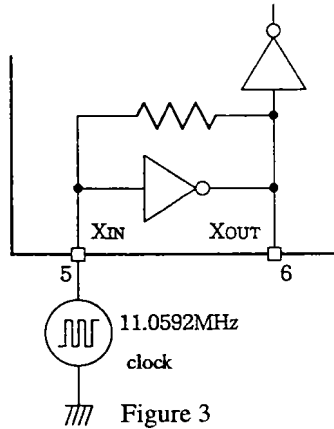

● Normal mode (BYPASS = 0)
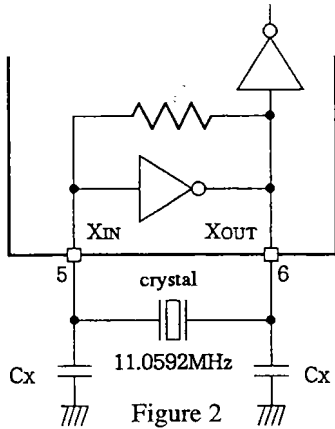
● Bypass mode (BYPASS = 1)

Figure 1 Timing waveform

■ OSCILLATOR CONNECTION CIRCUIT

Figure 2

Figure 3

System clock selection

(1) Crystal

Connect a crystal between XIN and XOUT as shown in Figure 2.
Use 10 pF capacitors (Cx).

(2) External clock signal

Input an external clock to the XIN pin as shown in Figure 3.

■ CHARACTER FORMAT

1. Asynchronous character format

Transmission/reception of an ASYNC signal starts from the start bit (1-bit length) and ends at the stop bit (1 to 2-bit length), as shown in Figure 4. Therefore, the synchronizing clock is not necessary for data input or sending.
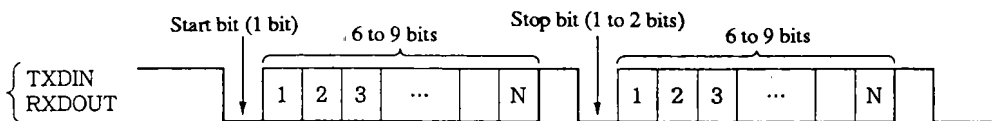

Figure 4 Asynchronous signal character format

2. Synchronous character format

Transmission/reception timing of synchronous data is synchronized by the transmission clock (EIA RS-232C, pin 15) and the reception clock (pin 17) supplied to $\overline{\text{TXCIN}}$ and $\overline{\text{RXCIN}}$, respectively.
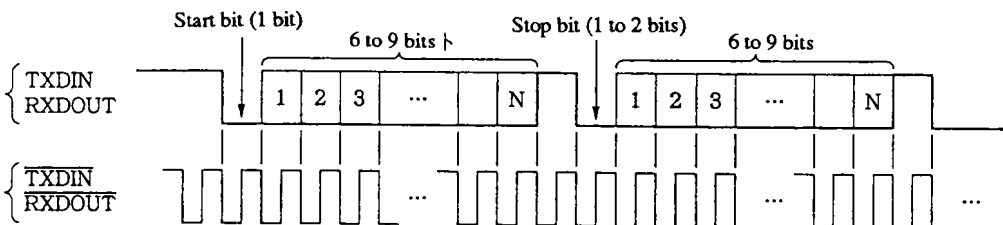

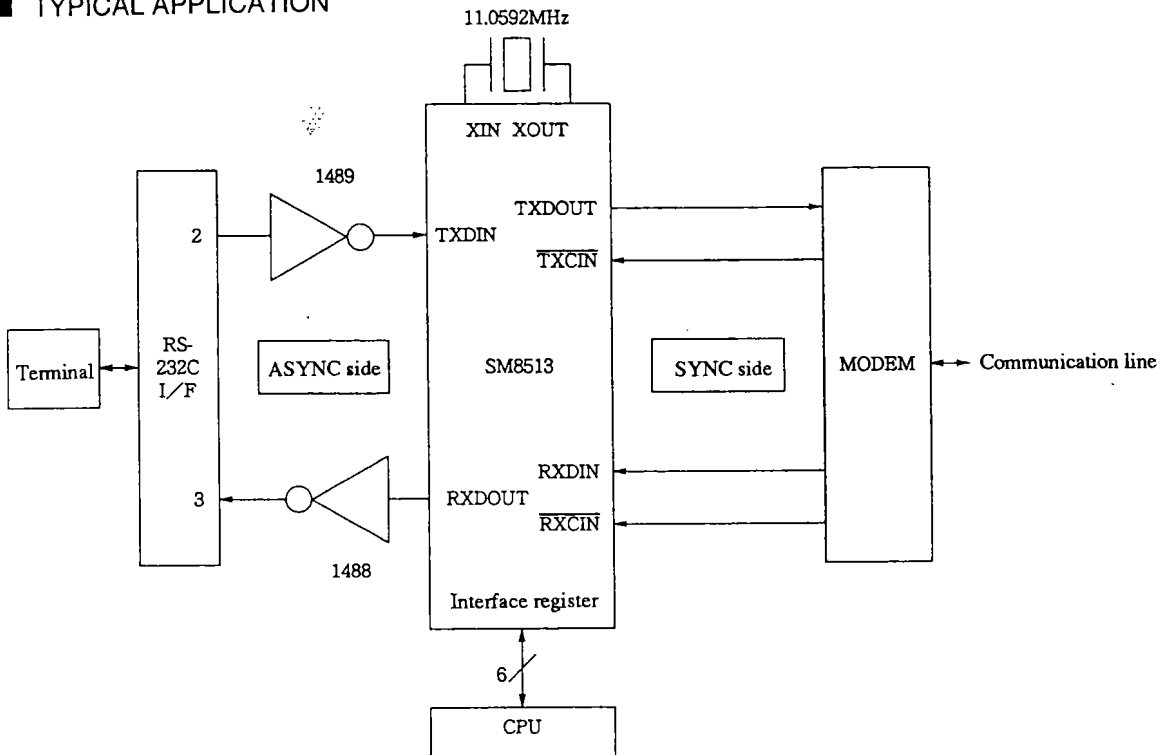Figure 5 Synchronous signal character format

■ TYPICAL APPLICATION

Figure 6 SM8513 application circuit example

■ INTERFACE REGISTER

The SM8513 has four CPU interface registers--BYPASS, EXTMD, CF0 and CF1--at pins 1, 2, 3 and 4, respectively. These registers can be controlled by the CPU with the $\overline{WR}$ pin and the $\overline{CS}$ pin.

(1) CPU control

Data at pins 1 to 4 is input when both $\overline{WR}$ and $\overline{CS}$ go Low.

The data is latched in the registers when $\overline{WR}$ and $\overline{CS}$ go High.

(See Figure 1 CPU interface for details of the timing.)

(2) No CPU control

Connect the $\overline{WR}$ and $\overline{CS}$ pins to the ground. Data becomes valid when pins 1 to 4 are changed.

■ ASYNC/SYNC CONVERSION

● Operation range

In the ASYNC mode, data transmission/reception timing is not as strict as that of the SYNC mode (0.01%). Therefore, the speed varies in the ASYNC mode, which causes a difference in speed between the ASYNC and SYNC mode. To cope with speed fluctuations in the ASYNC system, the SM8513 is designed to absorb speed differences in the following ranges, as specified in ITU-T Recommendation V.14.

(1) Speed fluctuations permissible in ASYNC signal reception

Basic signal speed range +1.0 to -2.5%

Extended signal speed range +2.3 to -2.5%

(2) Speed fluctuations permissible in ASYNC signal transmission

Basic signal speed range +1.0%

Extended signal speed range +2.3%

● Conversion from ASYNC signal to SYNC signal
1.   Speed fluctuations of ASYNC signal input
   (1)   Under speed (EXTMD = 0: 0 to -2.5%, EXTMD = 1: 0 to -2.5%)
         When the communication speed of the ASYNC signal input (TXDIN) is slower
         (under speed) than that of the SYNC signal output (TXDOUT), the speed difference
         is absorbed by adding a stop bit (1 bit or more) to the SYNC signal (TXDOUT) at the
         time of transmission.
   (2)   Over speed (EXTMD = 0: +1.0 to 0%, EXTMD = 1: +2.3 to 0%)
         When the communication speed of the ASYNC signal input (TXDIN) is higher (over
         speed) than that of the SYNC signal output (TXDOUT), the speed difference is
         absorbed by deleting a stop bit (maximum 1 bit) from the ASYNC signal as described
         below.
                 Per 8 continuous characters in the basic signal speed range (EXTMD = 0)
                 Per 4 continuous characters in the extended signal speed range (EXTMD = 1)

2.   SYNC signal output delay
     A signal input to the ASYNC signal input pin (TXDIN) is output synchronized with the
     synchronizing clock ($\overline{\text{TXCIN}}$). At this time, the signal transmitted from the SYNC signal
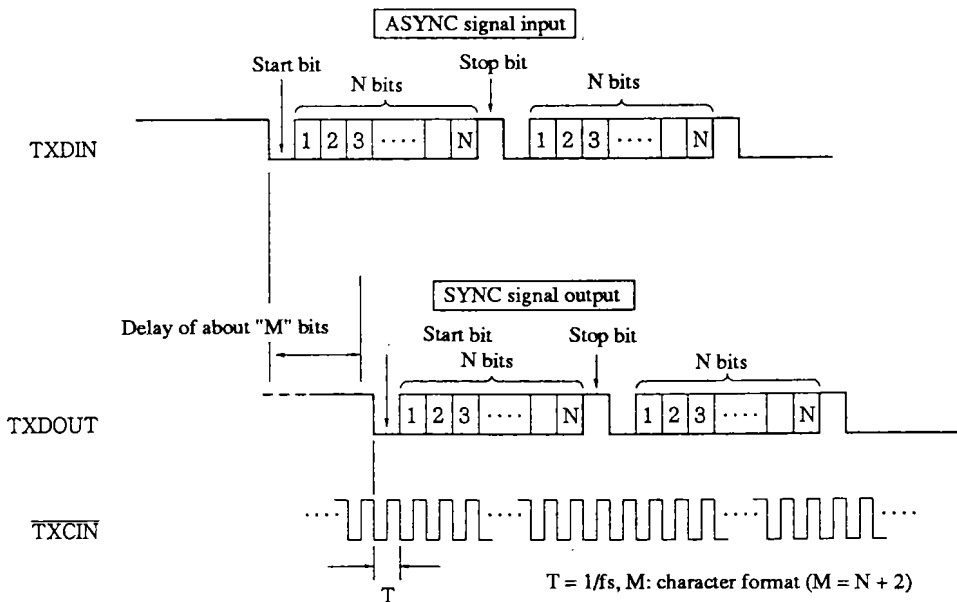   output pin (TXDOUT) has a delay of about "M" bits. (See Figure 7.)

Figure 7 Conversion from ASYNC signal to SYNC signal

● Conversion from SYNC signal to ASYNC signal

  1. Missing stop bit in SYNC signal input

When a signal received at the SYNC signal input pin (RXDIN) is found to have its stop bit missing, a stop bit is inserted at the missing position when converted data is output from the ASYNC signal output pin (RXDOUT). The stop bit to be inserted is shorter than the regular stop bit by the following percentages:

      Basic signal speed range (EXTMD = 0): 12.5%

      Extended signal speed range (EXTMD = 1): 25.0%

At the same time, the stop bit length is made identical to the length of the inserted stop bit for the following numbers of characters. The start bit length and the data bit length are not shortened. (See Figure 8.)

      Basic signal speed range (EXTMD = 0): 7 characters

      Extended signal speed range (EXTMD = 1): 3 characters

  2. ASYNC signal output delay

When a signal is input to the SYNC signal input pin (RXDIN), the signal output from the ASYNC signal output pin (RXDOUT) has a delay of about "2M" bits. (See Figure 8.)
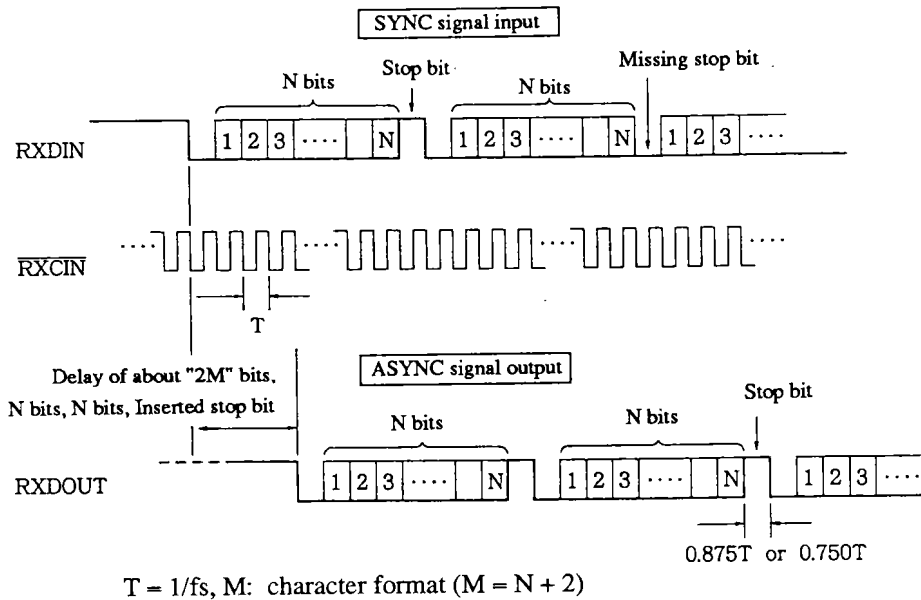

$T = 1/fs$, M: character format $(M = N + 2)$

Figure 8 Conversion from SYNC signal to ASYNC signal

■ HALT SIGNAL

● Conversion from ASYNC signal to SYNC signal

1. When detecting a continuos start polarity of "M to 2M + 3" bits at the ASYNC signal input (TXDIN), the LSI outputs a start polarity of "2M + 3" bits from the SYNC signal output (TXDOUT).
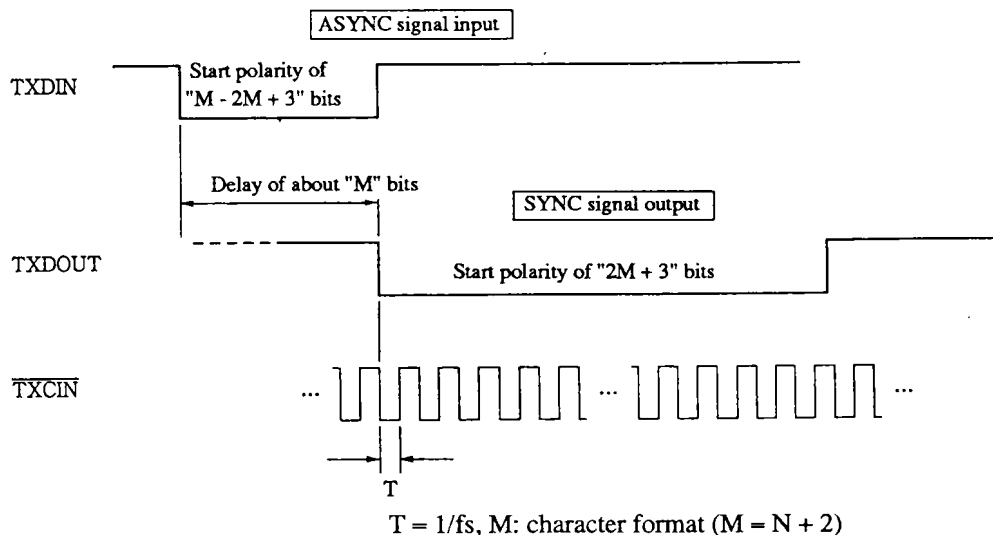

T = 1/fs, M: character format (M = N + 2)

Figure 9 Halt signal sending during ASYNC-to-SYNC signal conversion (1)

2. When the detected start polarity is input continuously for "2M + 3" bits or more, the LSI outputs the start polarity according to its duration.
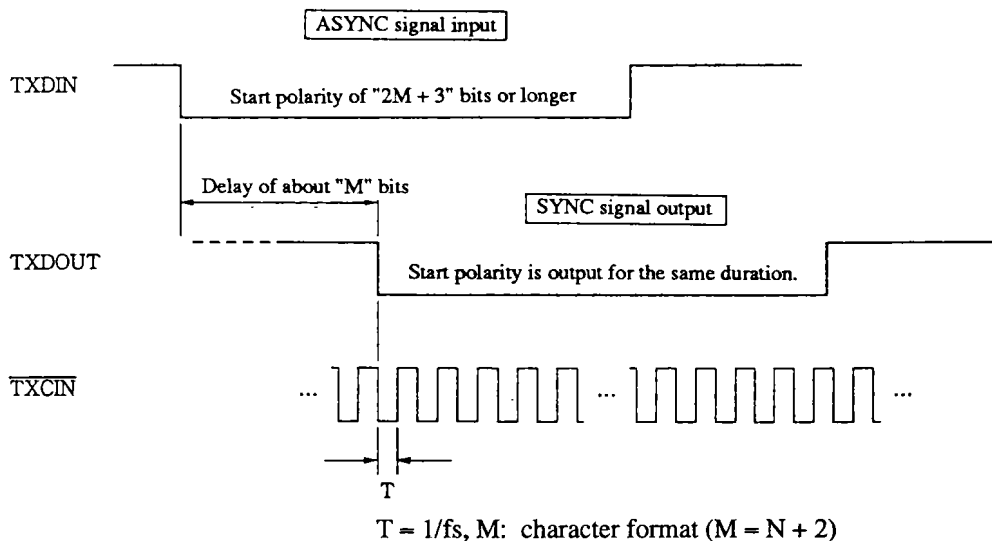

T = 1/fs, M: character format (M = N + 2)

Figure 10 Halt signal sending during ASYNC-to-SYNC signal conversion (2)

● Conversion from SYNC signal to ASYNC signal

When detecting a continuos start polarity of "2M + 3" bits or longer at the SYNC signal input (RXDIN), the LSI outputs a start polarity of the same duration from the ASYNC signal output (RXDOUT).
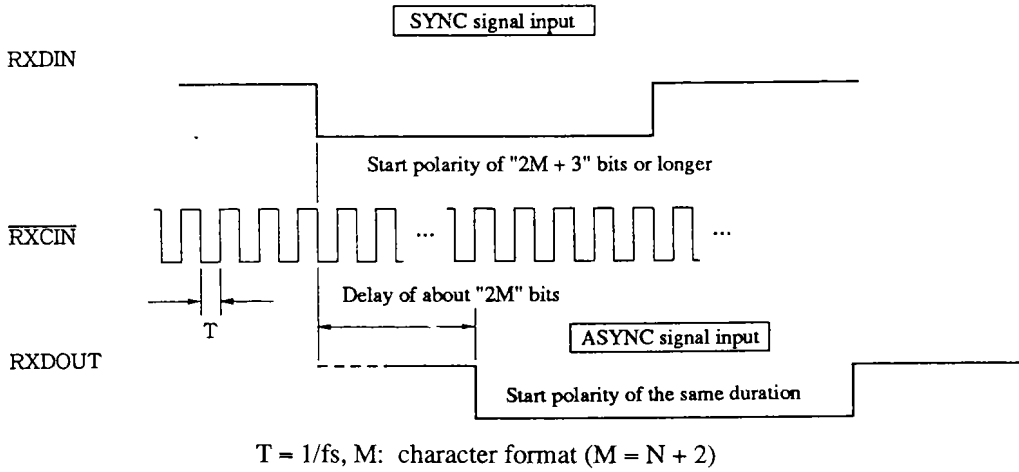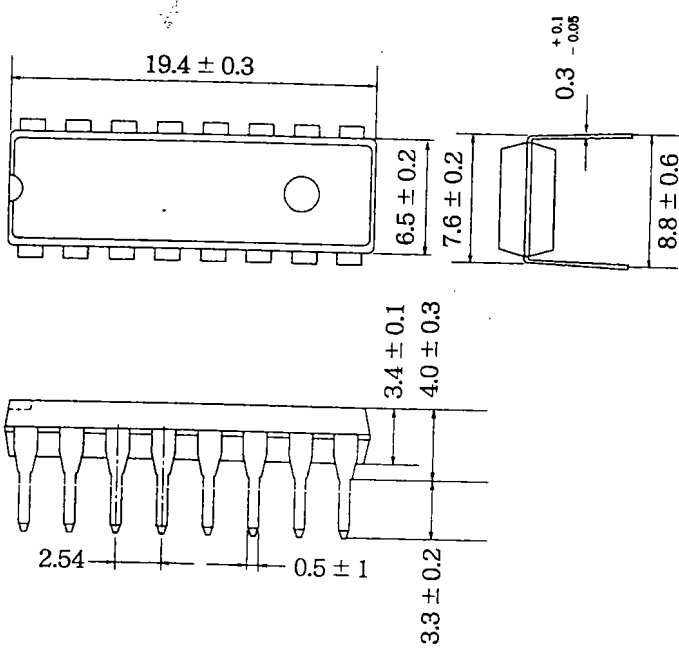

T = 1/fs, M: character format (M = N + 2)

Figure 11 Halt signal sending during SYNC-to-ASYNC signal conversion

■ PACKAGE DIMENSIONS

• SM8513P (16-pin plastic DIP)

19.4 ± 0.3

6.5 ± 0.2

7.6 ± 0.2

$0.3 \begin{smallmatrix} +0.1 \\ -0.05 \end{smallmatrix}$

8.8 ± 0.6

3.4 ± 0.1

4.0 ± 0.3

2.54

0.5 ± 1

3.3 ± 0.2

• SM8513S (16-pin SOP)

10.2 ± 0.3

4.4 ± 0.2

6.2 ± 0.3

$0.15 \begin{smallmatrix} +0.1 \\ -0.05 \end{smallmatrix}$

0.4 ± 0.2

1.5 ± 0.1

0.4 ± 0.1

1.27

0.05 ± 0.05

0 ~ 10°

Enlarged view of the lead