

# HD14538B

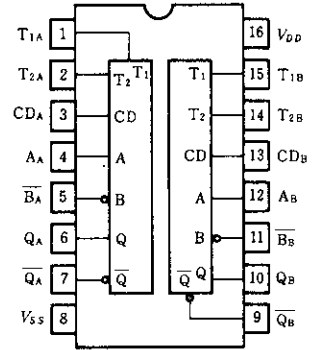
## Dual Precision Retriggerable/Resettable Monostable Multivibrator

The HD14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components,  $C_x$  and  $R_x$ . Linear CMOS techniques allow more precise control of output pulse width.

### FEATURES

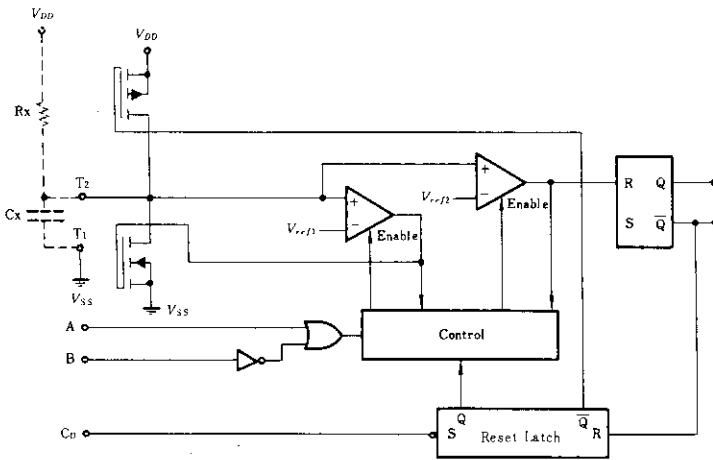
- New Formula:  $PW_{out} = R_x \cdot C_x$
- Pulse Width Range =  $10\mu s$  to  $\infty$
- Quiescent Current =  $5nA/pkg$  typ. @5V
- 3 to 18V Operational Limits
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Compatible with HD14528B

### PIN ARRANGEMENT

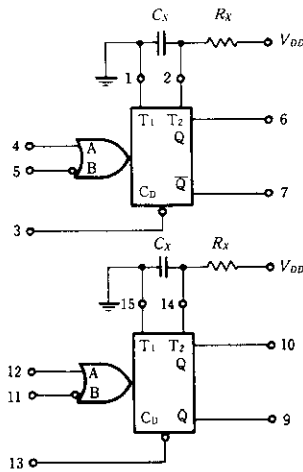


(Top View)

### LOGIC DIAGRAM (1/2)



### BLOCK DIAGRAM



$R_x$  and  $C_x$  are external components.

$V_{DD}$  = Pin 16

$V_{SS}$  = Pin 1, 8, 15

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Output Voltage	$V_{OL}$	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	$V_{OH}$	5.0	$V_{in}=0$ or $V_{DD}$	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	$V_{IL}$	5.0	$V_{out}=4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0	
	$V_{IH}$	5.0	$V_{out}=0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	$I_{OH}$	5.0	$V_{OH}=2.5V$	-2.5	—	-2.1	-4.2	—	-1.7	—	mA
		5.0	$V_{OH}=4.6V$	-0.52	—	-0.44	-0.88	—	-0.36	—	
		10	$V_{OH}=9.5V$	-1.3	—	-1.1	-2.25	—	-0.9	—	
	$I_{OL}$	15	$V_{OH}=13.5V$	-3.6	—	-3.0	-8.8	—	-2.4	—	
		5.0	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—	
15	$V_{OL}=1.5V$	3.6	—	3.0	8.8	—	2.4	—			
Input Current	$I_{in}$	15		—	$\pm 0.3$	—	$\pm 0.0001$	$\pm 0.3$	—	$\pm 1.0$	$\mu A$
Input Capacitance	$C_{in}$	—	$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	$I_{DD}$	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	$\mu A$
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	$I_T$			$I_T(5.0V) = (3.5 \times 10^{-2})R_x \cdot C_x \cdot f + 4C_x \cdot f + 1 \times 10^{-5}C_L \cdot f$ $I_T(10V) = (8 \times 10^{-2})R_x \cdot C_x \cdot f + 9C_x \cdot f + 2 \times 10^{-5}C_L \cdot f$ $I_T(15V) = (1.25 \times 10^{-1})R_x \cdot C_x \cdot f + 12C_x \cdot f + 3 \times 10^{-5}C_L \cdot f$							$\mu A$

$I_T$ :  $\mu A$ ,  $C_x$ :  $\mu F$ ,  $C_L$ : pF,  $R_x$ : k $\Omega$ ,  $f$ : Hz

■ SWITCHING CHARACTERISTICS ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic		Symbol	$C_x$	$R_x(\text{k}\Omega)$	$V_{DD}(\text{V})$	min	typ	max	Unit					
Output Rise Time		$t_r$	—	—	5.0	—	100	200	ns					
					10	—	50	100						
					15	—	40	80						
Output Fall Time		$t_f$	—	—	5.0	—	100	200	ns					
					10	—	50	100						
					15	—	40	80						
Propagation Delay Time	A, B to Q, $\bar{Q}$	$t_{PLH}$ , $t_{PHL}$	—	—	5.0	—	300	600	ns					
					10	—	150	300						
					15	—	100	220						
	$C_D$ to Q, $\bar{Q}$	—	—	5.0	—	250	500							
				10	—	125	250							
				15	—	95	190							
Minimum Input Pulse Width		$PW_{in}$	—	—	5.0	100	50	—	ns					
					10	60	30	—						
					15	50	25	—						
Output Pulse Width					$0.002\mu\text{F}$	100k $\Omega$	5.0	185	200	215	$\mu\text{s}$			
							10	185	200	215				
							15	185	200	215				
							$0.1\mu\text{F}$	100k $\Omega$	5.0	8.8		9.4	10.0	ms
									10	8.8		9.4	10.0	
									15	8.8		9.4	10.0	
					$10\mu\text{F}$	100k $\Omega$	5.0	0.915	0.965	1.015	s			
							10	0.915	0.965	1.015				
							15	0.915	0.965	1.015				
					Minimum Retrigger Time		$t_{rr}$	—	—	5.0	0	—	—	ns
										10	0	—	—	
										15	0	—	—	
External Timing Resistance		$R_x$	—	—	—	5.0	—	OPEN	k $\Omega$					
External Timing Capacitance		$C_x$	—	—	—	2000	—	No Limit	pF					

■ APPLICATIONS

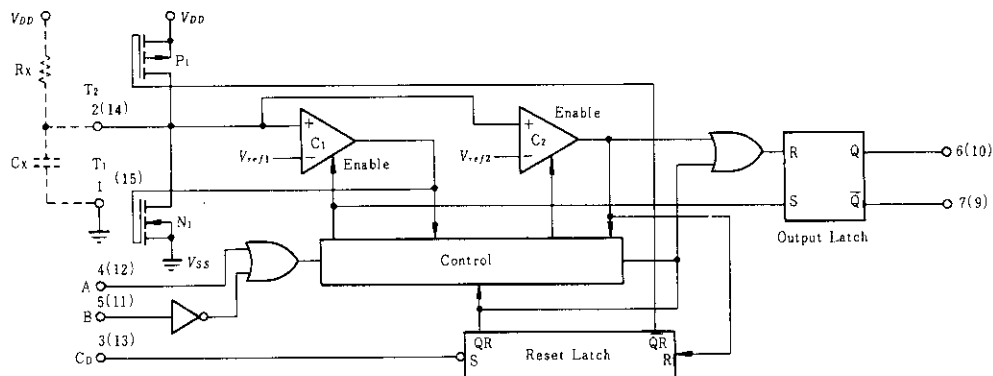


Fig.1 Logic Diagram

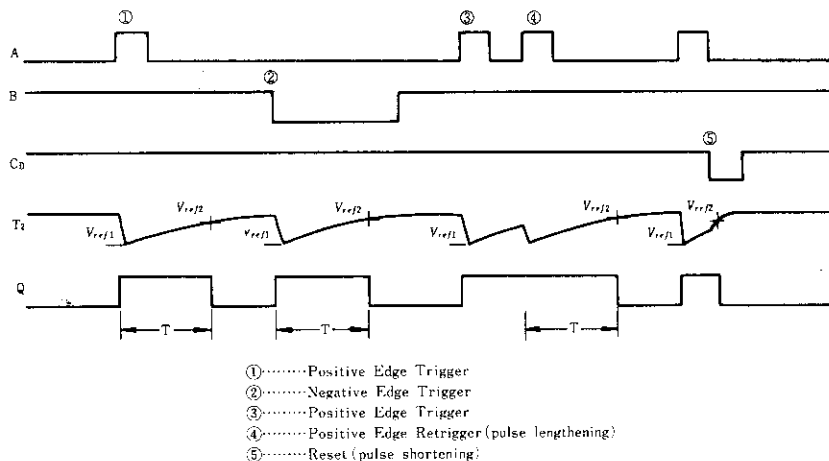


Fig. 2 Timing Operation

### ■ TRIGGER OPERATION

The block diagram of the HD14538B is shown in Figure 1, with circuit operation following. As shown in Figures 1 and 2 before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor Cx completely charged to  $V_{DD}$ . When the trigger input A goes from  $V_{SS}$  to  $V_{DD}$  (while inputs B and  $C_D$  are held to  $V_{DD}$ ) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 ①.

At the same time the output latch is set. With transistor N1 on, the capacitor Cx rapidly discharges toward  $V_{SS}$  until  $V_{ref1}$  is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor Cx begins to charge through the timing resistor, Rx, toward  $V_{DD}$ . When the voltage across Cx equals  $V_{ref2}$ , comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②.

This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger. It should be noted that in the quiescent state Cx is full charged to  $V_{DD}$  causing the current through resistor Rx to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages.

An added feature of the HD14538B is that the output latch is set via the input trigger with out regard to the capacitor voltage. Thus, propagation

delay from trigger to Q is independent of the value of Cx, Rx, or the duty cycle of the input waveform.

### ■ RETRIGGER OPERATION

The HD14538B is retriggered if a valid trigger occurs ③ followed by another valid trigger 4 before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from  $V_{ref1}$ , but has not yet reached  $V_{ref2}$ , will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at T2 will again drop to  $V_{ref1}$  before progressing along the RC charging curve toward  $V_{DD}$ .

The Q output will remain high until time T, after the last valid retrigger.

### ■ RESET OPERATION

The HD14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on  $C_D$  sets the reset latch and causes the capacitor to be fast charged to  $V_{DD}$  by turning on transistor P1 ⑤.

When the voltage on the capacitor reaches  $V_{ref2}$ , the reset latch will clear, and will then be ready to accept another pulse. If the  $C_D$  input is held low, any trigger inputs that occur will be inhibited and the Q and  $\bar{Q}$  outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the  $C_D$  input, the output pulse T can be made significantly shorter than the minimum pulse width specification.



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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