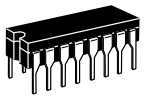
Dual A/D Converter

MC1650
MC1651



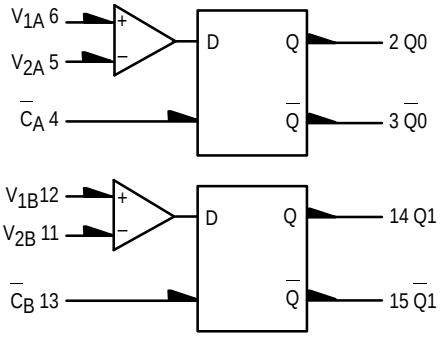
L SUFFIX
CERAMIC PACKAGE
CASE 620–10

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock inputs (C_a and C_b) operate from MECL III or MECL 10,000 digital levels. When C_a is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). Q0 is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

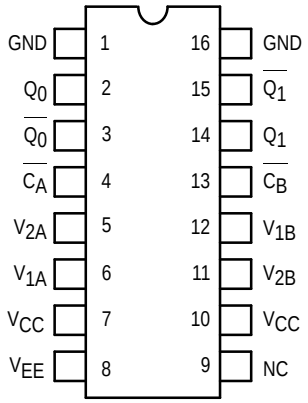
Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

LOGIC DIAGRAM



V_{CC} = +5.0 V = PIN 7, 10
V_{EE} = –5.2 V = PIN 8
GND = PIN 1, 16

PIN ASSIGNMENT



- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (MC1650)
  = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/µs (MC1650)
  = 500 V/µs (MC1651)
- Differential Input Voltage: 5.0 V (–30°C to +85°C)
- Common Mode Range:
  –3.0 V to +2.5 V (–30°C to +85°C) (MC1651)
  –2.5 V to +3.0 V (–30°C to +85°C) (MC1650)
- Resolution: ≤ 20 mV (–30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620).

TRUTH TABLE

$\overline{C}$	V_1 , V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	X X	$Q0_n$	$\overline{Q0}_n$

MOTOROLA

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Test Limits						Unit
			–30°C		+25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	Positive Negative	I_{CC} I_E				25* 55*			mAdc
Input Current	MC1650 MC1651	I_{in}				10 40			µAdc
Input Leakage Current	MC1650 MC1651	I_R				7.0 10.0			µAdc
Clock Input Current		I_{inH}				350			
Output Voltage	Logic 1	V_{OH}	–1.045	–0.875	–0.960	–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	–1.890	–1.650	–1.850	–1.620	–1.830	–1.575	Vdc
Threshold Voltage (Note 2.)	Logic 1	V_{OHA}	–1.065		–0.980		–0.910		Vdc
Threshold Voltage (Note 2.)	Logic 0	V_{OLA}		–1.630		–1.600		–1.555	Vdc

1. All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.
2. These tests are done in order indicated. See Figure 5.
3. Maximum Power Supply Voltages (beyond which device life may be impaired): $|V_{EE}| + |V_{CC}| \geq 12$ Vdc.
4.

All Temperature	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.0	+2.98	–2.5	–2.48
MC1651	+2.5	+2.48	–3.0	–2.98

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)											
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC}[3.]	V_{EE}[3.]
–30°C			–0.875	–1.890	–1.180	–1.515	+0.02	+0.02	See Note 4.				+5.0	–5.2
+25°C			–0.810	–1.850	–1.095	–1.485	+0.02	+0.02					+5.0	–5.2
+85°C			–0.700	–1.830	–1.025	–1.440	+0.02	+0.02					+5.0	–5.2
Characteristic		**Symbol**	TEST VOLTAGE APPLIED TO PINS LISTED BELOW										(V_{CC}) Gnd	
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}		
Power Supply Drain Current	Pos Neg	I_{CC} I_E	 4,13	4,13			6,12 6,12						1,5,11,16 1,5,11,16	
Input Current	MC1650 MC1651	I_{in}	4	13			12		6				1,5,11,16	
Input Leakage Current	MC1650 MC1651	I_R	4	13			12				6		1,5,11,16	
Clock Input Current		I_{inH}	4	13			6,12						1,5,11,16	
Output Voltage	Logic 1	V_{OH}	4,13				6,12 5,11	5,11 6,12	6,12 5,11	5,11 6,12	5,11 6,12	6,12 5,11	1,5,11,16 1,6,12,16 1,16 1,16 1,5,11,16 1,6,12,16 1,16 1,16	
Output Voltage	Logic 0	V_{OL}	4,13				5,11 6,12	6,12 5,11	5,11 6,12	6,12 5,11	6,12 5,11	5,11 6,12	1,5,11,16 1,6,12,16 1,16 1,16 1,5,11,16 1,6,12,16 1,16 1,16	
Threshold Voltage Note 2.	Logic 1	V_{OHA}		13	4 4	 4 4	6 6	 6 6					1,5,16	
Threshold Voltage Note 2.	Logic 0	V_{OLA}		13	4 4	 4 4	6 6	 6 6					1,5,16	

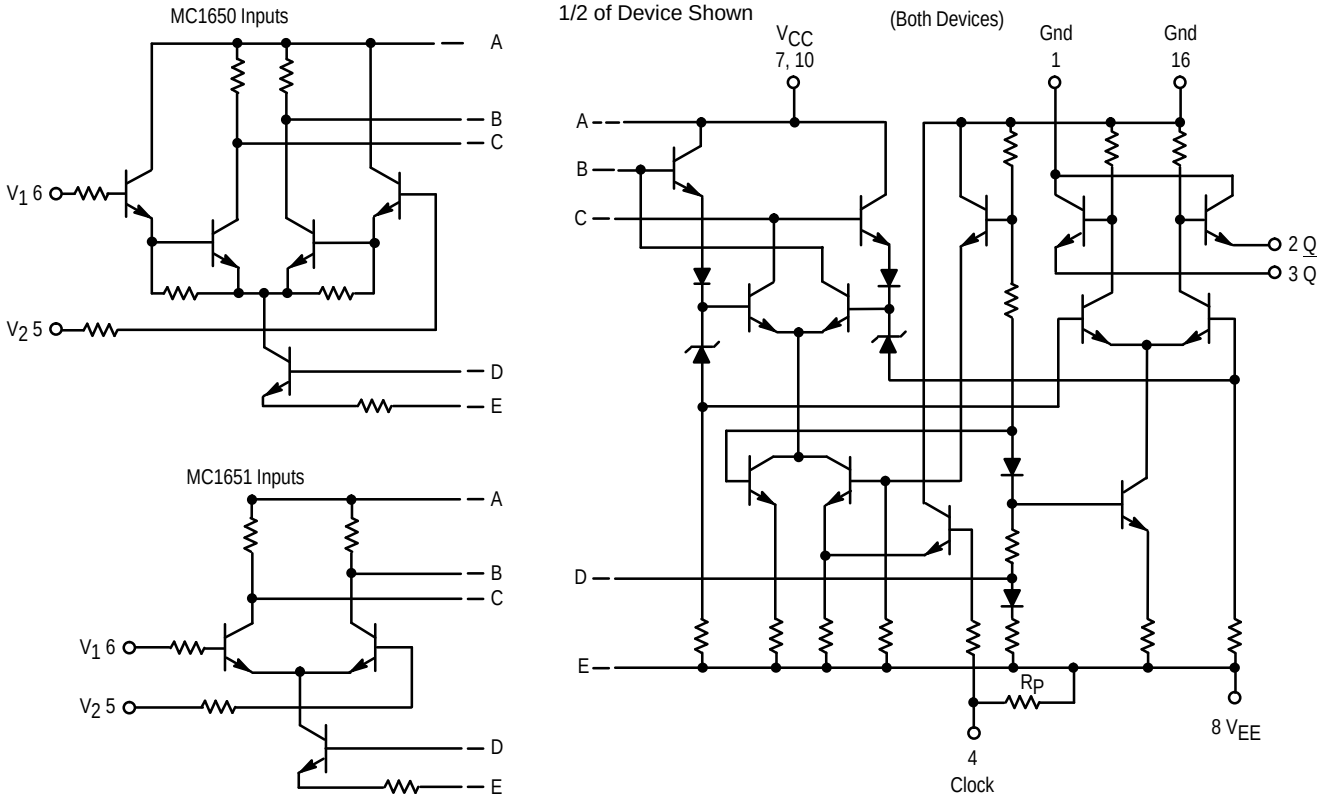
1. All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.
2. These tests are done in order indicated. See Figure 5.
3. Maximum Power Supply Voltages (beyond which device life may be impaired): $|V_{EE}| + |V_{CC}| \geq 12$ Vdc.

4.

All Temperature	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.0	+2.98	–2.5	–2.48
MC1651	+2.5	+2.48	–3.0	–2.98

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

CIRCUIT SCHEMATIC
1/2 of Device Shown



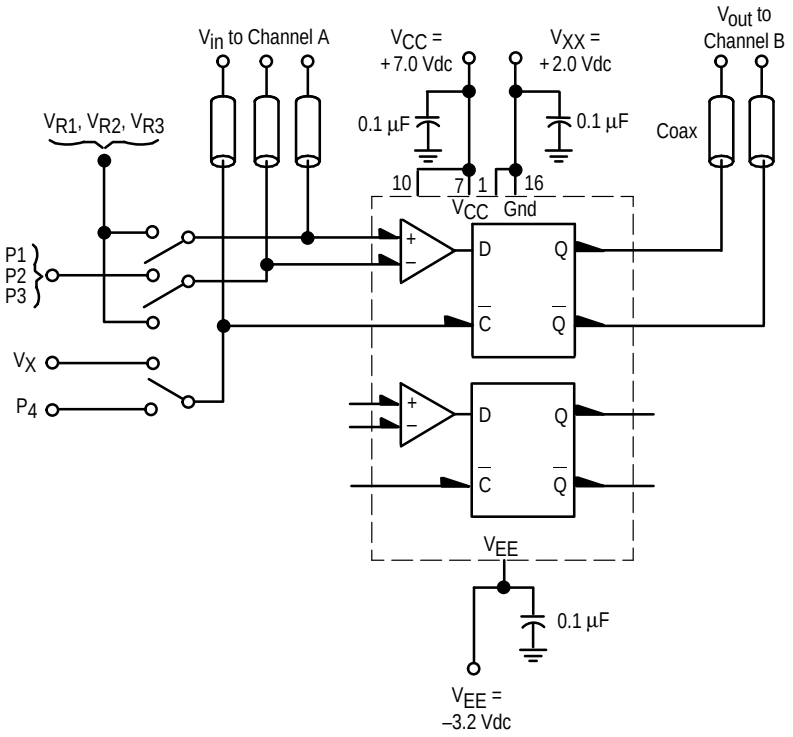
@Test Temperature	SWITCHING TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2} V_{R3}	V_X	V_{XX}	V_{CC}[1]	V_{EE}[1]
–30°C	+2.0	See Note 4	+1.04	+2.0	+7.0	–3.2
+25°C	+2.0		+1.11	+2.0	+7.0	–3.2
+85°C	+2.0		+1.19	+2.0	+7.0	–3.2

Characteristic	Symbol	–30°C Min	–30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions (See Figures 1–3)
Switching Times Propagation Delay (50% to 50%) V-Input	t_{pd}	2.0	5.0	2.0	5.0	2.0	5.7	ns	V_{R1} to V_2, V_X to Clock, P_1 to V_1, or, V_{R2} to V_2, V_X to Clock, P_2 to V_1, or, V_{R3} to V_2, V_X to Clock, P_3 to V_1.
Clock[2]		2.0	4.7	2.0	4.7	2.0	5.2		V_{R1} to V_2, P_1 to V_1 and P_4 to Clock, or, V_{R1} to V_1, P_1 to V_2 and P_4 to Clock.
Clock Enable[3]	t_{setup}	—	—	2.5	—	—	—	ns	V_{R1} to V_2, P_1 to V_1, P_4 to Clock
Clock Aperture[3]	t_{ap}	—	—	1.5	—	—	—	ns	
Rise Time (10% to 90%)	t^+	1.0	3.5	1.0	3.5	1.0	3.8	ns	V_R to V_2, V_X to Clock, P_1 to V_1.
Fall Time (10% to 90%)	t^-	1.0	3.0	1.0	3.0	1.0	3.3	ns	

NOTES:
1. Maximum Power Supply Voltages (beyond which device life may be impaired:
   $|V_{CC}| + |V_{EE}| \geq 12$ Vdc.
2. Unused clock inputs may be tied to ground.
3. See Figure 3.
4.

All Temperatures	V_{R2}	V_{R3}
MC1650	+4.9	–0.4
MC1651	+4.4	–0.9

FIGURE 1 — SWITCHING TIME TEST CIRCUIT @ 25°C

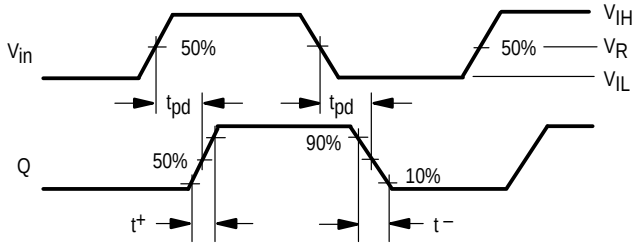


Note: All power supply and logic levels are shown shifted 2.0 volts positive.
50 ohm termination to ground located in each scope channel input.
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.

FIGURE 2 — SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

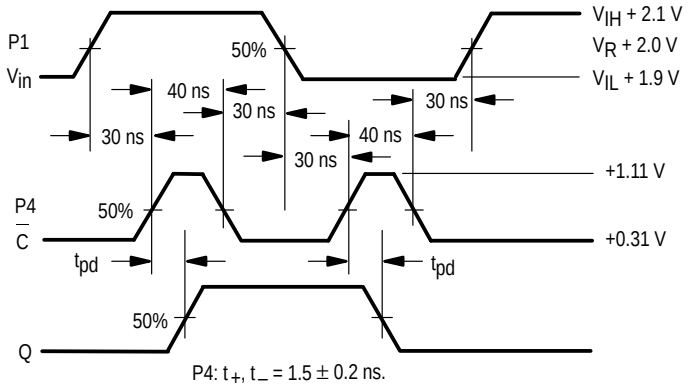
The pulse levels shown are used to check ac parameters over the full common-mode range.

V — INPUT TO OUTPUT



Test pulses: t_+, t_- = 1.5 ± 0.2 ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle

CLOCK TO OUTPUT

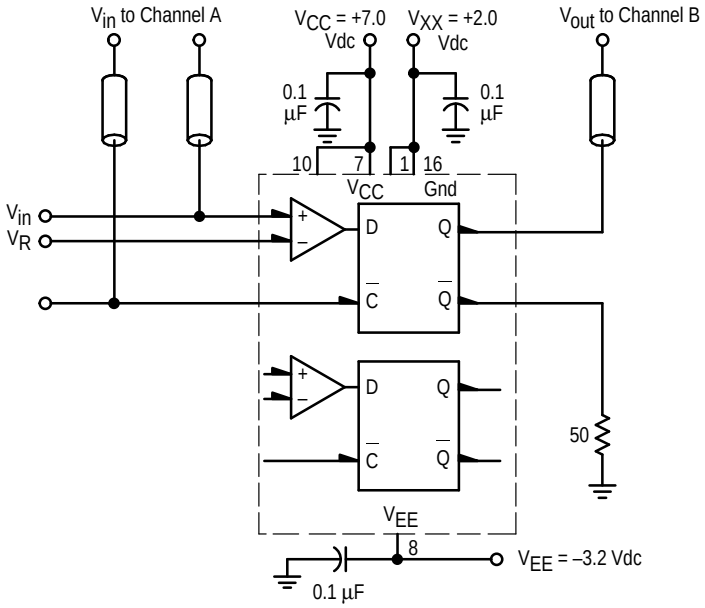


P4: t_+, t_- = 1.5 ± 0.2 ns.

TEST PULSE LEVELS

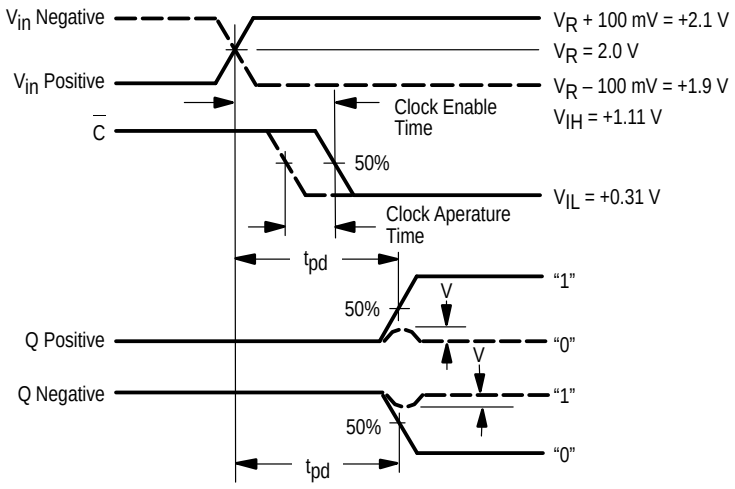
	P1		P2		P3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V_{IH}	+2.1 V	+2.1 V	+5.0 V	+4.5 V	–0.3 V	–0.8 V
V_R	+2.0 V	+2.0 V	+4.9 V	+4.4 V	–0.4 V	–0.9 V
V_{IL}	+1.9 V	+1.9 V	+4.8 V	+4.3 V	–0.5 V	–1.0 V

FIGURE 3 — CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50 ohm termination to ground located in each scope channel input.
All input and output cables to the scope are equal lengths of 50 ohms coaxial cable.

ANALOG SIGNAL POSITIVE AND NEGATIVE SLEW CASE



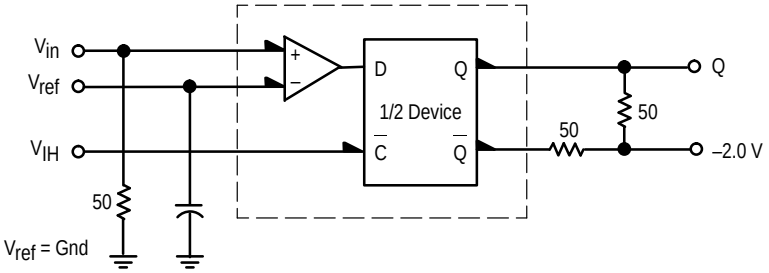
Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

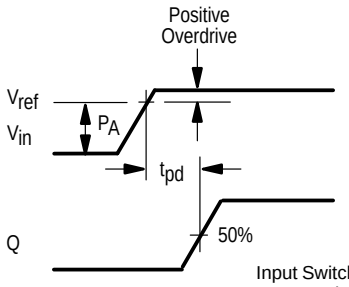
Note: All power supply and logic levels are shown shifted 2.0 volts positive.

FIGURE 4 — PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE

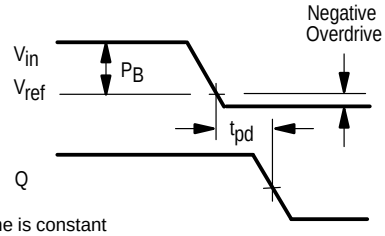
TEST CIRCUIT



POSITIVE PULSE DIAGRAM

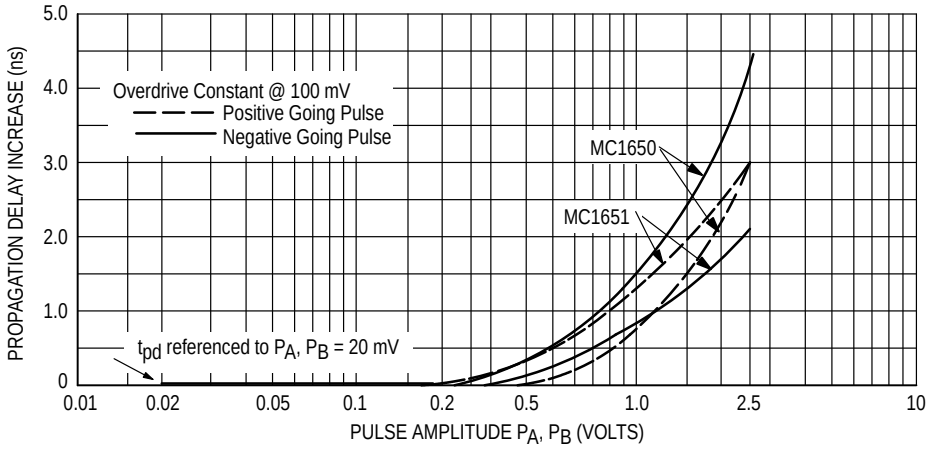


NEGATIVE PULSE DIAGRAM



Input Switching time is constant at 1.5 ns (10% to 90%).

PROPAGATION DELAY versus PULSE AMPLITUDE



PROPAGATION DELAY versus OVERDRIVE

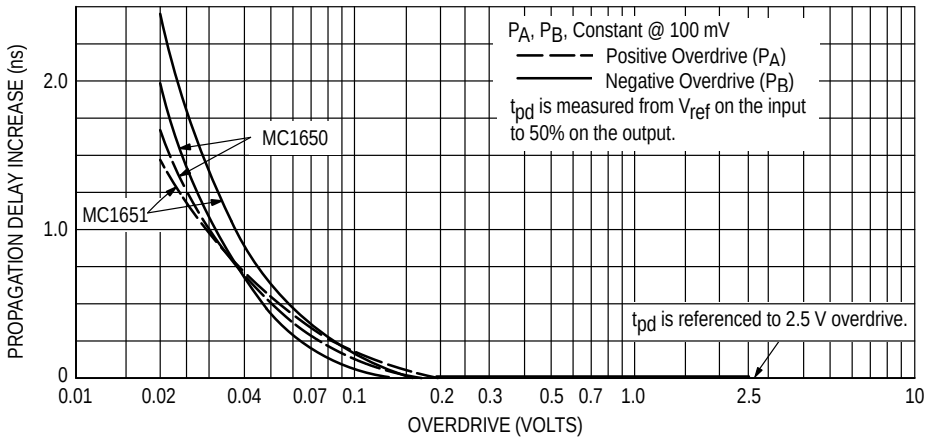


FIGURE 5 — LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

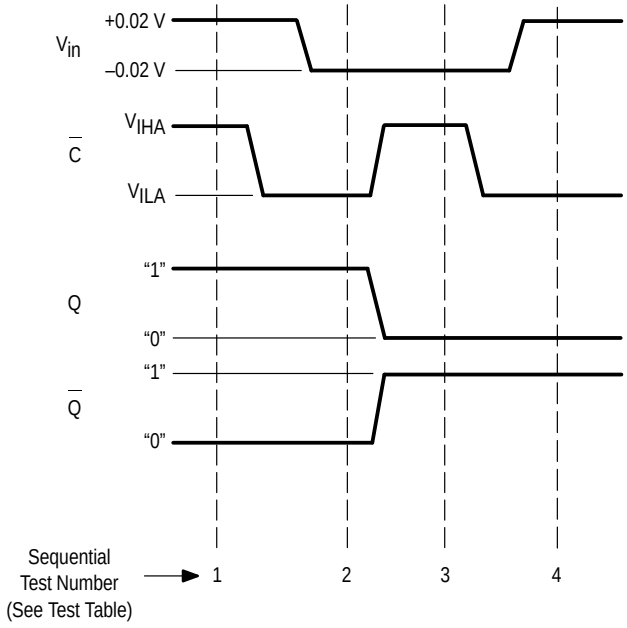
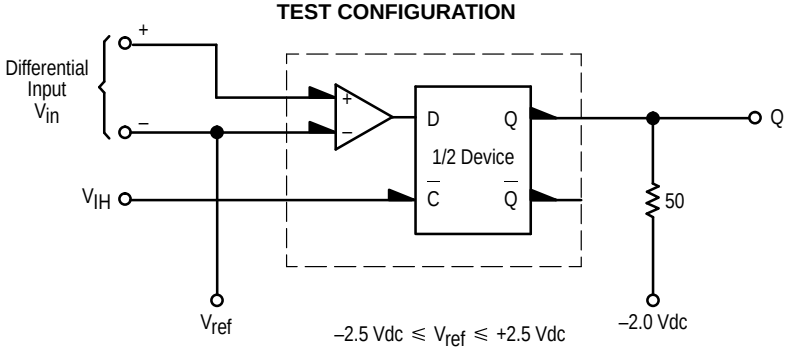


FIGURE 6 — TRANSFER CHARACTERISTICS (Q versus V_{in})

TEST CONFIGURATION



TYPICAL TRANSFER CURVES

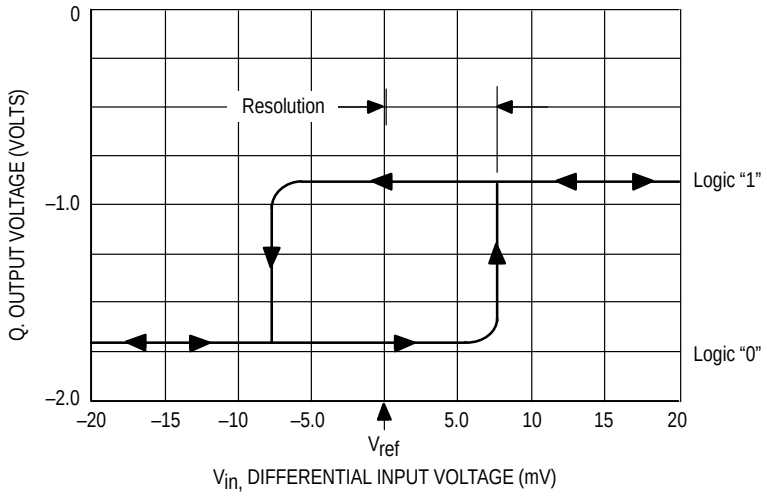
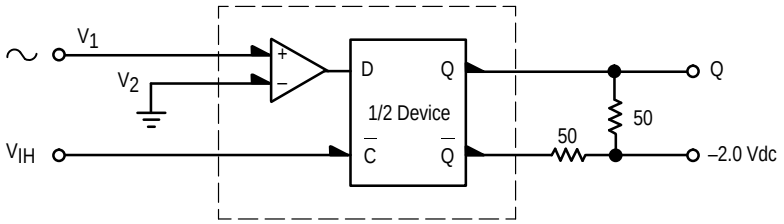
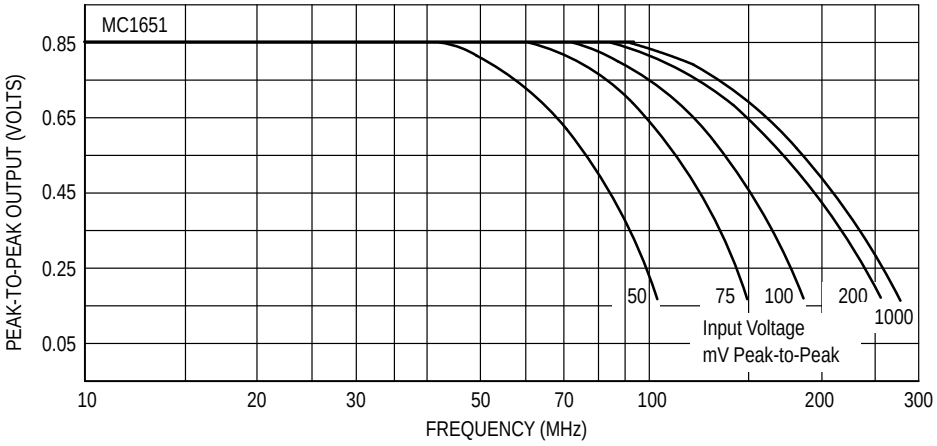


FIGURE 7 — OUTPUT VOLTAGE SWING versus FREQUENCY

(A) TEST CIRCUIT



(B) TYPICAL OUTPUT LOGIC SWING versus FREQUENCY



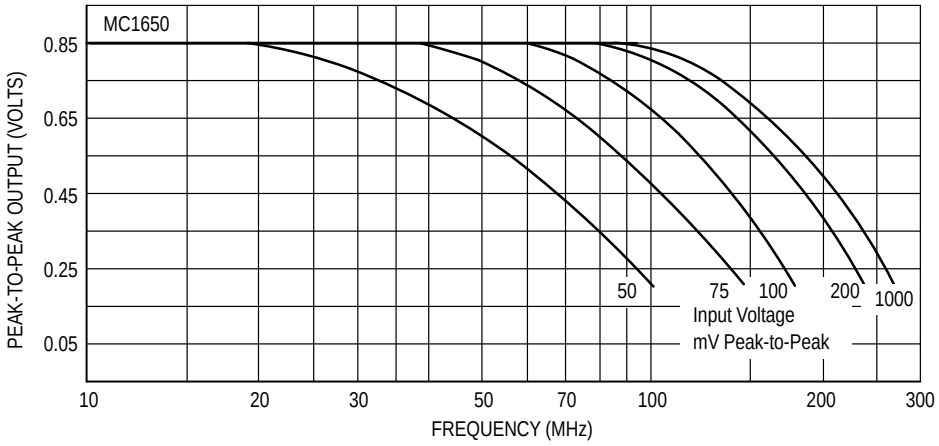
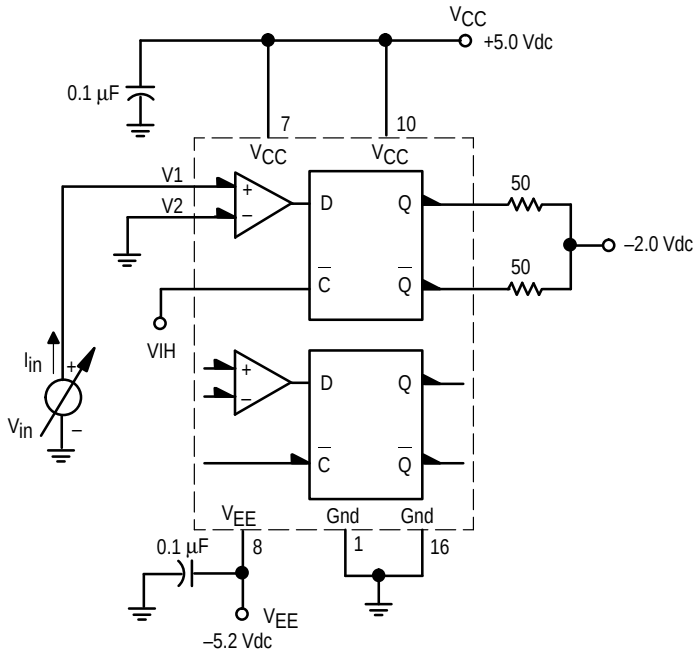
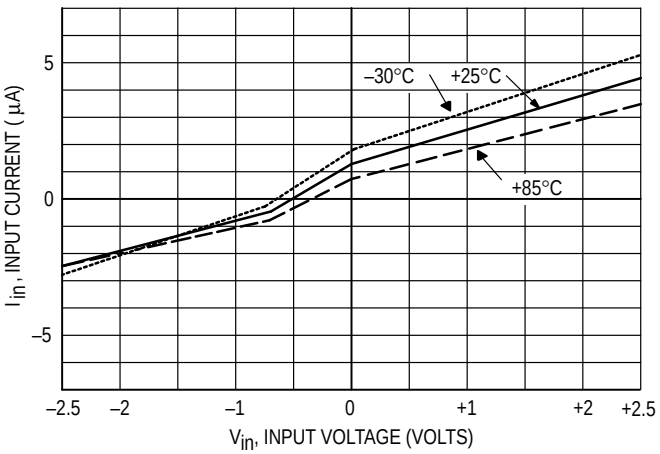


FIGURE 8 — INPUT CURRENT versus INPUT VOLTAGE

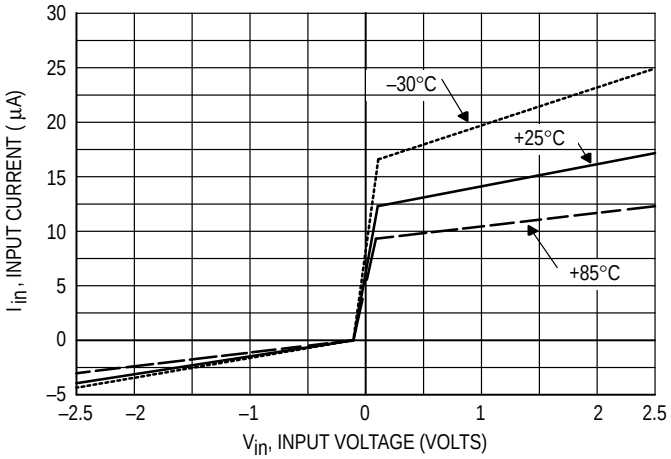
TEST CIRCUIT



Typical MC1650 (Complementary Input Grounded)

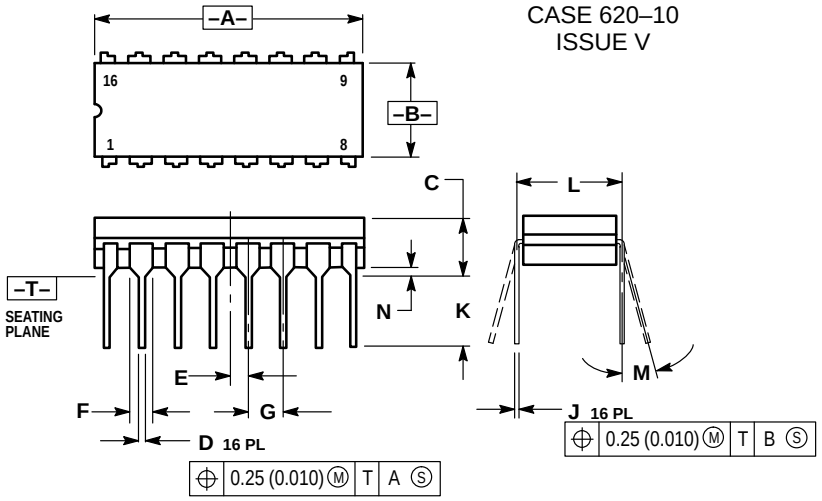


Typical MC1651 (Complementary Input Grounded)



OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

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