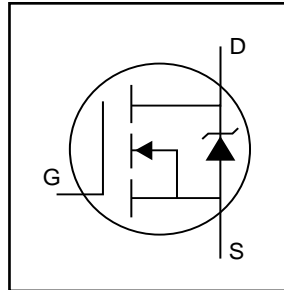


- Logic-Level Gate Drive
- Ultra Low On-Resistance
- Surface Mount (IRLR3103)
- Straight Lead (IRLU3103)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

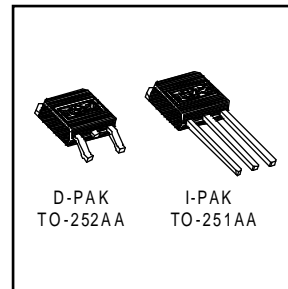


$V_{DSS} = 30V$
$R_{DS(on)} = 0.019\Omega$
$I_D = 46A \textcircled{5}$

**Description**

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	46 $\textcircled{5}$	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	29 $\textcircled{5}$	
$I_{DM}$	Pulsed Drain Current $\textcircled{1} \textcircled{7}$	220	
$P_D @ T_C = 25^\circ C$	Power Dissipation	69	W
	Linear Derating Factor	0.56	W/ $^\circ C$
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy $\textcircled{2} \textcircled{7}$	240	mJ
$I_{AR}$	Avalanche Current $\textcircled{1} \textcircled{7}$	34	A
$E_{AR}$	Repetitive Avalanche Energy $\textcircled{1}$	6.9	mJ
dv/dt	Peak Diode Recovery dv/dt $\textcircled{3} \textcircled{7}$	2.0	V/ns
$T_J$	Operating Junction and	-55 to + 150	$^\circ C$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

**Thermal Resistance**

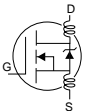
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.8	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	—	110	

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material) .

For recommended footprint and soldering techniques refer to application note #AN-994

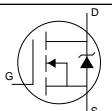
## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.037	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.019	$\Omega$	$V_{GS} = 10V, I_D = 28A$ ④
		—	—	0.024		$V_{GS} = 4.5V, I_D = 23A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	23	—	—	S	$V_{DS} = 25V, I_D = 34A$ ⑦
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
$Q_g$	Total Gate Charge	—	—	50	nC	$I_D = 34A$
$Q_{gs}$	Gate-to-Source Charge	—	—	14		$V_{DS} = 24V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	28		$V_{GS} = 4.5V$ , See Fig. 6 and 13 ④ ⑦
$t_{d(on)}$	Turn-On Delay Time	—	9.0	—	ns	$V_{DD} = 15V$
$t_r$	Rise Time	—	210	—		$I_D = 34A$
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		$R_G = 3.4\Omega, V_{GS} = 4.5V$
$t_f$	Fall Time	—	54	—		$R_D = 0.43\Omega$ , See Fig. 10 ④ ⑦
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑥
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	1600	—	pF	$V_{DS} = 0V$
$C_{oss}$	Output Capacitance	—	640	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	320	—		$f = 1.0\text{MHz}$ , See Fig. 5 ⑦



## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	46	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ① ⑦	—	—	220		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 28A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	81	120	ns	$T_J = 25^\circ\text{C}, I_F = 34A$
$Q_{rr}$	Reverse Recovery Charge	—	210	310	nC	$di/dt = 100A/\mu s$ ④ ⑦
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

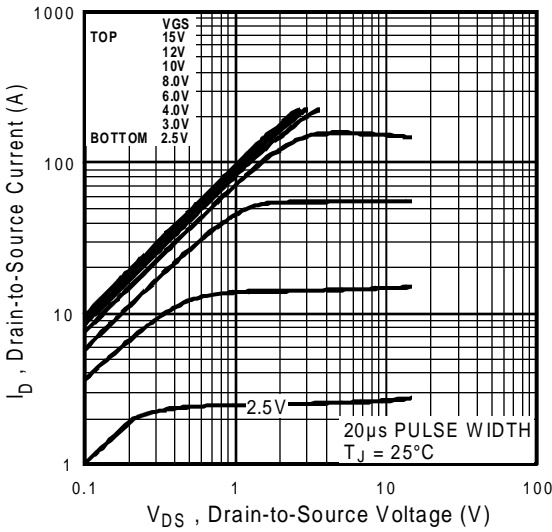


## Specification changes

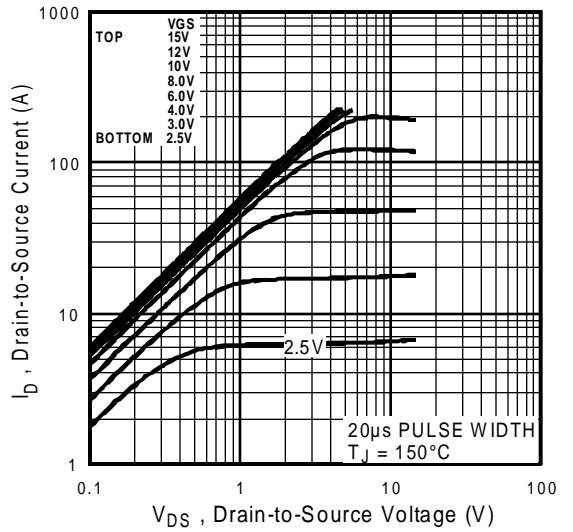
Rev. #	Parameters	Old spec.	New spec.	Comments	Revision Date
1	$V_{GS(th)}$ (Max.)	2.5V	No spec.	Removed $V_{GS(th)}$ Max. Specification	5/1/96
1	$V_{GS}$ (Max.)	$\pm 20$	$\pm 16$	Decrease $V_{GS}$ Max. Specification	5/1/96

### Notes:

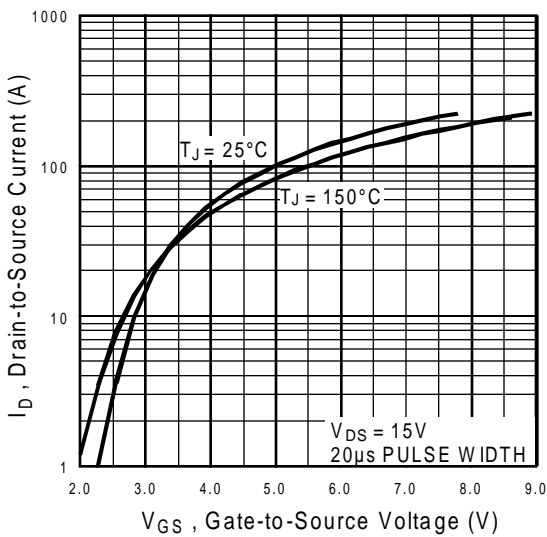
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $V_{DD} = 15V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 300\mu H$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 34A$ . (See Figure 12)
- ③  $I_{SD} \leq 34A$ ,  $di/dt \leq 140A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current = 20A.
- ⑥ This is applied for I-PAK,  $L_S$  of D-PAK is measured between lead and center of die contact
- ⑦ Uses IRL3103 data and test conditions.



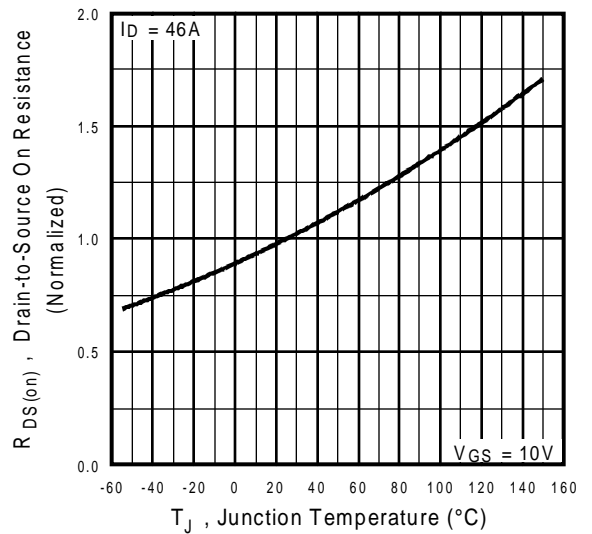
**Fig 1.** Typical Output Characteristics,  $T_J = 25^\circ\text{C}$



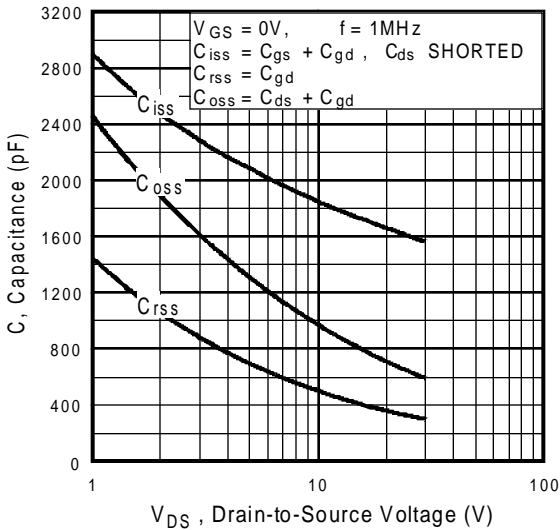
**Fig 2.** Typical Output Characteristics,  $T_J = 150^\circ\text{C}$



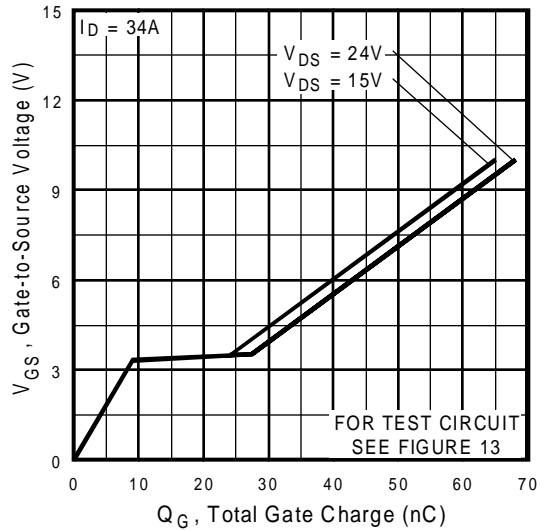
**Fig 3.** Typical Transfer Characteristics



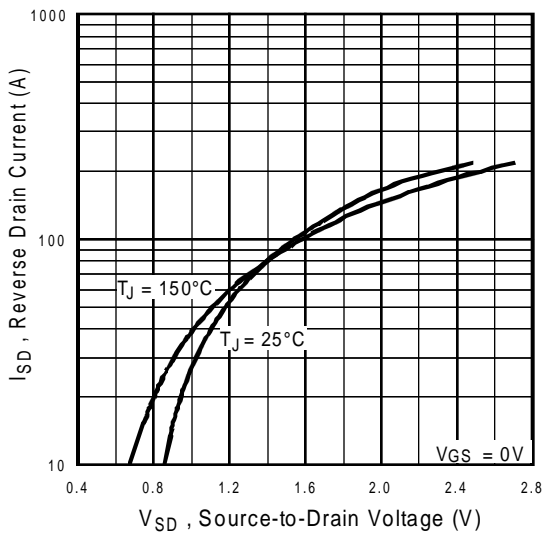
**Fig 4.** Normalized On-Resistance Vs. Temperature



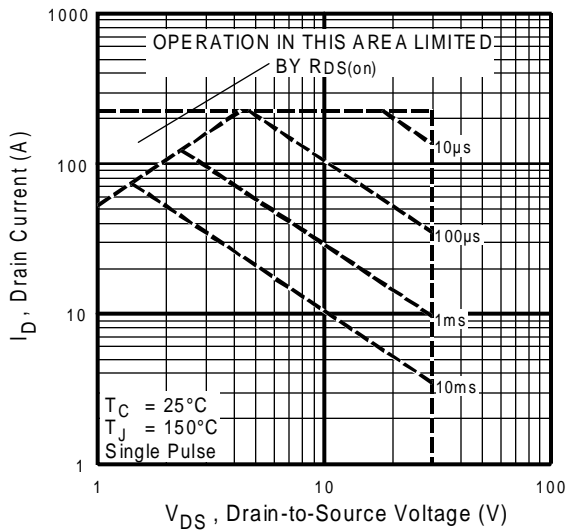
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



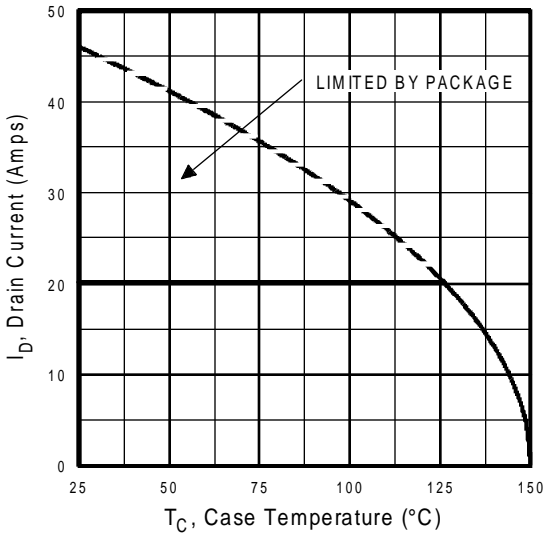
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



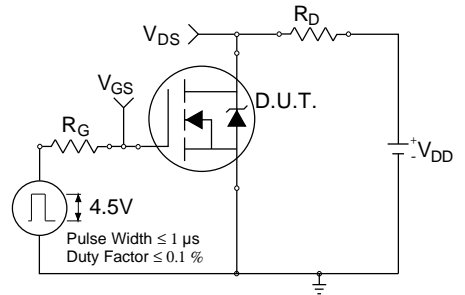
**Fig 7.** Typical Source-Drain Diode Forward Voltage



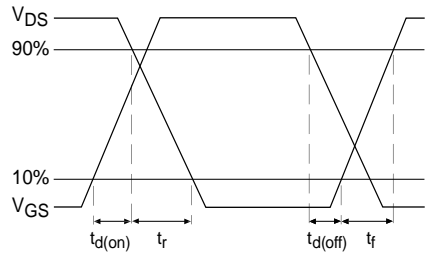
**Fig 8.** Maximum Safe Operating Area



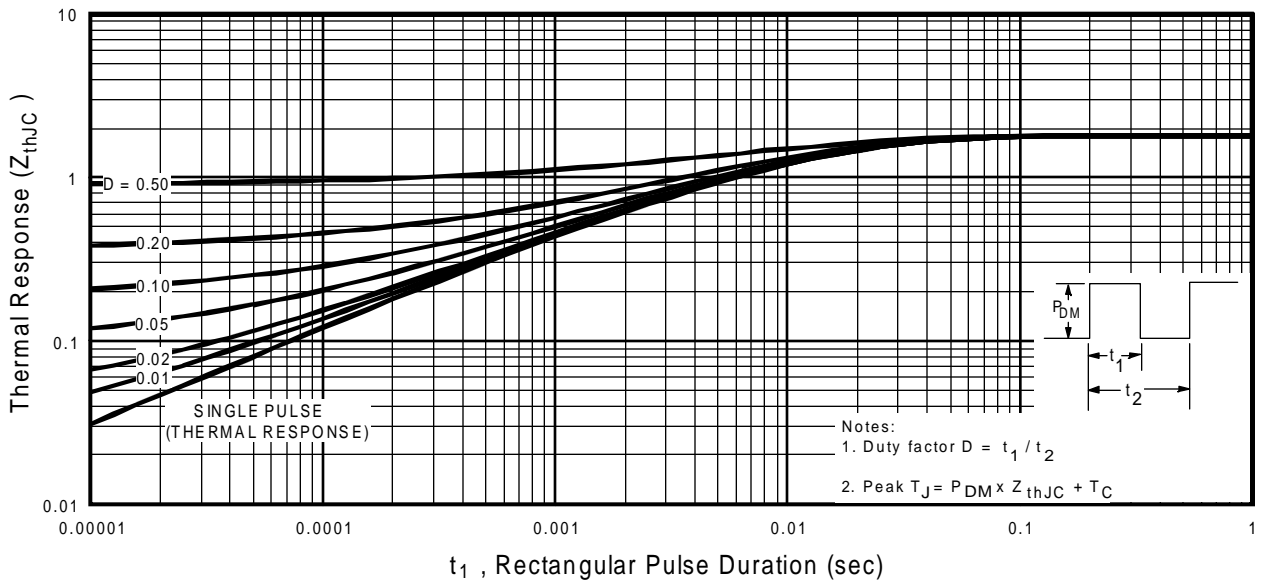
**Fig 9.** Maximum Drain Current Vs. Case Temperature



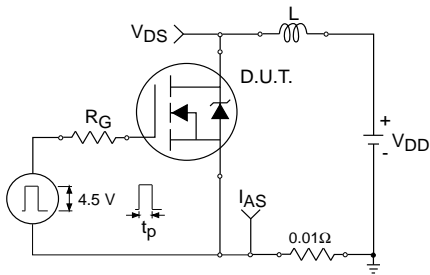
**Fig 10a.** Switching Time Test Circuit



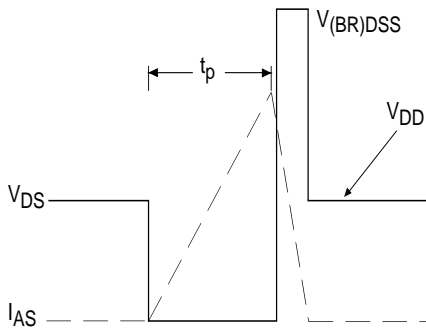
**Fig 10b.** Switching Time Waveforms



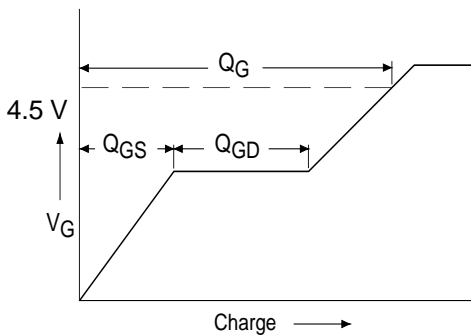
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



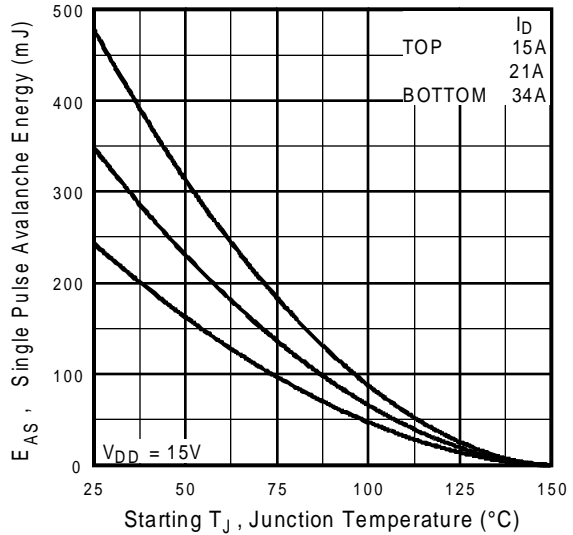
**Fig 12a.** Unclamped Inductive Test Circuit



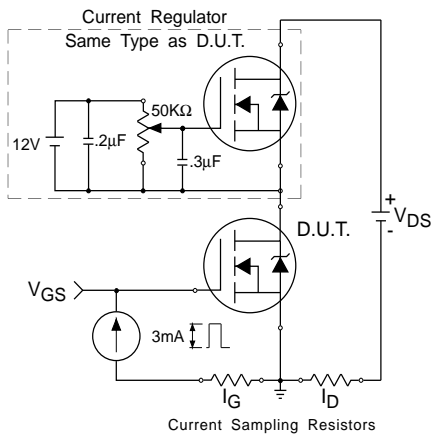
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

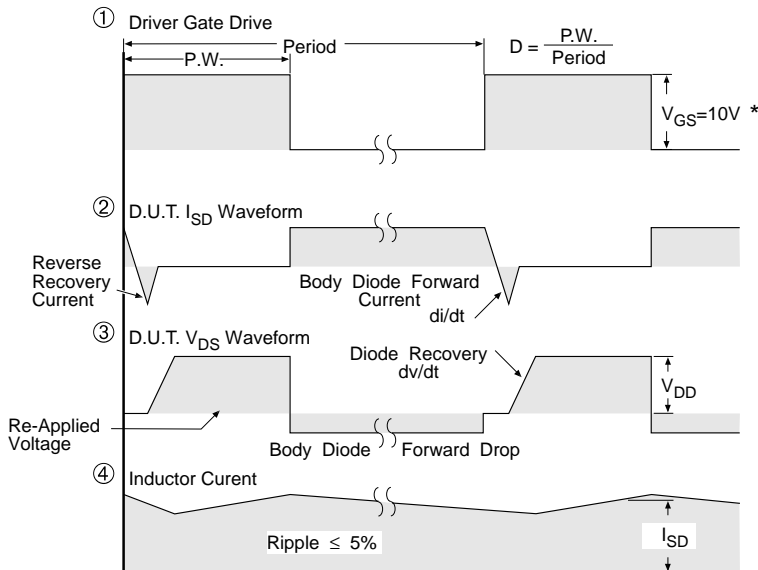
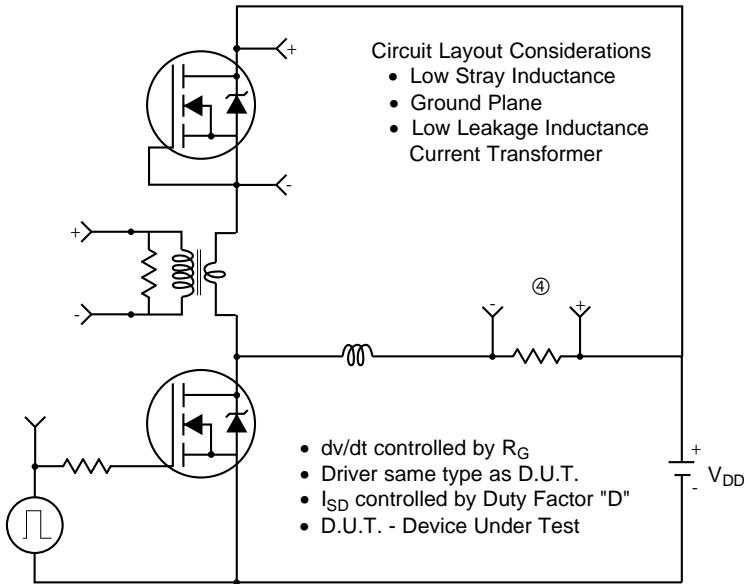


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



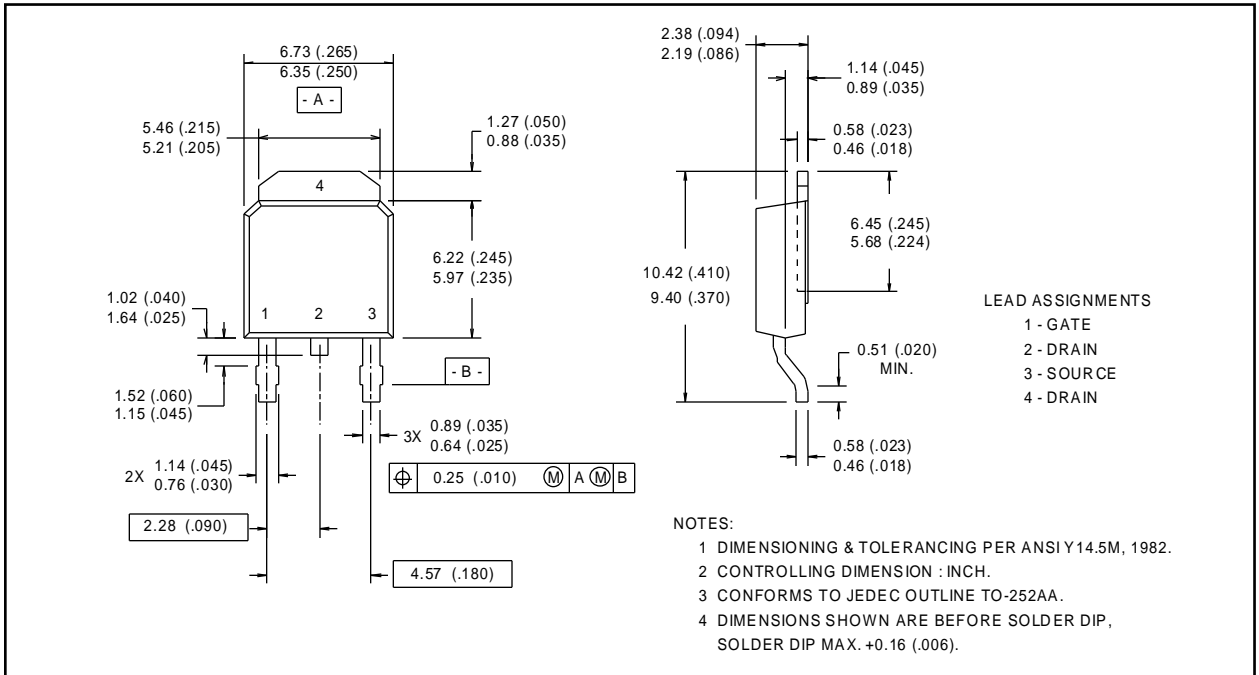
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 13.** For N-Channel HEXFETS

## Package Outline

### TO-252AA Outline

Dimensions are shown in millimeters (inches)



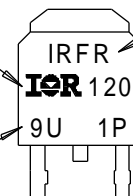
## Part Marking Information

### TO-252AA (D-PARK)

EXAMPLE : THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 9U1P

INTERNATIONAL  
RECTIFIER  
LOGO

ASSEMBLY  
LOT CODE



FIRST PORTION  
OF PART NUMBER

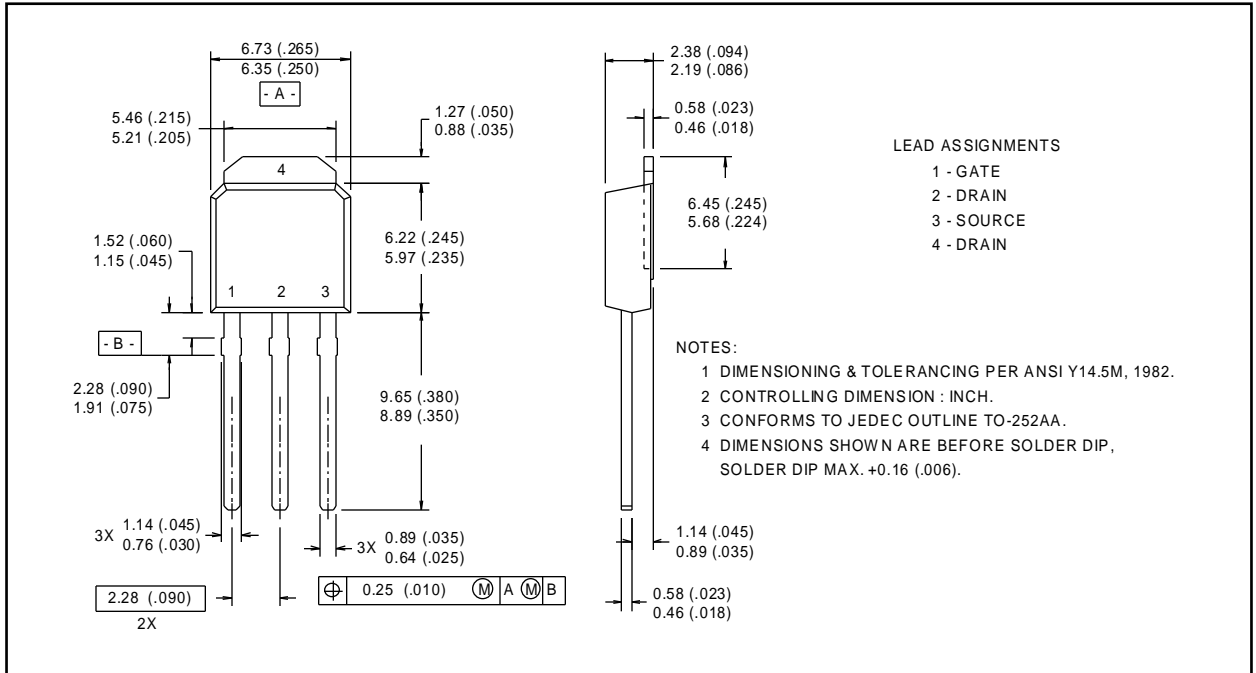
SECOND PORTION  
OF PART NUMBER



## Package Outline

### TO-251AA Outline

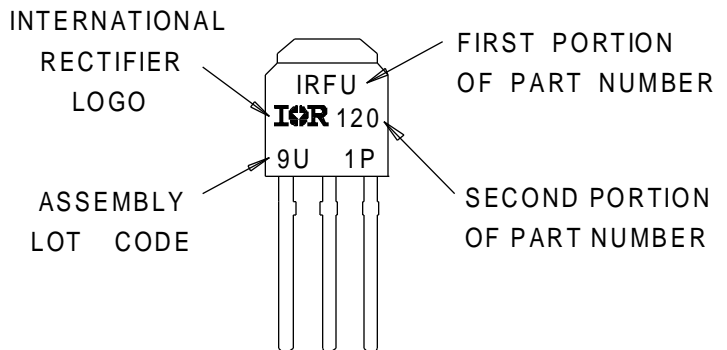
Dimensions are shown in millimeters (inches)



## Part Marking Information

### TO-251AA (I-PARK)

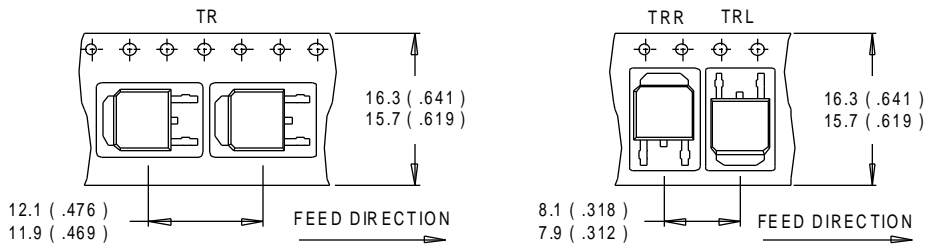
EXAMPLE : THIS IS AN IRFU120  
 WITH ASSEMBLY  
 LOT CODE 9U1P



## Tape & Reel Information

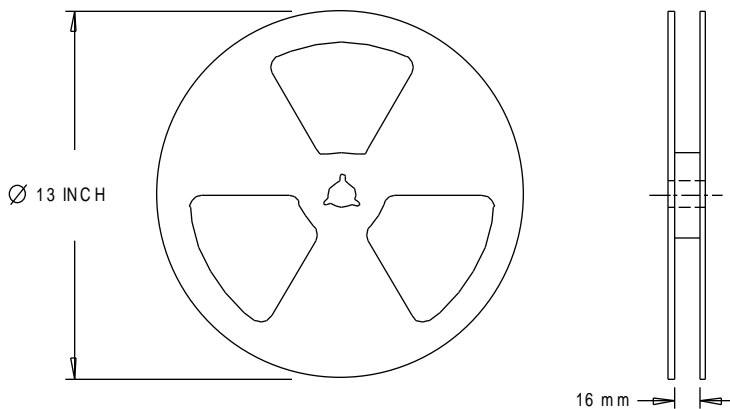
### TO-252AA

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.