

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

DESCRIPTION

This product is Dual N-channel MOS Field Effect Transistor designed for DC/DC converters.

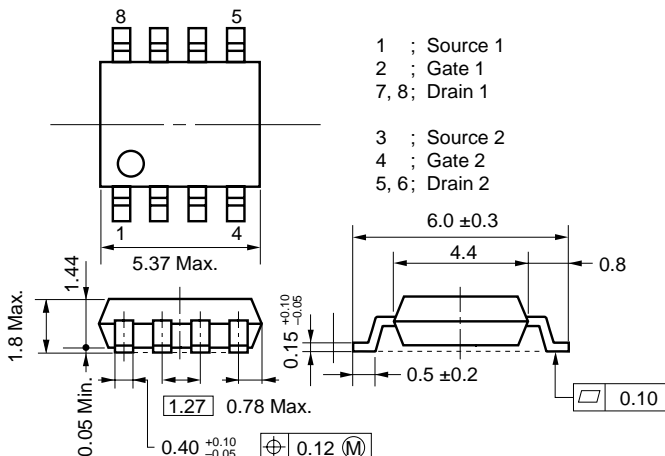
FEATURES

- Dual chip type
- Low on-resistance  
 $R_{DS(on)1} = 110 \text{ m}\Omega \text{ TYP. (} V_{GS} = 10 \text{ V, } I_D = 2.5 \text{ A)}$   
 $R_{DS(on)2} = 170 \text{ m}\Omega \text{ TYP. (} V_{GS} = 4 \text{ V, } I_D = 2.5 \text{ A)}$
- Low input capacitance  $C_{iss} = 190 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1759G	Power SOP8

PACKAGE DRAWING (Unit : mm)

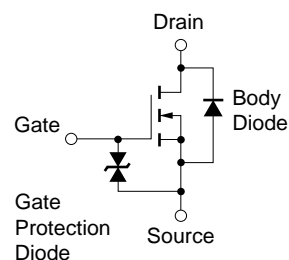


ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0$ )	$V_{DSS}$	60	V
Gate to Source Voltage ( $V_{DS} = 0$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 5.0$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 20$	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	$P_T$	1.7	W
Total Power Dissipation (2 unit) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	2.5	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	0.625	mJ

- Notes
1.  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1 \%$
  2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 1.7 \text{ mm}$
  3. Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

EQUIVALENT CIRCUIT  
(1/2 Circuit)



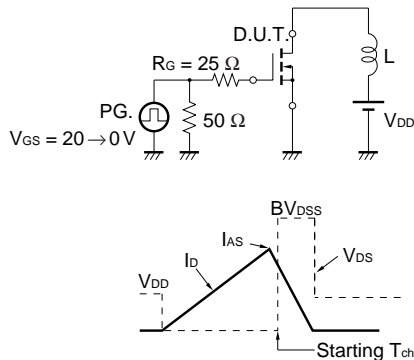
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

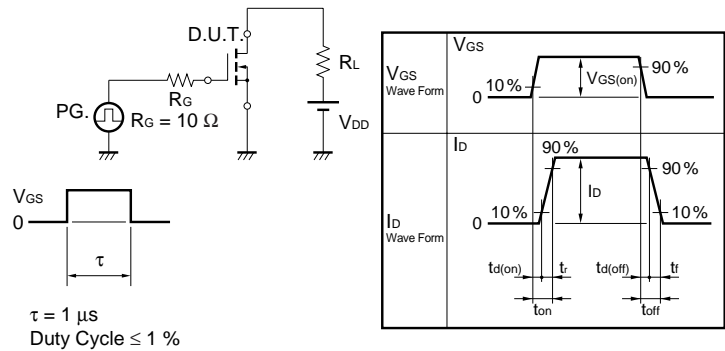
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A		110	150	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 2.5 A		170	240	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.7	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.5 A	2.0	3.9		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		190		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		100		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		36		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 2.5 A		6		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		50		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 15 V		80		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		50		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 5.0 A		8		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 24 V		1		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		2.4		nC
Body Diode forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 5.0 A, V <sub>GS</sub> = 0 V		0.9		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 5.0 A, V <sub>GS</sub> = 0 V		40		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		50		nC

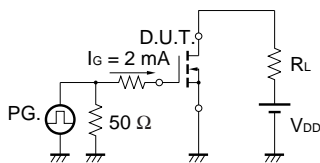
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**



**TEST CIRCUIT 3 GATE CHARGE**



[MEMO]

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