DATA SHEET

TDA9861
Universal HiFi audio processor for TV

Preliminary specification
File under Integrated Circuits, IC02

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Philips
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PHILIPS

Universal HiFi audio processor for TV TDA9861

FEATURES

- Multi-source selector switches six AF inputs (three stereo sources or six mono sources)
- Each of the input signals can be switched to each of the outputs (crossbar switch)
- Outputs for loudspeaker channel, headphone channel and peri-TV connector (SCART)
- Switchable spatial stereo and pseudo stereo effects
- Audio surround decoder can be added externally
- Two general purpose logic output ports
- I²C-bus control of all functions.

GENERAL DESCRIPTION

The TDA9861 provides control facilities for the main, the headphone and the SCART channel of a TV set. Due to extended switching possibilities, signals from 3 stereo sources can be handled.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 6)	7.2	8.0	8.8	V
I_P	supply current	–	25	–	mA
V_i	input signal levels for 0 dB gain (RMS value)	2	–	–	V
V_o	output signal levels for 0 dB gain (RMS value)	2	–	–	V
G_v	gain in main channel				
	volume control (1 dB steps, balance included)	–63	–	+15	dB
	bass control (1.5 dB steps)	–12	–	+15	dB
	treble control (3 dB steps)	–12	–	+12	dB
	gain in headphone channel				
	volume control (2 dB steps)	–54	–	+16	dB
	gain for muting in all channels	–80	–	–	dB
THD	total harmonic distortion	–	0.1	–	%
S/N	signal-to-noise ratio	–	85	–	dB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9861	32	SDIL	plastic	SOT232(1)

Note

1. SOT232-1; 1996 December 10.

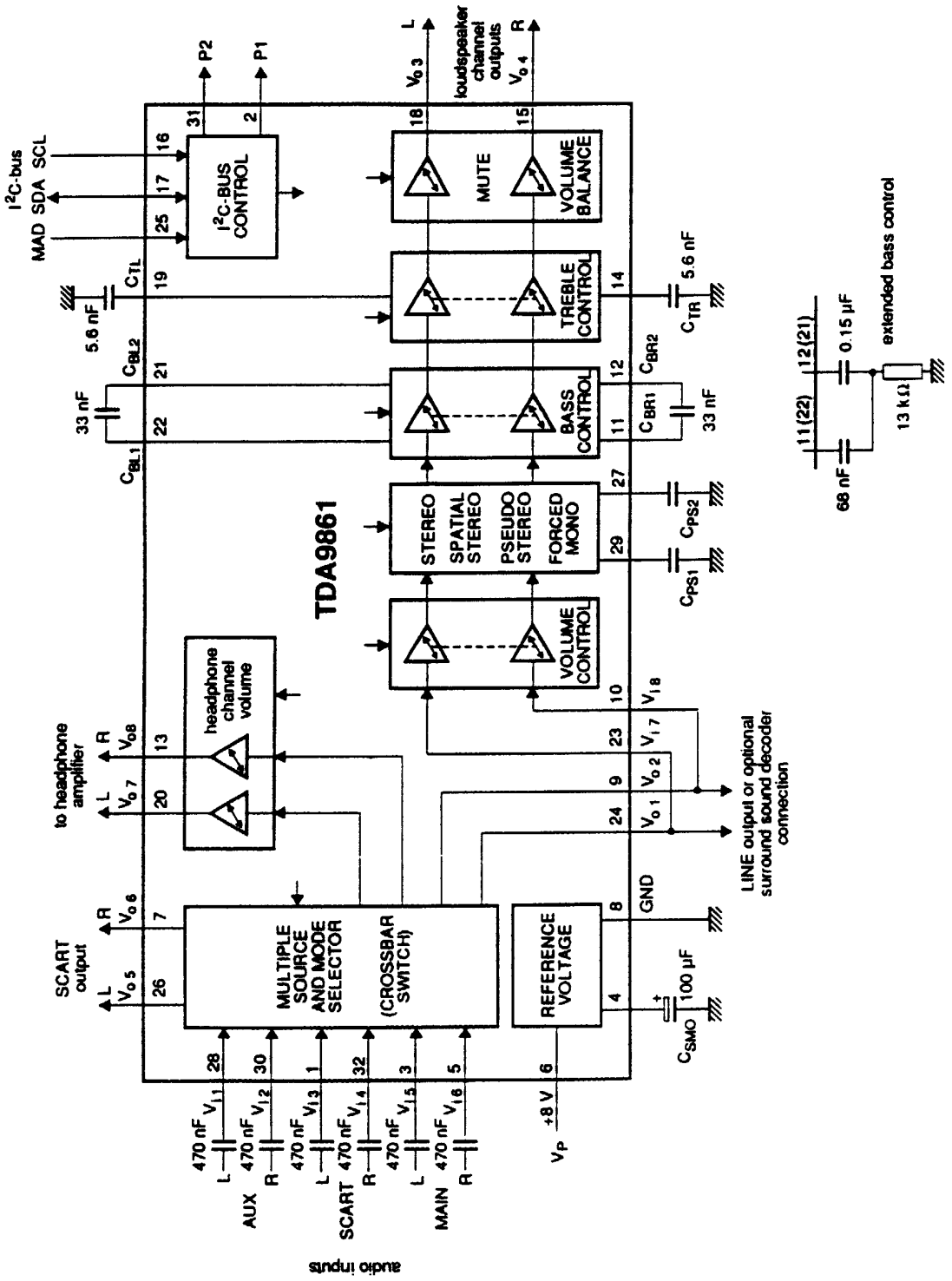


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\,3}$	1	SCART input signal LEFT
P1	2	port 1 output
$V_{i\,5}$	3	MAIN input signal LEFT
C_{SMO}	4	smoothing capacitor of reference voltage
$V_{i\,6}$	5	MAIN input signal RIGHT
V_P	6	positive supply voltage
$V_{o\,6}$	7	SCART output signal RIGHT
GND	8	ground
$V_{o\,2}$	9	MAIN output signal RIGHT
$V_{i\,8}$	10	input signal RIGHT to loudspeaker channel
C_{BR1}	11	bass capacitor RIGHT 1
C_{BR2}	12	bass capacitor RIGHT 2
$V_{o\,8}$	13	headphone output signal RIGHT
C_{TR}	14	treble capacitor RIGHT
$V_{o\,4}$	15	loudspeaker channel output signal RIGHT
SCL	16	I^2C-bus clock line
SDA	17	I^2C-bus data line
$V_{o\,3}$	18	loudspeaker channel output signal LEFT
C_{TL}	19	treble capacitor LEFT
$V_{o\,7}$	20	headphone output signal LEFT
C_{BL2}	21	bass capacitor LEFT 2
C_{BL1}	22	bass capacitor LEFT 1
$V_{i\,7}$	23	input signal LEFT to loudspeaker channel
$V_{o\,1}$	24	MAIN output signal LEFT
MAD	25	module address select input
$V_{o\,5}$	26	SCART output signal LEFT
C_{PS2}	27	pseudo stereo capacitor 2
$V_{i\,1}$	28	AUX input signal LEFT
C_{PS1}	29	pseudo stereo capacitor 1
$V_{i\,2}$	30	AUX input signal RIGHT
P2	31	port 2 output
$V_{i\,4}$	32	SCART input signal RIGHT

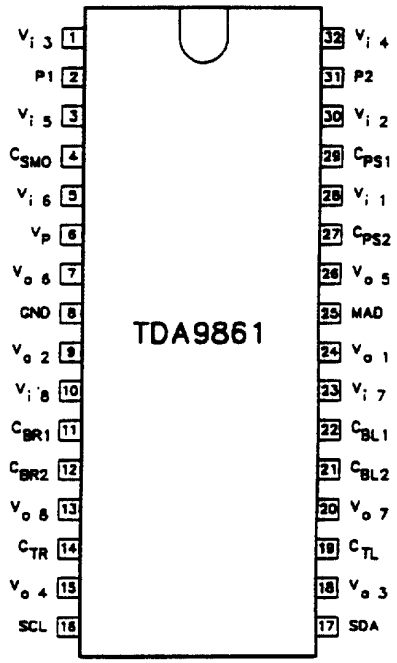


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9861 consists of the following functions:

- source select switching block
- loudspeaker channel with effect controls
- headphone channel
- two port outputs for general purpose
- I^2C–bus control

Source select switching block

The TDA9861 selects and switches the input signals from three stereo or six mono sources as there are MAIN, AUX and SCART (Fig.1) to one of the outputs SCART, loudspeaker and headphone (crossbar-switching Table 3). Due to the fact, that the main channel (LINE outputs) is looped outside the circuit (from pins 9 and 24 to pins 10 and 23), signals can be used as LINE output or to insert a 'surround sound decoder'.

Loudspeaker channel

Volume control is divided into the parts volume 1 and volume 2 / balance. The first part (55 dB) controls left and right channels simultaneously; the second part (23 dB) controls volume and balance of left and right channels independently. Treble control provides a control range from –12 to +12 dB and bass control from –12 to +15 dB. Extended bass control can be provided by an external T-network (Fig.1) from –15 to +19 dB (2 dB steps).

Effect controls

'Linear stereo', 'stereo with spatial effect (30% or 52% anti-phase crosstalk)' and 'forced mono with or without pseudo-stereo effect' are controlled by three bits. A muting of 85 dB is provided.

Headphone channel

The headphone channel is only equipped with volume / balance control. A muting of 85 dB is provided.

I^2C-bus control

All settings of control are stored in subaddress registers. Data transmission is simplified by auto-incrementing the subaddresses. The on-chip power on reset sets the mute bit to active, so all 3 stereo outputs are muted.
The muting can be switched off by writing a '0' (non-muted) into the mute control bits.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 6)	0	10	V
V_n	voltage on all pins, ground excluded	0	V_P	V
I_O	output current			
	at pins 15, 18, 13, 20, 7 and 26	–	2.5	mA
	at pins 2 and 31	–	1.5	mA
P_{tot}	total power dissipation	–	850	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	–	±300	V
	electrostatic handling for all pins (note 2)	–	±2000	V

Notes to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	60 K/W

CHARACTERISTICS

V_P = 8 V; T_{amb} = +25 °C; treble and bass in linear positions; balance in mid position; spatial function, pseudo-stereo function and forced-mono function in off position and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 6)		7.2	8.0	8.8	V
I_P	supply current (pin 6)		–	25	–	mA
V_{ref}	internal reference voltage		–	$V_P/2$	–	V
V_4	voltage (pin 4)		–	$V_P - 0.1$	–	V
DC voltage on pins						
V_i	DC input voltage (pins 1, 3, 5, 10, 23, 28, 30 and 32)		–	$V_P/2$	–	V
V_O	DC output voltage (pins 7, 9, 13, 15, 18, 20, 24 and 26)		–	$V_P/2$	–	V
V_C	DC voltage on capacitors (pins 11, 12, 14, 19, 21, 22, 27 and 29)		–	$V_P/2$	–	V
Audio select switch. Line, SCART and headphone outputs (controlled via I^2C-bus, Table 3)						
V_i	maximum AF input signal on pins 1, 3, 5, 28, 30, 32 (RMS value)	THD ≤ 0.5% on output pins	2	–	–	V
R_i	input resistance (pins 1, 3, 5, 28, 30, 32)		20	30	40	kΩ
f	frequency response for all AF outputs	–0.5 dB	20	–	20000	Hz
V_o	maximum AF output signal on pins 7, 9, 24, 26 (RMS value)	THD ≤ 0.5%	2	–	–	V
R_L	allowed external load resistance					
	on output (pins 9 and 24)		10	–	–	kΩ
	on output (pins 7 and 26)		5	–	–	kΩ
G_v	gain for all signal arms		–	0	–	dB
α_{cr}	switch crosstalk on outputs between AF inputs at f = 10 kHz	unused inputs connected to ground	–	90	–	dB
LOUDSPEAKER CHANNEL (controlled via I^2C-bus, Table 3)						
Volume control 1 (LEFT and RIGHT simultaneously)		f = 1 kHz, 55 steps				
V_i	maximum input signal (RMS value; pins 10 and 23)	G_v = 0; THD ≤ 0.5% on output pins 15 and 18	2	–	–	V
R_i	input resistance (pins 10 and 23)		7.5	10	–	kΩ
G_v	nominal volume control		–40	–	+15	dB
	minimum volume control		–38	–	+14	dB
ΔG_v	step width	G_v = –32 to +15 dB	0.5	1.0	1.5	dB
		G_v = –40 to –33 dB	0.25	1.0	1.75	dB
	gain set error	G_v = –32 to +15 dB	–	–	1	dB
		G_v = –40 to –33 dB	–	–	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume 2 / balance control		f = 1 kHz, 24 steps				
G_v	nominal volume control		–24	–	0	dB
	minimum volume control		–23	–	–1	dB
	gain in mute position		–80	–85	–	dB
ΔG_v	step width		0.5	1.0	1.5	dB
	gain tracking error		–	–	2	dB
Bass control						
G_v	controllable bass	C_B = 33 nF				
	maximum boost	f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
ΔG_v	step width		1	1.5	2	dB
G_v	controllable enhanced bass	Fig.1				
	maximum boost	f = 60 Hz	18	19	20	dB
	maximum attenuation	f = 60 Hz	14	15	16	dB
ΔG_v	step width		1	2	3	dB
Treble control						
G_v	controllable treble					
	maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
ΔG_v	step width (resolution)		2.5	3	3.5	dB
Effect controls						
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo		–	Fig.3	–	
Loudspeaker channel outputs (pins 15 and 18)						
V_o	maximum output signal (RMS value; pins 15 and 18)	THD ≤ 0.5%; R_L > 10 kΩ; C_L < 1.5 nF	2	–	–	V
$\Delta V_{15, 18}$	maximum DC offset voltage	between adjoining step and any step to mute				
	for volume control	G_v = 0 to +15 dB/mute	–	2	15	mV
		G_v = –64 to 0 dB/mute	–	0.5	10	mV
	for bass control	G_v = 0 to +15 dB/mute	–	2	15	mV
		G_v = –12 to 0 dB/mute	–	0.5	10	mV
	for treble control	G_v = –12 to +12 dB/mute	–	0.5	10	mV
R_o	output resistance (pins 15 and 18)		–	–	100	Ω
R_L	allowed output load resistor		10	–	–	kΩ
C_L	allowed output load capacitor		–	–	1.5	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{N(W)}$	weighted noise voltage at output (quasi-peak level)	CCIR468-3				
	for +15 dB gain		–	102	–	μV
	for 0 dB gain		–	32	–	μV
	for –40 dB gain		–	27	–	μV
	for mute position	G_v = –80 dB	–	20	–	μV
B	AF bandwidth	–1 dB	–	20 to 20000	–	Hz
THD	total harmonic distortion	f = 20 to 12500 Hz				
	for V_i = 0.2 V (RMS value)	G_v = –30 to + 15 dB	–	0.1	0.3	%
	for V_i = 1 V (RMS value)	G_v = –30 to 0 dB	–	0.1	0.3	%
	for V_i = 2 V (RMS value)	G_v = –30 to –6 dB	–	0.1	0.3	%
α_{sp}	stereo channel separation	f = 10 kHz; G_v = 0 dB; opposite input grounded by 1 kΩ resistor	–	75	–	dB
α_{bus}	crosstalk of I^2C-bus	G_v = 0 dB; note 1	–	100	–	dB
RR_{100}	ripple rejection with 100 Hz ripple on V_P	G_v = 0 dB; V_R < 200 mV RMS	–	55	–	dB
HEADPHONE CHANNEL (controlled via I^2C-bus, Table 3)						
Volume control headphone channel		f = 1 kHz, 36 steps				
G_v	nominal volume control		–54	–	+16	dB
	minimum volume control		–51	–	–1	dB
	gain in mute position		–80	–85	–	dB
ΔG_v	step width (resolution)	G_v = –36 to +16 dB	1.5	2	2.5	dB
		G_v = –54 to –36 dB	1	2	3	dB
	gain set error	G_v = –36 to +16 dB	–	–	1	dB
		G_v = –54 to +36 dB	–	–	3	dB
$\Delta V_{13, 20}$	DC offset voltage	for adjoining step and any step to mute				
		G_v = 0 to +16 dB/mute	–	2	15	mV
		G_v = –54 to 0 dB/mute	–	0.5	10	mV
Headphone channel output (pins 13 and 20)						
V_o	maximum output signal (RMS value)	THD ≤ 0.5%; R_L > 10 kΩ; C_L < 1.5 nF	2	–	–	V
R_o	output resistance		–	–	100	Ω
R_L	allowed output load resistor		10	–	–	kΩ
C_L	allowed output load capacitor		–	–	1.5	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{N(W)}$	weighted noise voltage at output (quasi-peak level) CCIR468-3					
	for +16 dB gain		–	115	–	μV
	for 0 dB gain		–	20	–	μV
	for −16 dB gain		–	15	–	μV
	for mute position	G_v = −80 dB	–	12	–	μV
B	AF bandwidth	−1 dB	–	20 to 20000	–	Hz
THD	total harmonic distortion	f = 20 to 12500 Hz				
	for V_i = 1 V (RMS value)	G_v = −40 to 0 dB	–	0.08	0.25	%
α_{sp}	stereo channel separation	f = 10 kHz; G_v = 0 dB; opposite input grounded by 1 kΩ resistor	–	75	–	dB
α_{bus}	crosstalk of I²C-bus	G_v = 0 dB; note 1	–	100	–	dB
RR_{100}	ripple rejection with 100 Hz ripple on V_P	G_v = 0 dB; V_R < 200 mV RMS	–	55	–	dB
SCART output (pins 7 and 26)						
V_o	maximum output signal (RMS value)	THD ≤ 0.5%; R_L > 5 kΩ	2	–	–	V
R_L	admissible output load resistor		5	–	–	kΩ
Power on reset						
V_{PONR}	increasing supply voltage					
	start of reset		–	–	2.5	V
	end of reset		5.2	6.0	6.8	V
V_{PONR}	decreasing supply voltage start of reset		4.4	5.2	6.0	V
I²C-bus, SCL and SDA (pins 16 and 17, observe I²C-bus specification)						
$V_{16, 17}$	input voltage HIGH-level		3	–	V_P	V
	input voltage LOW-level		0	–	1.5	V
$I_{16, 17}$	input current		–	–	±10	μA
V_{ACK}	output voltage at acknowledge (pin 17)	I_{17} = −3 mA	–	–	0.4	V
Module address (pin 25)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level output voltage		3	–	V_P	V
Port outputs P1 and P2 (open-collector outputs pins 2 and 31)						
V_{OL}	LOW level output voltage	$I_{2, 31}$ = 1 mA (sink)	–	–	0.3	V
$I_{2, 31}$	port output current	sink current	–	–	1	mA

Note to the characteristics

1. $\alpha_{bus} = 20 \log V_{bus} / V_o$ (V_{bus} = spurious bus signal voltage on AF output pin).

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S	= start condition
SLAVE ADDRESS	= 1000 0000 (V_{25} = LOW) or 1000 0010 (V_{25} = HIGH)
A	= acknowledge, generated by the slave or by the master
SUBADDRESS	= subaddress byte, see Table 1
DATA	= data byte, see Table 1
P	= stop condition

This circuit only operates as a slave transmitter.
If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission.

FUNCTION	SUBADDRESS	HEX	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
loudspeaker channel										
volume control both	0000 0000	00	0	0	V05	V04	V03	V02	V01	V00
volume/balance left	0000 0001	01	0	0	0	VL4	VL3	VL2	VL1	VL0
volume/balance right	0000 0010	02	0	0	0	VR4	VR3	VR2	VR1	VR0
bass control byte	0000 0011	03	0	0	0	BA4	BA3	BA2	BA1	BA0
treble control byte	0000 0100	04	0	0	0	0	TR3	TR2	TR1	TR0
headphone channel										
volume control left	0000 0101	05	0	0	VHL5	VHL4	VHL3	VHL2	VHL1	VHL0
volume control right	0000 0110	06	0	0	VHR5	VHR4	VHR3	VHR2	VHR1	VHR0
switching control byte										
headphone output	0000 0111	07	0	MU0	0	0	I03	I02	I01	I00
SCART output	0000 1000	08	0	MU1	P1	P2	I13	I12	I11	I10
loudspeaker output	0000 1001	09	EF2	MU2	EF1	ST	I23	I22	I21	I20

Table 2 Bits of data bytes.

FUNCTION OF THE BITS IN TABLE 1	DESCRIPTION
V00 to V05	volume control common for loudspeaker channel
VL0 to VL4	volume control LEFT for loudspeaker channel
VR0 to VR4	volume control RIGHT for loudspeaker channel
BA0 to BA4	bass control for LEFT and RIGHT loudspeaker channel
TR0 to TR3	treble control for LEFT and RIGHT loudspeaker channel
VHL0 to VHL5	volume control LEFT for headphone channel
VHR0 to VHR5	volume control RIGHT for headphone channel
I00 to I03	input selection for headphone channel
I10 to I13	input selection for SCART channel
I20 to I23	input selection for loudspeaker channel
MU0, MU1 and MU2	mute control bits: 0 = non-muted; 1 = muted
EF1, EF2 and ST	special mode control bits
P1 and P2	control bits for ports P1 (pin 2) and P2 (pin 31); output levels: 0 = LOW; 1 = HIGH

Table 3 Output and input selection by subaddress bytes 07, 08 and 09.

OUTPUT AND INPUT CONTROL BYTES, MUTE INCLUDED (EFFECTS TABLE 4)												
SELECT OUTPUT PINS		**INPUT GROUP**	**INPUT SIGNAL**	**ADDR**	**DATA BYTE TO SUBADDRESS**							
Loudspeaker channels												
output pin 18	output pin 15			09	EF2	MU2	EF1	ST	I23	I22	I21	I20
SCART channels												
output pin 26	output pin 7			08	0	MU1	P1	P2	I13	I12	I11	I10
headphone channels												
output pin 20	output pin 13			07	0	MU0	0	0	I03	I02	I01	I00
SELECT INPUT SIGNAL PINS				**HEX**	**BITS OF DATA BYTE**							
28	28	AUX LEFT	V_{i1}	XB	X	0	X	X	1	0	1	1
30	30	AUX RIGHT	V_{i2}	X9	X	0	X	X	1	0	0	1
28	30	AUX STEREO	V_{i1} and V_{i2}	X7	X	0	X	X	0	1	1	1
1	1	SCART LEFT	V_{i3}	XA	X	0	X	X	1	0	1	0
32	32	SCART RIGHT	V_{i4}	X5	X	0	X	X	0	1	0	1
1	32	SCART STEREO	V_{i3} and V_{i4}	X6	X	0	X	X	0	1	1	0
3	3	MAIN LEFT	V_{i5}	XC	X	0	X	X	1	1	0	0
5	5	MAIN RIGHT	V_{i6}	XD	X	0	X	X	1	1	0	1
3	5	MAIN STEREO	V_{i5} and V_{i6}	X8	X	0	X	X	1	0	0	0

Note

1. X = don’t care

Table 4 Effect controls.

SETTING SPECIAL MODES	HEX	DATA BYTE TO SUBADDRESS 09							
		EF2	MU2	EF1	ST	I23	I22	I21	I20
stereo with spatial (52%)	BX	1	0	1	1	X	X	X	X
stereo with spatial (30%)	3X	0	0	1	1	X	X	X	X
stereo without spatial	1X	0	0	0	1	X	X	X	X
forced mono with pseudo stereo	2X	0	0	1	0	X	X	X	X
forced mono without pseudo stereo	0X	0	0	0	0	X	X	X	X

Table 5 Volume 2 / balance control LEFT.

G_v	DATA					
(dB)	HEX	VL4	VL3	VL2	VL1	VL0
0	1F	1	1	1	1	1
–1	1E	1	1	1	1	0
–2	1D	1	1	1	0	1
–3	1C	1	1	1	0	0
–4	1B	1	1	0	1	1
–5	1A	1	1	0	1	0
–6	19	1	1	0	0	1
–7	18	1	1	0	0	0
–8	17	1	0	1	1	1
–9	16	1	0	1	1	0
–10	15	1	0	1	0	1
–11	14	1	0	1	0	0
–12	13	1	0	0	1	1
–13	12	1	0	0	1	0
–14	11	1	0	0	0	1
–15	10	1	0	0	0	0
–16	0F	0	1	1	1	1
–17	0E	0	1	1	1	0
–18	0D	0	1	1	0	1
–19	0C	0	1	1	0	0
–20	0B	0	1	0	1	1
–21	0A	0	1	0	1	0
–22	09	0	1	0	0	1
–23	08	0	1	0	0	0
mute left	07	0	0	1	1	1

Table 6 Volume 2 / balance control RIGHT.

G_v	DATA					
(dB)	HEX	VR4	VR3	VR2	VR1	VR0
0	1F	1	1	1	1	1
–1	1E	1	1	1	1	0
–2	1D	1	1	1	0	1
–3	1C	1	1	1	0	0
–4	1B	1	1	0	1	1
–5	1A	1	1	0	1	0
–6	19	1	1	0	0	1
–7	18	1	1	0	0	0
–8	17	1	0	1	1	1
–9	16	1	0	1	1	0
–10	15	1	0	1	0	1
–11	14	1	0	1	0	0
–12	13	1	0	0	1	1
–13	12	1	0	0	1	0
–14	11	1	0	0	0	1
–15	10	1	0	0	0	0
–16	0F	0	1	1	1	1
–17	0E	0	1	1	1	0
–18	0D	0	1	1	0	1
–19	0C	0	1	1	0	0
–20	0B	0	1	0	1	1
–21	0A	0	1	0	1	0
–22	09	0	1	0	0	1
–23	08	0	1	0	0	0
mute right	07	0	0	1	1	1

Table 7 Volume 1 to control both channels.

G_v	DATA						
(dB)	HEX	V05	V04	V03	V02	V01	V00
+15	3F	1	1	1	1	1	1
+14	3E	1	1	1	1	1	0
+13	3D	1	1	1	1	0	1
+12	3C	1	1	1	1	0	0
+11	3B	1	1	1	0	1	1
+10	3A	1	1	1	0	1	0
+9	39	1	1	1	0	0	1
+8	38	1	1	1	0	0	0
+7	37	1	1	0	1	1	1
+6	36	1	1	0	1	1	0
+5	35	1	1	0	1	0	1
+4	34	1	1	0	1	0	0
+3	33	1	1	0	0	1	1
+2	32	1	1	0	0	1	0
+1	31	1	1	0	0	0	1
0	30	1	1	0	0	0	0
–1	2F	1	0	1	1	1	1
–2	2E	1	0	1	1	1	0
–3	2D	1	0	1	1	0	1
–4	2C	1	0	1	1	0	0
–5	2B	1	0	1	0	1	1
–6	2A	1	0	1	0	1	0
–7	29	1	0	1	0	0	1
–8	28	1	0	1	0	0	0
–9	27	1	0	0	1	1	1
–10	26	1	0	0	1	1	0
–11	25	1	0	0	1	0	1
–12	24	1	0	0	1	0	0
–13	23	1	0	0	0	1	1
–14	22	1	0	0	0	1	0
–15	21	1	0	0	0	0	1
–16	20	1	0	0	0	0	0

G_v	DATA						
(dB)	HEX	V05	V04	V03	V02	V01	V00
–17	1F	0	1	1	1	1	1
–18	1E	0	1	1	1	1	0
–19	1D	0	1	1	1	0	1
–20	1C	0	1	1	1	0	0
–21	1B	0	1	1	0	1	1
–22	1A	0	1	1	0	1	0
–23	19	0	1	1	0	0	1
–24	18	0	1	1	0	0	0
–25	17	0	1	0	1	1	1
–26	16	0	1	0	1	1	0
–27	15	0	1	0	1	0	1
–28	14	0	1	0	1	0	0
–29	13	0	1	0	0	1	1
–30	12	0	1	0	0	1	0
–31	11	0	1	0	0	0	1
–32	10	0	1	0	0	0	0
–33	0F	0	0	1	1	1	1
–34	0E	0	0	1	1	1	0
–35	0D	0	0	1	1	0	1
–36	0C	0	0	1	1	0	0
–37	0B	0	0	1	0	1	1
–38	0A	0	0	1	0	1	0
–39	09	0	0	1	0	0	1
–40	08	0	0	1	0	0	0

Table 8 Bass control LEFT and RIGHT.

G_v	DATA					
(dB)	HEX	BA4	BA3	BA2	BA1	BA0
+15	19	1	1	0	0	1
+13.5	18	1	1	0	0	0
+12	17	1	0	1	1	1
+10.5	16	1	0	1	1	0
+9	15	1	0	1	0	1
+7.5	14	1	0	1	0	0
+6	13	1	0	0	1	1
+4.5	12	1	0	0	1	0
+3	11	1	0	0	0	1
+1.5	10	1	0	0	0	0
0	0F	0	1	1	1	1
0	0E	0	1	1	1	0
−1.5	0D	0	1	1	0	1
−3	0C	0	1	1	0	0
−4.5	0B	0	1	0	1	1
−6	0A	0	1	0	1	0
−7.5	09	0	1	0	0	1
−9	08	0	1	0	0	0
−10.5	07	0	0	1	1	1
−12	06	0	0	1	1	0

Table 9 Treble control LEFT and RIGHT.

G_v	DATA					
(dB)	HEX	0	TR3	TR2	TR1	TR0
+12	0A	0	1	0	1	0
+9	09	0	1	0	0	1
+6	08	0	1	0	0	0
+3	07	0	0	1	1	1
0	06	0	0	1	1	0
−3	05	0	0	1	0	1
−6	04	0	0	1	0	0
−9	03	0	0	0	1	1
−12	02	0	0	0	1	0

Table 10 Volume control of headphone LEFT.

G_v (dB)	DATA						
	HEX	VHL 5	VHL 4	VHL 3	VHL 2	VHL 1	VHL 0
+16	3F	1	1	1	1	1	1
+14	3E	1	1	1	1	1	0
+12	3D	1	1	1	1	0	1
+10	3C	1	1	1	1	0	0
+8	3B	1	1	1	0	1	1
+6	3A	1	1	1	0	1	0
+4	39	1	1	1	0	0	1
+2	38	1	1	1	0	0	0
0	37	1	1	0	1	1	1
–2	36	1	1	0	1	1	0
–4	35	1	1	0	1	0	1
–6	34	1	1	0	1	0	0
–8	33	1	1	0	0	1	1
–10	32	1	1	0	0	1	0
–12	31	1	1	0	0	0	1
–14	30	1	1	0	0	0	0
–16	2F	1	0	1	1	1	1
–18	2E	1	0	1	1	1	0
–20	2D	1	0	1	1	0	1
–22	2C	1	0	1	1	0	0
–24	2B	1	0	1	0	1	1
–26	2A	1	0	1	0	1	0
–28	29	1	0	1	0	0	1
–30	28	1	0	1	0	0	0
–32	27	1	0	0	1	1	1
–34	26	1	0	0	1	1	0
–36	25	1	0	0	1	0	1
–38	24	1	0	0	1	0	0
–40	23	1	0	0	0	1	1
–42	22	1	0	0	0	1	0
–44	21	1	0	0	0	0	1
–46	20	1	0	0	0	0	0
–48	1F	0	1	1	1	1	1
–50	1E	0	1	1	1	1	0
–52	1D	0	1	1	1	0	1
–54	1C	0	1	1	1	0	0
mute left	1B	0	1	1	0	1	1

Table 11 Volume control of headphone RIGHT.

G_v (dB)	DATA						
	HEX	VHR 5	VHR 4	VHR 3	VHR 2	VHR 1	VHR 0
+16	3F	1	1	1	1	1	1
+14	3E	1	1	1	1	1	0
+12	3D	1	1	1	1	0	1
+10	3C	1	1	1	1	0	0
+8	3B	1	1	1	0	1	1
+6	3A	1	1	1	0	1	0
+4	39	1	1	1	0	0	1
+2	38	1	1	1	0	0	0
0	37	1	1	0	1	1	1
–2	36	1	1	0	1	1	0
–4	35	1	1	0	1	0	1
–6	34	1	1	0	1	0	0
–8	33	1	1	0	0	1	1
–10	32	1	1	0	0	1	0
–12	31	1	1	0	0	0	1
–14	30	1	1	0	0	0	0
–16	2F	1	0	1	1	1	1
–18	2E	1	0	1	1	1	0
–20	2D	1	0	1	1	0	1
–22	2C	1	0	1	1	0	0
–24	2B	1	0	1	0	1	1
–26	2A	1	0	1	0	1	0
–28	29	1	0	1	0	0	1
–30	28	1	0	1	0	0	0
–32	27	1	0	0	1	1	1
–34	26	1	0	0	1	1	0
–36	25	1	0	0	1	0	1
–38	24	1	0	0	1	0	0
–40	23	1	0	0	0	1	1
–42	22	1	0	0	0	1	0
–44	21	1	0	0	0	0	1
–46	20	1	0	0	0	0	0
–48	1F	0	1	1	1	1	1
–50	1E	0	1	1	1	1	0
–52	1D	0	1	1	1	0	1
–54	1C	0	1	1	1	0	0
mute right	1B	0	1	1	0	1	1

CURVE	CAPACITANCE AT PIN 29 (nF)	CAPACITANCE AT PIN 27 (nF)	EFFECT
1	15	15	normal
2	47	5.6	intensified
3	68	5.6	more intensified

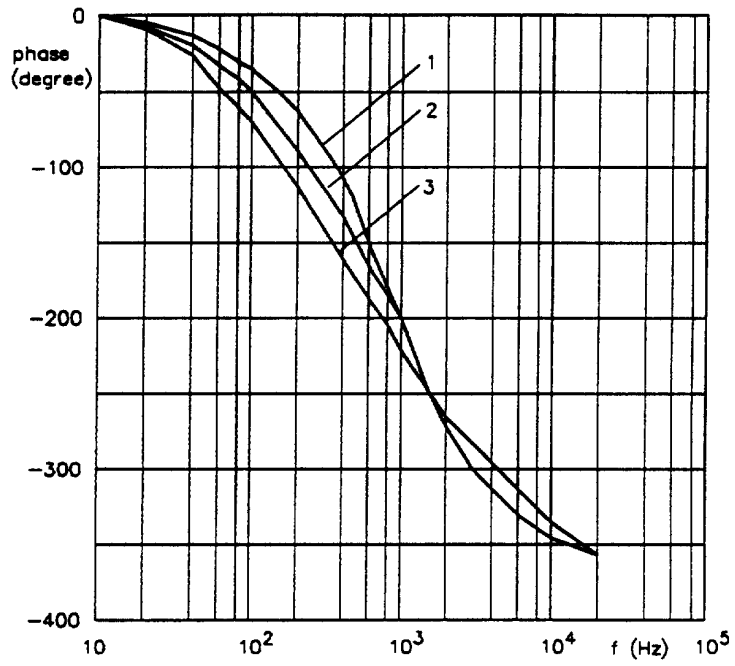
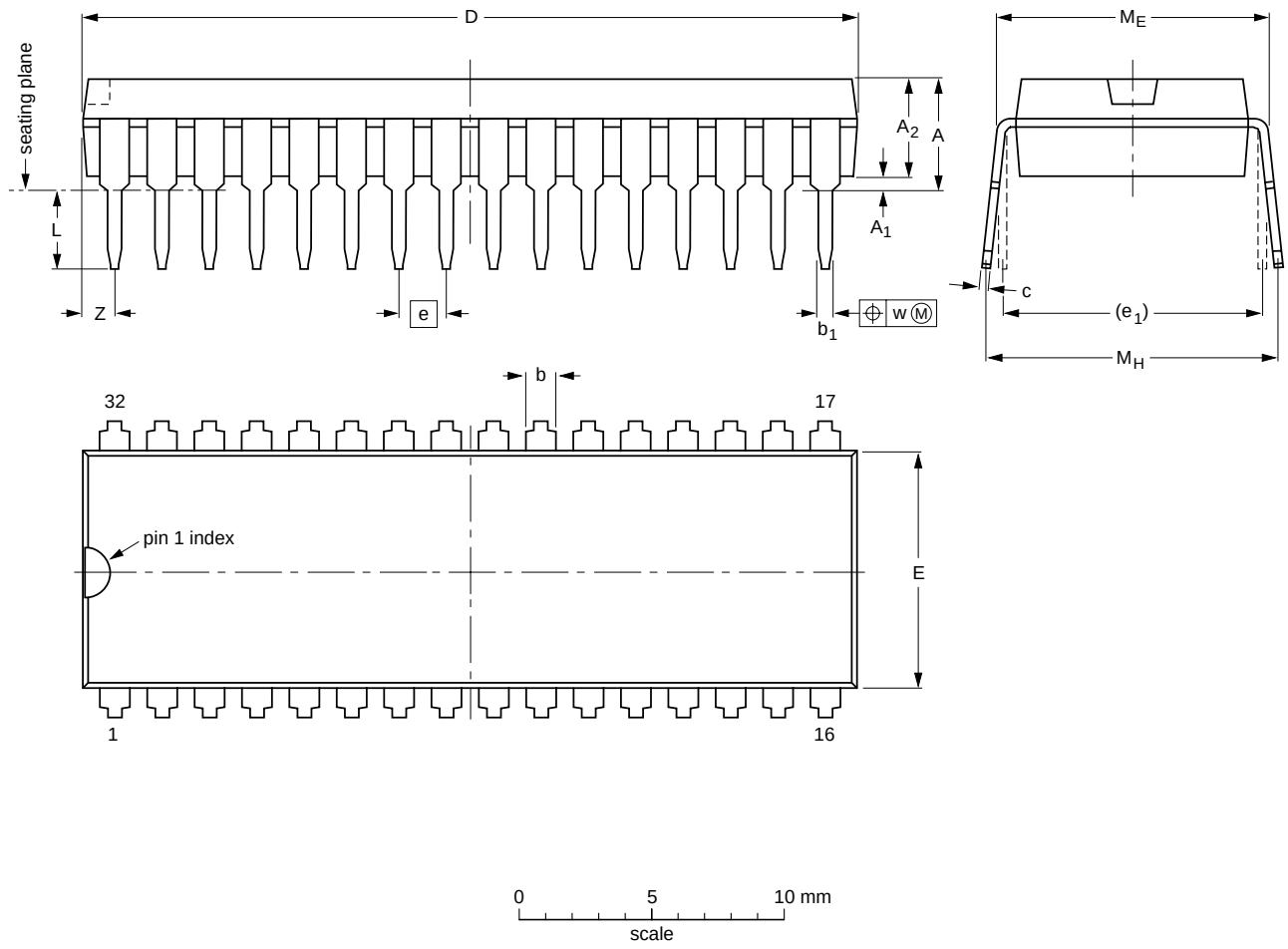


Fig.3 Pseudo (phase) as a function of frequency.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been preheated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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