

4,194,304 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514100APL/AJL/ASJL/AZL is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100APL/AJL/ASJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100APL/AJL/ASJL/AZL to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

		TC514100APL/AJL/ASJL/AZL - 70/80/10		
t _{RAC}	\overline{RAS} Access Time	70ns	80ns	100ns
t _{AA}	Column Address Access Time	35ns	40ns	50ns
t _{CAC}	\overline{CAS} Access Time	20ns	20ns	25ns
t _{RC}	Cycle Time	130ns	150ns	180ns
t _{PC}	Fast Page Mode Cycle Time	45ns	50ns	60ns

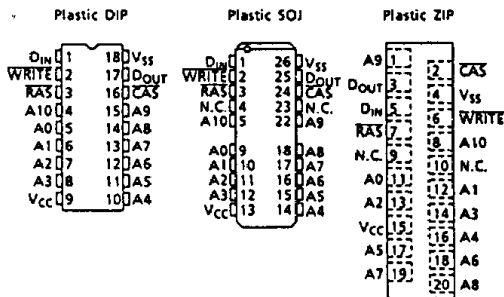
- Single power supply of 5V±10% with a built-in V_{BB} generator

- Low Power
 550mW MAX. Operating (TC514100APL/AJL/ASJL/AZL-70)
 468mW MAX. Operating (TC514100APL/AJL/ASJL/AZL-80)
 413mW MAX. Operating (TC514100APL/AJL/ASJL/AZL-10)
 1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, \overline{RAS} -only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514100APL : DIP18-P-300E
 TC514100AJL : SOJ26-P-350
 TC514100ASJL : SOJ26-P-300A
 TC514400AZL : ZIP20-P-400A

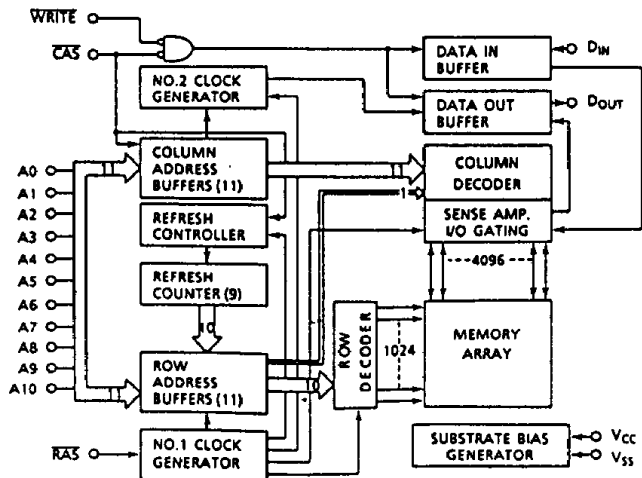
PIN NAMES

A0~A10	Address Inputs	WRITE	Read/Write Input
\overline{RAS}	Row Address Strobe	V _{CC}	Power (+5V)
D _{IN}	Data In	V _{SS}	Ground
D _{OUT}	Data Out	N.C.	No Connection
\overline{CAS}	Column Address Strobe		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80 TC514100APL/AJL/ASJL/AZL-10

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80 TC514100APL/AJL/ASJL/AZL-10

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I _{CC1}	OPERATING CURRENT Average Power Supply Operating Current (\overline{RAS} , \overline{CAS} , Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514100APL/AJL/ASJL/AZL-70	-	100	mA	3, 4
		TC514100APL/AJL/ASJL/AZL-80	-	85		
		TC514100APL/AJL/ASJL/AZL-10	-	75		5
I _{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	-	2	mA		
I _{CC3}	\overline{RAS} ONLY REFRESH CURRENT Average Power Supply Current, \overline{RAS} Only Mode (\overline{RAS} Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514100APL/AJL/ASJL/AZL-70	-	100	mA	3, 5
		TC514100APL/AJL/ASJL/AZL-80	-	85		
		TC514100APL/AJL/ASJL/AZL-10	-	75		
I _{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, \overline{CAS} , Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC514100APL/AJL/ASJL/AZL-70	-	70	mA	3, 4
		TC514100APL/AJL/ASJL/AZL-80	-	60		
		TC514100APL/AJL/ASJL/AZL-10	-	55		5
I _{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	-	200	μA		
I _{CC6}	\overline{CAS} BEFORE \overline{RAS} REFRESH CURRENT Average Power Supply Current, \overline{CAS} Before \overline{RAS} Mode (\overline{RAS} , \overline{CAS} Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514100APL/AJL/ASJL/AZL-70	-	100	mA	3, 5
		TC514100APL/AJL/ASJL/AZL-80	-	85		
		TC514100APL/AJL/ASJL/AZL-10	-	75		
I _{CC7}	Battery Back Up Current Average power Supply Current, Battery Back Up Mode ($\overline{CAS} = \overline{CAS}$ Before \overline{RAS} Cycling or 0.2V, $\overline{WRITE} = V_{CC} - 0.2V$ $A_0 \sim 10 = V_{CC} - 0.2V$ or 0.2V, $D_{IN} = V_{CC} - 0.2V$, 0.2V or OPEN: $t_{RC} = 125\mu s$, $t_{RAS} = 300ns \sim 1\mu s$)	-	400	μA	3, 6	
I _{CC7}	Battery Back Up Current Average power Supply Current, Battery Back Up Mode ($\overline{CAS} = \overline{CAS}$ Before \overline{RAS} Cycling or 0.2V, $\overline{WRITE} = V_{CC} - 0.2V$ $A_0 \sim 10 = V_{CC} - 0.2V$ or 0.2V, $D_{IN} = V_{CC} - 0.2V$, 0.2V or OPEN: $t_{RC} = 125\mu s$, $t_{RAS} = t_{RAS}$ MIN. $\sim 300ns$)	-	300	μA	3, 6	
I _{I(L)}	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)	- 10	10	μA		
I _{O(L)}	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)	- 10	10	μA		
V _{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	-	V		
V _{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	-	0.4	V		

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80 TC514100APL/AJL/ASJL/AZL-10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100APL/ AJL/ASJL/AZL-70		TC514100APL/ AJL/ASJL/AZL-80		TC514100APL/ AJL/ASJL/AZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	-	175	-	210	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	60	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	-	75	-	90	-	ns	
t_{RAC}	Access Time from \overline{RAS}	-	70	-	80	-	100	ns	10, 15 16
t_{CAC}	Access Time from \overline{CAS}	-	20	-	20	-	25	ns	10, 15
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	10, 16
t_{CPA}	Access Time from \overline{CAS} Precharge	-	40	-	45	-	55	ns	10
t_{CLZ}	\overline{CAS} to Output in Low-Z	0	-	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{RP}	\overline{RAS} Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	\overline{RAS} Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	\overline{RAS} Pulse Width (Fast Page Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	\overline{RAS} Hold Time	20	-	20	-	25	-	ns	
t_{RHCP}	\overline{RAS} Hold Time From \overline{CAS} Precharge (Fast Page Mode)	40	-	45	-	55	-	ns	
t_{CSH}	\overline{CAS} Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	\overline{CAS} Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	\overline{RAS} to \overline{CAS} Delay Time	20	50	20	60	25	75	ns	15
t_{RAD}	\overline{RAS} to Column Address Delay Time	15	35	15	40	20	50	ns	16
t_{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	5	-	5	-	10	-	ns	
t_{CP}	\overline{CAS} Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{RAL}	Column Address to \overline{RAS} Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to \overline{RAS}	0	-	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	

**TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
TC514100APL/AJL/ASJL/AZL-10**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514100APL/ AJL/ASJL/AZL-70		TC514100APL/ AJL/ASJL/AZL-80		TC514100APL/ AJL/ASJL/AZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t _{RWL}	Write Command to \overline{RAS} Lead Time	20	-	20	-	25	-	ns	
t _{CWL}	Write Command to \overline{CAS} Lead Time	20	-	20	-	25	-	ns	
t _{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	13
t _{DH}	Data Hold Time	15	-	15	-	20	-	ns	13
t _{REF}	Refresh Period	-	128	-	128	-	128	ms	
t _{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	14
t _{CWD}	\overline{CAS} to WRITE Delay Time	20	-	20	-	25	-	ns	14
t _{RWD}	\overline{RAS} to WRITE Delay Time	70	-	80	-	100	-	ns	14
t _{AWD}	Column Address to WRITE Delay Time	35	-	40	-	50	-	ns	14
t _{CPWD}	\overline{CAS} Precharge to WRITE Delay Time	40	-	45	-	55	-	ns	14
t _{CSR}	\overline{CAS} Set-Up Time (\overline{CAS} before \overline{RAS} Cycle)	5	-	5	-	5	-	ns	
t _{CHR}	\overline{CAS} Hold Time (\overline{CAS} before \overline{RAS} Cycle)	15	-	15	-	20	-	ns	
t _{RPC}	\overline{RAS} to \overline{CAS} Precharge Time	0	-	0	-	0	-	ns	
t _{CPT}	\overline{CAS} Precharge Time (\overline{CAS} before \overline{RAS} Counter Test Cycle)	40	-	40	-	50	-	ns	
t _{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	10	-	ns	
t _{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t _{WRP}	WRITE to \overline{RAS} Precharge Time (\overline{CAS} before \overline{RAS} Cycle)	10	-	10	-	10	-	ns	
t _{WRH}	WRITE to \overline{RAS} Hold Time (\overline{CAS} before \overline{RAS} Cycle)	10	-	10	-	10	-	ns	

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80 TC514100APL/AJL/ASJL/AZL-10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100APL/ AJL/ASJL/AZL-70		TC514100APL/ AJL/ASJL/AZL-80		TC514100APL/ AJL/ASJL/AZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read Write Cycle Time	135	-	155	-	185	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	180	-	215	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	65	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns	14
t_{RAC}	Access Time from \overline{RAS}	-	75	-	85	-	105	ns	10, 15 16
t_{CAC}	Access Time from \overline{CAS}	-	25	-	25	-	30	ns	10, 15
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	10, 16
t_{CPA}	Access Time from \overline{CAS} Precharge	-	45	-	50	-	60	ns	10
t_{RAS}	\overline{RAS} Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASP}	\overline{RAS} Pulse Width (Fast Page Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	\overline{RAS} Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	\overline{CAS} Hold Time	75	-	85	-	105	-	ns	
t_{RHCP}	\overline{CAS} Precharge to \overline{RAS} Hold Time	40	-	50	-	60	-	ns	
t_{CAS}	\overline{CAS} Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to \overline{RAS} Lead Time	40	-	45	-	55	-	ns	
t_{CWD}	\overline{CAS} to \overline{WRITE} Delay Time	25	-	25	-	30	-	ns	14
t_{RWD}	\overline{RAS} to \overline{WRITE} Delay Time	75	-	85	-	105	-	ns	14
t_{AWD}	Column Address to \overline{WRITE} Delay Time	40	-	45	-	55	-	ns	14
t_{CPWD}	\overline{CAS} Precharge to \overline{WRITE} Delay Time	45	-	50	-	60	-	ns	14

CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $f = 1MHz$, $T_a = 0 \sim 70^\circ C$)

*SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance ($A_0 \sim A_{10}$, D_{IN})	-	5	pF
C_{I2}	Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{WRITE})	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80 TC514100APL/AJL/ASJL/AZL-10

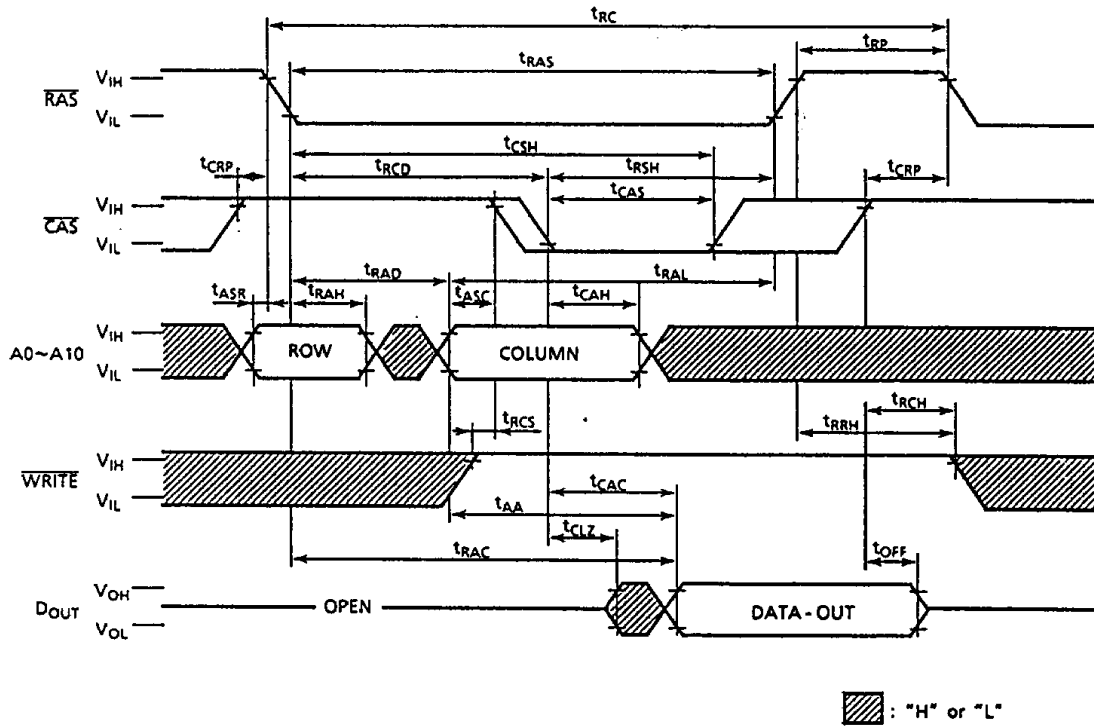
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. $ICC1$, $ICC3$, $ICC4$, $ICC6$, $ICC7$ depend on cycle rate.
4. $ICC1$, $ICC4$ depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. $t_{RAS}(\max.)=1\mu s$ is only applied to refresh of battery-back up. $t_{RAS}(\max.)=10\mu s$ is applied to functional operating.
7. An initial pause of $200\mu s$ is required after power-up followed by 8 \overline{RAS} only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CAS} before \overline{RAS} refresh cycles instead of 8 \overline{RAS} only refresh cycles are required.
8. AC measurements assume $t_T=5ns$.
9. $V_{IH}(\min.)$ and $V_{IL}(\max.)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. $t_{OFF}(\max.)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WRITE} leading edge in read-write cycles.
14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min.)$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD}(\min.)$, $t_{CWD} \geq t_{CWD}(\min.)$, $t_{AWD} \geq t_{AWD}(\min.)$ and $t_{CPWD} \geq t_{CPWD}(\min.)$ (Fast Page Mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the $t_{RCD}(\max.)$ limit insures that $t_{RAC}(\max.)$ can be met. $t_{RCD}(\max.)$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\max.)$ limit, then access time is controlled by t_{CAC} .
16. Operation within the $t_{RAD}(\max.)$ limit insures that $t_{RAC}(\max.)$ can be met. $t_{RAD}(\max.)$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\max.)$ limit, then access time is controlled by t_{AA} .

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80 TC514100APL/AJL/ASJL/AZL-10

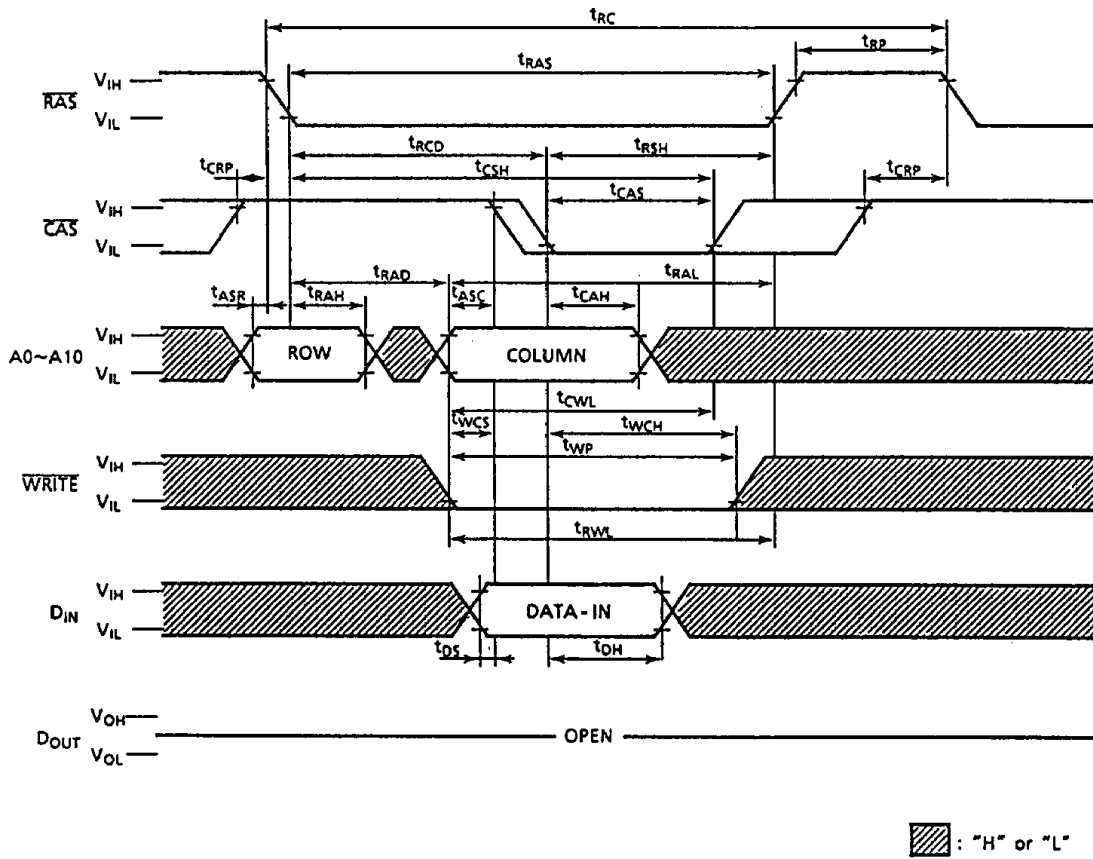
TIMING WAVEFORMS

READ CYCLE



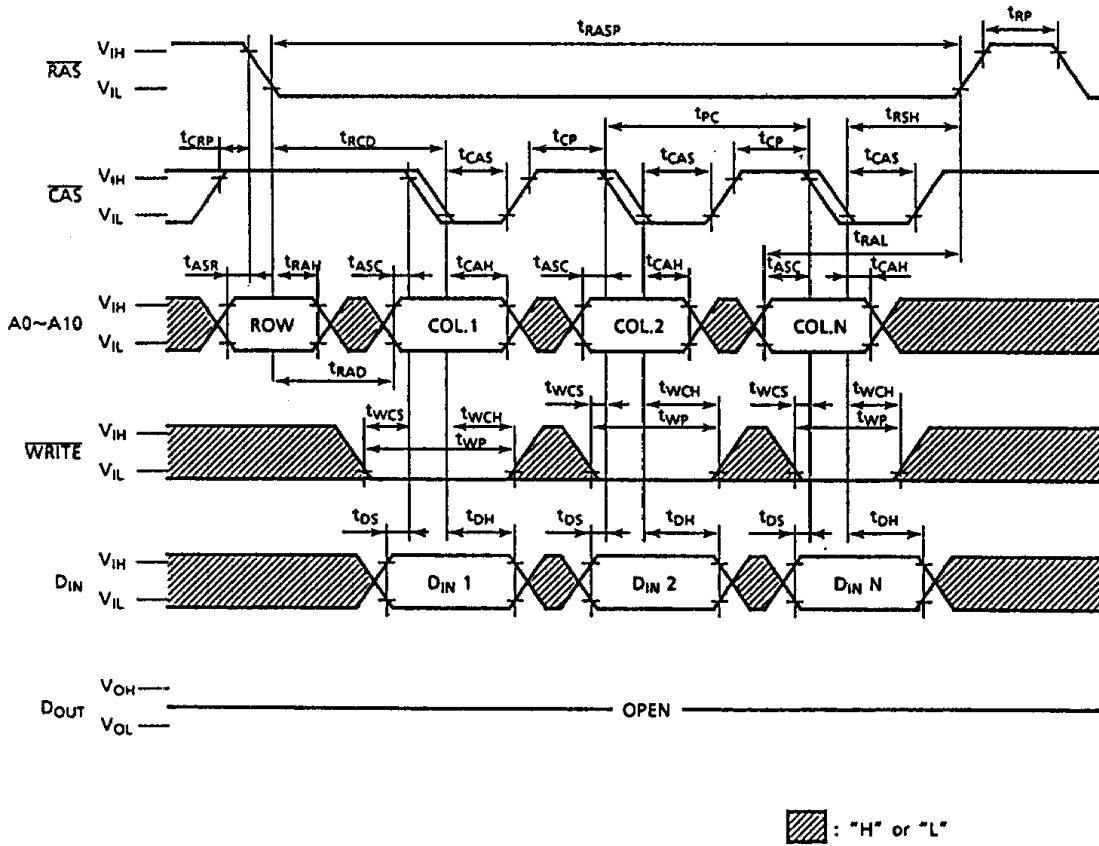
TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

WRITE CYCLE (EARLY WRITE)



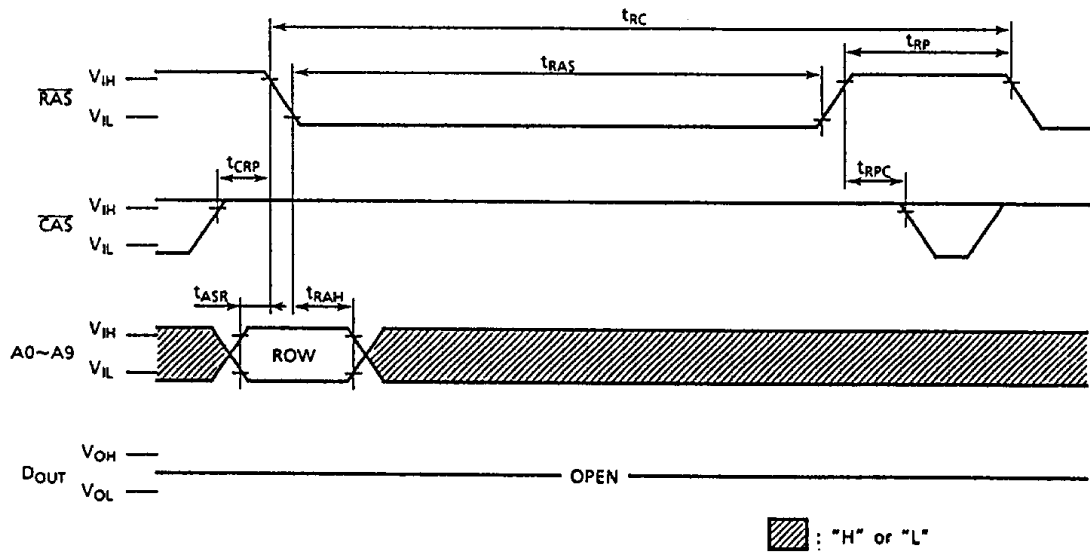
TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

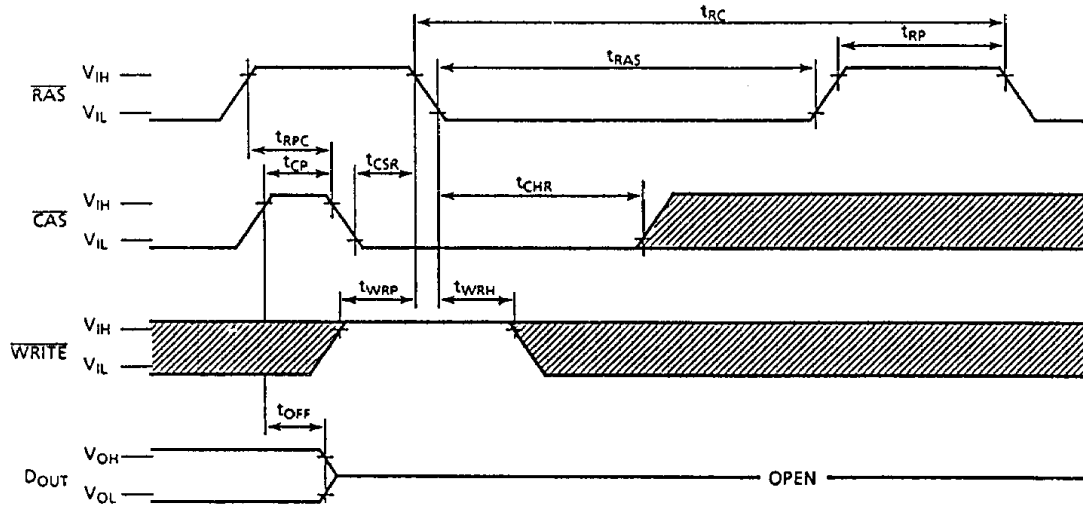
RAS ONLY REFRESH CYCLE




Note: WRITE, A10="H" or "L"

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

CAS BEFORE RAS REFRESH CYCLE

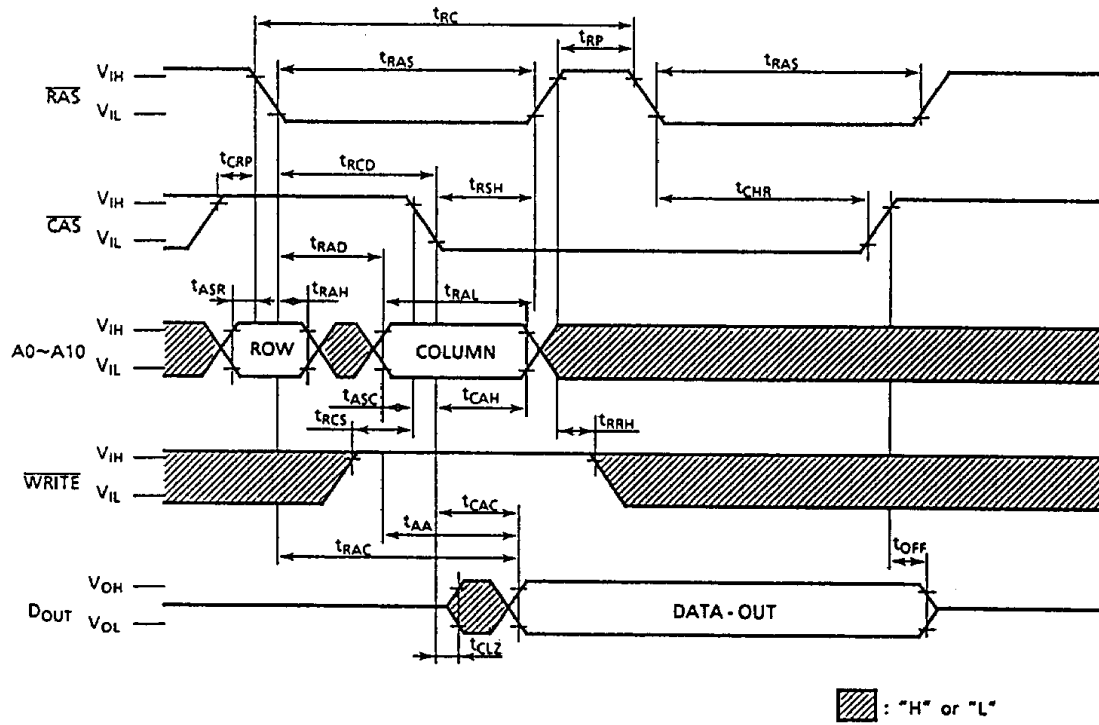


Note: A0~A10 = "H" or "L"

 : "H" or "L"

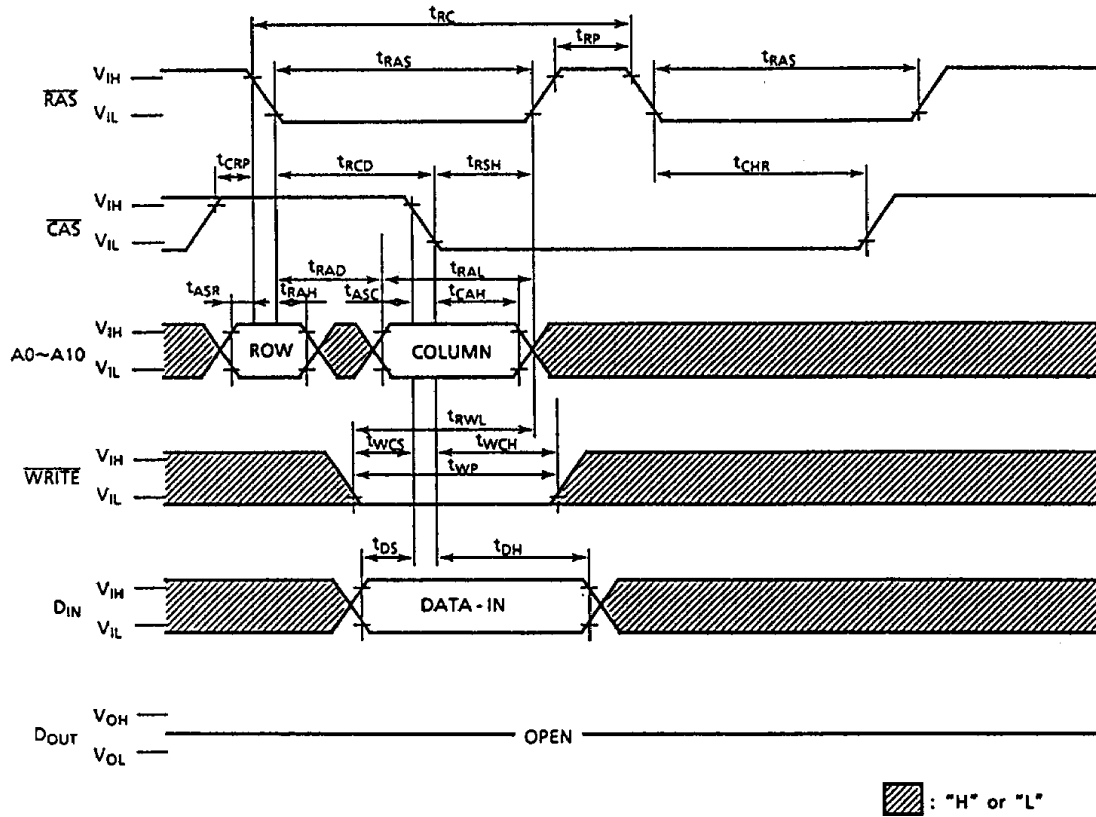
TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

HIDDEN REFRESH CYCLE (READ)



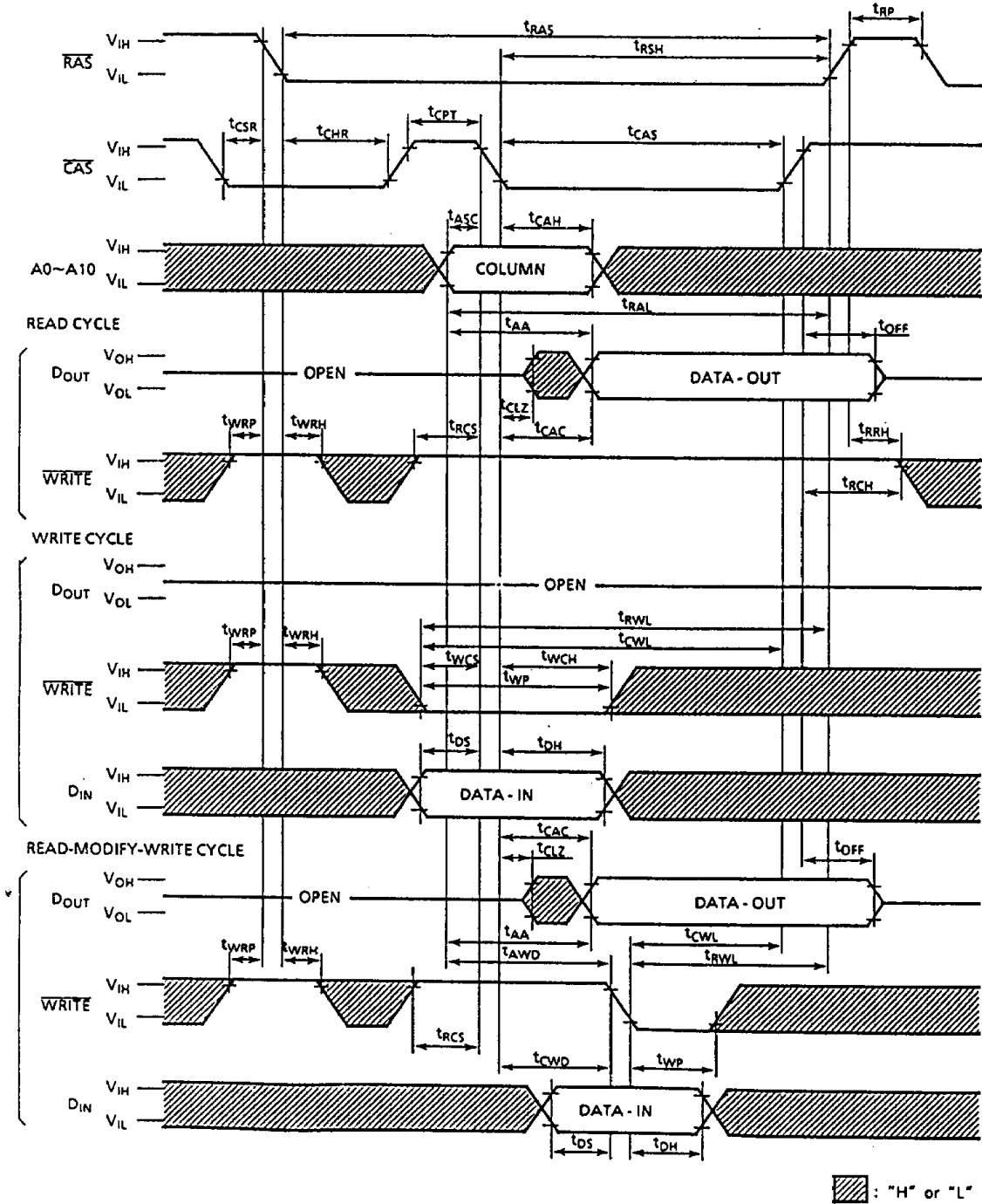
TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

HIDDEN REFRESH CYCLE (WRITE)



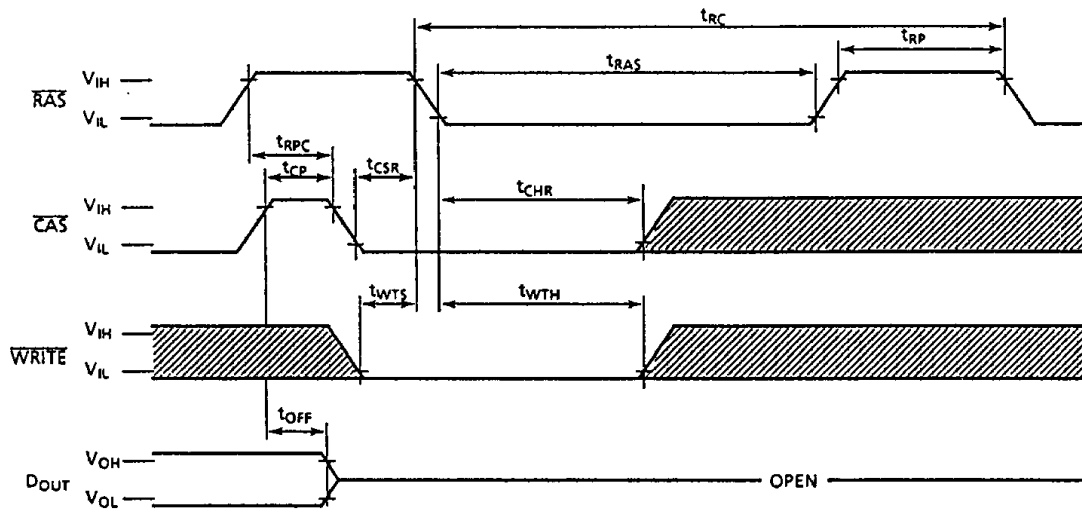
TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE




TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

WRITE, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



Note: D_{IN} , $A_0 \sim A_{10} = \text{"H" or "L"}$

 : "H" or "L"

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80 TC514100APL/AJL/ASJL/AZL-10

TEST MODE

The TC514100APL/AJL/ASJL/AZL is the RAM organized 4,194,304 words by 1 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, and A_{0C} are not used. If, upon reading, all bits equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig.1 shows the block diagram of TC514100APL/AJL/ASJL/AZL. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"WRITE, CAS Before RAS Refresh Cycle" puts the device into "Test Mode". And "CAS Before RAS Refresh Cycle" or "RAS Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "WRITE, CAS Before RAS Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

TC514100APL/AJL/ASJL/AZL-70, TC514100APL/AJL/ASJL/AZL-80
 TC514100APL/AJL/ASJL/AZL-10

BLOCK DIAGRAM IN THE TEST MODE

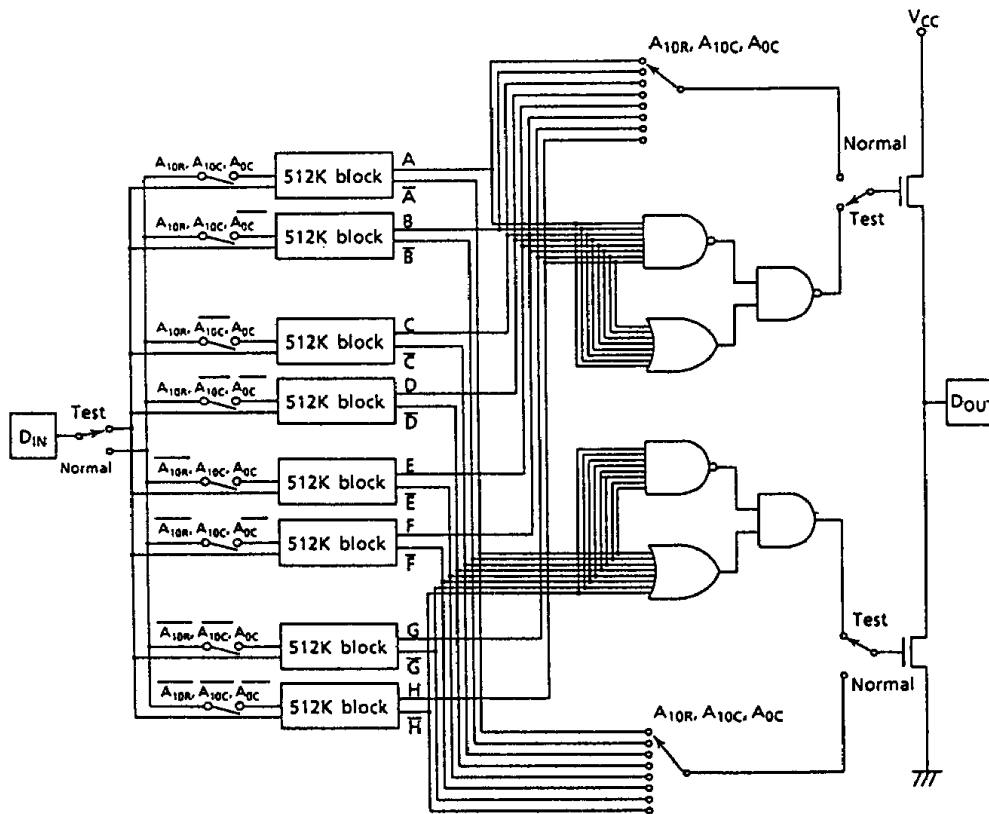


Fig. 1