
MSM7543/7544

Single Rail CODEC

GENERAL DESCRIPTION

The MSM7543 and MSM7544 are single-channel CODEC CMOS ICs for voice signals ranging from 300 to 3400 Hz. These devices contain filters for A/D and D/A conversion.

Designed especially for a single-power supply and low-power applications, these devices are optimized for telephone terminals in digital wireless systems, ISDN terminals, and digital PBXs. The MSM7543 and MSM7544 use newly-designed operational amplifiers to keep small current deviations caused by power voltage fluctuations.

The devices use the same transmission clocks as those used in the MSM7508B and MSM7509B. The analog output signal, which is of a differential type and can drive a 600 Ω load, can directly drive a handset receiver.

FEATURES

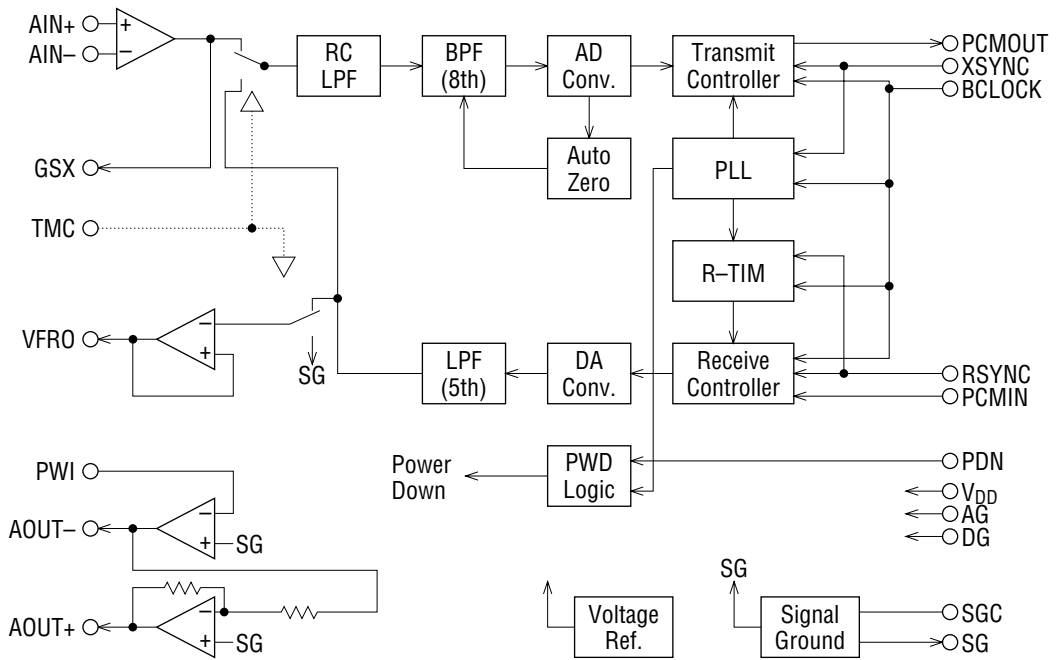
- Single power supply: +5 V \pm 5%
- Low power consumption

| | | | |
|------------------|-------------|--------------|-----------------------|
| Operating mode: | 20 mW Typ. | 31.5 mW Max. | $V_{DD} = 5\text{ V}$ |
| Power save mode: | 4.5 mW Typ. | 8 mW Max. | $V_{DD} = 5\text{ V}$ |
| Power down mode: | 1.5 mW Typ. | 3 mW Max. | $V_{DD} = 5\text{ V}$ |
- ITU-T Companding law

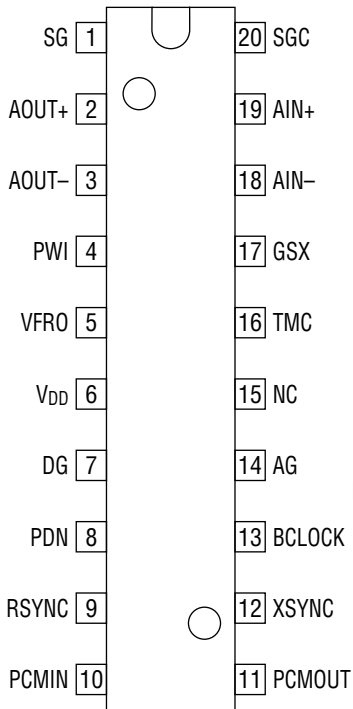
| | |
|----------|------------|
| MSM7543: | μ -law |
| MSM7544: | A-law |
- The transmission characteristics of the devices comply with ITU-T G.714
- Built-in PLL eliminates a master clock
- Serial data rate: 64/128/256/512/1024/2048 kHz
96/192/384/768/1536/1544 kHz
- Adjustable transmit gain
- Adjustable receive gain
- Built-in reference voltage supply
- Built-in analog loop back test mode
- Differential type analog output. Directly drives a 600 Ω line transformer
- Package options:

| | |
|---|------------------------------|
| 20-pin plastic skinny DIP (DIP20-P-300-2.54-S1) | (Product name : MSM7543RS) |
| | (Product name : MSM7544RS) |
| 24-pin plastic SOP (SOP24-P-430-1.27-K) | (Product name : MSM7543GS-K) |
| | (Product name : MSM7544GS-K) |
| 26-pin plastic TSOP (TSOPII26/20-P-300-1.27-K) | (Product name : MSM7543TS-K) |
| | (Product name : MSM7544TS-K) |

BLOCK DIAGRAM

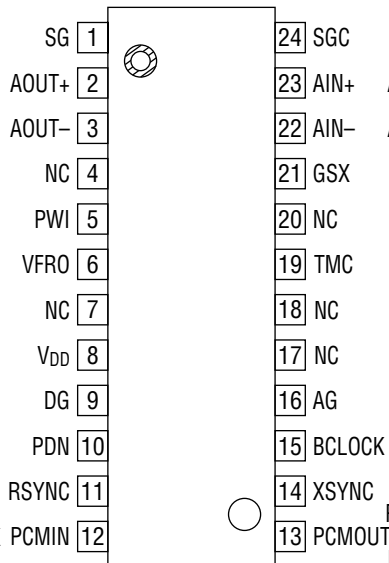


PIN CONFIGURATION (TOP VIEW)



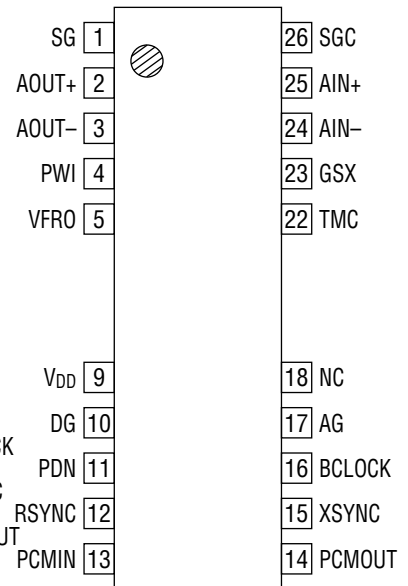
NC : No connect pin

20-Pin Plastic Skinny DIP



NC : No connect pin

24-Pin Plastic SOP



NC : No connect pin

26-Pin Plastic TSOP

PIN AND FUNCTIONAL DESCRIPTIONS

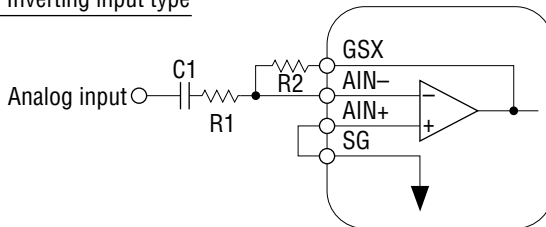
AIN+, AIN-, GSX

Transmit analog input and transmit level adjustment.

AIN+ is a non-inverting input to the op-amp; AIN- is an inverting input to the op-amp; GSX is connected to the output of the op-amp and is used to adjust the level, as shown below.

When not using AIN- and AIN+, connect AIN- to GSX and AIN+ to SG. During power saving and power down modes, the GSX output is at AG voltage.

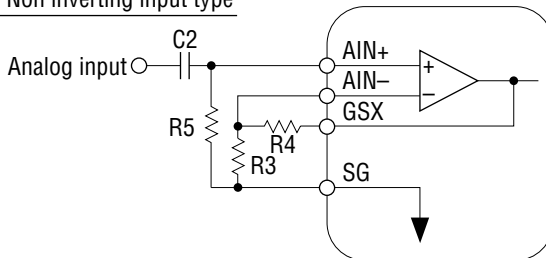
1) Inverting input type



R1 : variable
 R2 > 20 kΩ
 $C1 > 1/(2 \times 3.14 \times 30 \times R1)$

$$\text{Gain} = R2/R1 \leq 10$$

2) Non inverting input type



R3 > 20 kΩ
 R4 > 20 kΩ
 R5 > 50 kΩ
 $C2 > 1/(2 \times 3.14 \times 30 \times R5)$

$$\text{Gain} = 1 + R4 / R3 \leq 10$$

AG

Analog signal ground.

VFRO

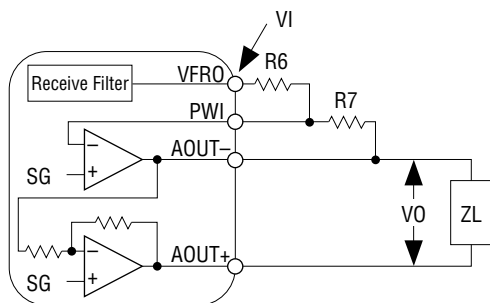
Receive filter output.

The output signal has an amplitude of 2.4 V_{PP} above and below the signal ground voltage (SG) when the digital signal of +3 dBm_O is input to PCMIN and can drive a load of 20 kΩ or more. For driving a load of 20 kΩ or less, connect a resistor of 20 kΩ or more between the pins VFRO and PWI.

When adding the frequency characteristics to the receive signal, refer to the application example. During power saving or power down mode, the output of VFRO is at the voltage level of AG.

PWI, AOUT+, AOUT-

PWI is connected to the inverting input of the receive driver. The receive driver output is connected to the AOUT- pin. Therefore, the receive level can be adjusted with the pins VFRO, PWI, and AOUT-. When the PWI pin is not used, connect the PWI pin to the AOUT- pin, and leave open the pins AOUT- and AOUT+. The output of AOUT+ is inverted with respect to the output of AOUT-. Since the signal from which provides differential drive of an impedance of 1.2 kΩ, these outputs can directly be connected to a receiver of handset using a piezoelectric earphone. Refer to the application example.



$R6 > 20 \text{ k}\Omega$
 $ZL \geq 1.2 \text{ k}\Omega$
 $\text{Gain} = VO/VI = 2 \times R7/R6 \leq 2$

During power saving and power down modes, the outputs of AOUT+ and AOUT- are in a high impedance state .

The electrical driving capability of the AOUT- pin and AOUT+ pin is ±1.3 V maximum. The output load resistor has a minimum value of 0.6 kΩ.

If an output amplitude less than ±1.3 V is allowed, these outputs can drive a load resistance less than that described above.

For more details, refer to SINGLE POWER SUPPLY PCM CODEC APPLICATION NOTE.

VDD

Power supply pin for +5 V.

PCMIN

PCM signal input.

A serial PCM signal input to this pin is converted to an analog signal in synchronization with the RSYNC signal and BCLOCK signal.

The data rate of the PCM signal is equal to the frequency of the BCLOCK signal.

The PCM signal is shifted at a falling edge of the BCLOCK signal and latched into the internal register when shifted by eight bits.

The start of the PCM data (MSD) is identified at the rising edge of RSYNC.

BCLOCK

Shift clock signal input for the PCMIN and PCMOUT signal.

The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, 2048, or 200 kHz. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

RSYNC

Receive synchronizing signal input.

Eight required bits are selected from serial PCM signals on the PCMIN pin by the receive synchronizing signal.

Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLOCK. The frequency should be 8 kHz \pm 50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the receive section.

However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of 8 kHz \pm 2 kHz, but the electrical characteristics in this specification are not guaranteed.

XSYNC

Transmit synchronizing signal input.

The PCM output signal from the PCMOUT pin is output in synchronization with this transmit synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.

This synchronizing signal must be synchronized in phase with BCLOCK.

The frequency should be 8 kHz \pm 50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the transmit section.

However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of 8 kHz \pm 2 kHz, but the electrical characteristics in this specification are not guaranteed.

Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

TMC

Control signal input for mode selection.

This pin select the normal operating mode or the analog loop-back mode.

In the analog loop-back mode, the receive filter output is connected to the transmit filter input and the digital signal input to the PCMIN pin is converted from a digital to an analog signal (D/A conversion). Next, the analog signal is converted to a digital signal (A/D conversion) through the receive filter and transmit filter. The result is output to the PCMOUT pin.

When in the analog loop-back mode, the VFRO pin outputs the SG level. (signal ground)

| TMC Input | Mode |
|-----------|------------------|
| < 0.8 V | Normal operation |
| > 2.2 V | Analog loop-back |

DG

Ground for the digital signal circuits.

This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

PDN

Power down control signal.

A logic "0" level drives both transmit and receive circuits to a power down state.

PCMOUT

PCM signal output.

The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLOCK signal.

MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLOCK and XSYNC.

This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power saving or power down modes.

A pull-up resistor must be connected to this pin because its output is configured as an open drain. This device is compatible with the ITU-T recommendation on coding law and output coding format.

The MSM7544(A-law) outputs the character signal, inverting the even bits.

| Input/Output Level | PCMIN/PCMOUT | | | | | | | | | | | | | | | |
|--------------------|-----------------------|---|---|---|-----------------|---|---|---|---|---|---|---|---|---|---|---|
| | MSM7543 (μ -law) | | | | MSM7544 (A-law) | | | | | | | | | | | |
| | MSD | | | | MSD | | | | | | | | | | | |
| +Full scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| +0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -Full scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

SG

Signal ground voltage output.

The output voltage is 1/2 of the power supply voltage.

The output drive current capability is $\pm 300 \mu A$.

This pin provides the SG level for CODEC peripherals.

This output voltage level is undefined during power saving or power down modes.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor.

Connect a 0.1 μF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|-----------------------|-----------|-----------|------------------------|------|
| Power Supply Voltage | V_{DD} | — | 0 to 7 | V |
| Analog Input Voltage | V_{AIN} | — | -0.3 to $V_{DD} + 0.3$ | V |
| Digital Input Voltage | V_{DIN} | — | -0.3 to $V_{DD} + 0.3$ | V |
| Storage Temperature | T_{STG} | — | -55 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|-----------|--|---|------|----------|----------|
| Power Supply Voltage | V_{DD} | Voltage must be fixed | 4.75 | 5.0 | 5.25 | V |
| Operating Temperature | T_a | — | -30 | +25 | +85 | °C |
| Analog Input Voltage | V_{AIN} | Connect AIN- and GSX | — | — | 2.4 | V_{PP} |
| Digital Input High Voltage | V_{IH} | XSYNC, RSYNC, BCLOCK, PCMIN, PDN, TMC | 2.2 | — | V_{DD} | V |
| Digital Input Low Voltage | V_{IL} | | 0 | — | 0.8 | V |
| Clock Frequency | F_C | BCLOCK | 64, 128, 256, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544, 200 | | | kHz |
| Sync Pulse Frequency | F_S | XSYNC, RSYNC | 6.0 | 8.0 | 10.0 | kHz |
| Clock Duty Ratio | D_C | BCLOCK | 40 | 50 | 60 | % |
| Digital Input Rise Time | t_{ir} | XSYNC, RSYNC, BCLOCK, PCMIN, PDN, TMC | — | — | 50 | ns |
| Digital Input Fall Time | t_{if} | | — | — | 50 | ns |
| Transmit Sync Pulse Setting Time | t_{XS} | BCLOCK→XSYNC, See Timing Diagram | 100 | — | — | ns |
| | t_{SX} | XSYNC→BCLOCK, See Timing Diagram | 100 | — | — | ns |
| Receive Sync Pulse Setting Time | t_{RS} | BCLOCK→RSYNC, See Timing Diagram | 100 | — | — | ns |
| | t_{SR} | RSYNC→BCLOCK, See Timing Diagram | 100 | — | — | ns |
| Sync Pulse Width | t_{WS} | XSYNC, RSYNC | 1 BCLK | — | 100 | μs |
| PCMIN Set-up Time | t_{DS} | — | 100 | — | — | ns |
| PCMIN Hold Time | t_{DH} | — | 100 | — | — | ns |
| Digital Output Load | R_{DL} | Pull-up resistor | 0.5 | — | — | kΩ |
| | C_{DL} | — | — | — | 100 | pF |
| Analog Input Allowable DC Offset | V_{off} | Transmit gain stage, Gain = 1 | -100 | — | +100 | mV |
| | | Transmit gain stage, Gain = 10 | -10 | — | +10 | mV |
| Allowable Jitter Width | — | XSYNC, RSYNC, BCLOCK | — | — | 500 | ns |

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|-----------|--|------|------|----------|---------------|
| Power Supply Current | I_{DD1} | Operating mode, No signal | — | 4.0 | 6.0 | mA |
| | I_{DD2} | Power-save mode, PDN = 1, XSYNC or BCLOCK → OFF | — | 0.9 | 1.5 | mA |
| | I_{DD3} | Power-down mode, PDN = 0 | — | 0.3 | 0.5 | mA |
| Input High Voltage | V_{IH} | — | 2.2 | — | V_{DD} | V |
| Input Low Voltage | V_{IL} | — | 0.0 | — | 0.8 | V |
| High Level Input Leakage Current | I_{IH} | — | — | — | 2.0 | μA |
| Low Level Input Leakage Current | I_{IL} | — | — | — | 0.5 | μA |
| Digital Output Low Voltage | V_{OL} | Pull-up resistance $> 500\ \Omega$ | 0.0 | 0.2 | 0.4 | V |
| Digital Output Leakage Current | I_O | — | — | — | 10 | μA |
| Input Capacitance | C_{IN} | — | — | 5 | — | pF |

Transmit Analog Interface Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------|------------|------------------------|----------|------|------|---------------|
| Input Resistance | R_{INX} | AIN+, AIN- | 10 | — | — | $M\Omega$ |
| Output Load Resistance | R_{LGX} | GSX with respect to SG | 20 | — | — | $k\Omega$ |
| Output Load Capacitance | C_{LGX} | | — | — | 100 | μF |
| Output Amplitude | V_{OGX} | | -1.2 | — | +1.2 | V |
| Offset Voltage | V_{OSGX} | | Gain = 1 | -20 | — | +20 |

Receive Analog Interface Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------|------------|---|------|------|------|---------------|
| Input Resistance | R_{INPW} | PWI | 10 | — | — | $M\Omega$ |
| Output Load Resistance | R_{LVF} | VFRO with respect to SG | 20 | — | — | $k\Omega$ |
| | R_{LAO} | AOUT+, AOUT- (each) with respect to SG | 0.6 | — | — | $k\Omega$ |
| Output Load Capacitance | C_{LVF} | VFRO | — | — | 100 | μF |
| | C_{LAO} | AOUT+, AOUT- | — | — | 50 | μF |
| Output Amplitude | V_{OVF} | VFRO, $R_L = 20\text{ k}\Omega$ with respect to SG | -1.2 | — | +1.2 | V |
| | V_{OAO} | AOUT+, AOUT-, $R_L = 1.2\text{ k}\Omega$ with respect to SG | -1.3 | — | +1.3 | V |
| Offset Voltage | V_{OSVF} | VFRO with respect to SG | -100 | — | +100 | mV |
| | V_{OSAO} | AOUT+, AOUT-, Gain = 1 with respect to SG | -100 | — | +100 | mV |

AC Characteristics

(V_{DD} = +5 V ±5%, T_a = -30°C to +85°C)

| Parameter | Symbol | Freq. (Hz) | Level (dBm0) | Condition | Min. | Typ. | Max. | Unit | |
|-------------------------------------|---------|------------|--------------|-----------|-----------|-----------|-------|------|----|
| Transmit Frequency Response | Loss T1 | 60 | 0 | | 20 | 26 | — | dB | |
| | Loss T2 | 300 | | | -0.20 | +0.07 | +0.20 | | |
| | Loss T3 | 1020 | | | Reference | | | | |
| | Loss T4 | 2020 | | | -0.15 | -0.04 | +0.20 | | |
| | Loss T5 | 3000 | | | -0.15 | +0.06 | +0.20 | | |
| | Loss T6 | 3400 | | | 0 | 0.4 | 0.80 | | |
| Receive Frequency Response | Loss R1 | 300 | 0 | | -0.15 | -0.03 | +0.20 | dB | |
| | Loss R2 | 1020 | | | Reference | | | | |
| | Loss R3 | 2020 | | | -0.15 | -0.02 | +0.20 | | |
| | Loss R4 | 3000 | | | -0.15 | +0.15 | +0.20 | | |
| | Loss R5 | 3400 | | | 0.0 | 0.56 | 0.80 | | |
| Transmit Signal to Distortion Ratio | SD T1 | 1020 | 3 | *1 | *2 | 35 | 43 | — | dB |
| | SD T2 | | 0 | | | 35 | 41 | — | |
| | SD T3 | | -30 | | | 35 | 38 | — | |
| | SD T4 | | -40 | | | 29 | 31.5 | — | |
| | SD T5 | | -45 | | | 24 | 27 | — | |
| | | | | | | 26 | | | |
| Receive Signal to Distortion Ratio | SD R1 | 1020 | 3 | *1 | *2 | 36 | 43 | — | dB |
| | SD R2 | | 0 | | | 36 | 41 | — | |
| | SD R3 | | -30 | | | 36 | 40 | — | |
| | SD R4 | | -40 | | | 30 | 34.5 | — | |
| | SD R5 | | -45 | | | 25 | 30 | — | |
| | | | | | | 27 | | | |
| Transmit Gain Tracking | GT T1 | 1020 | 3 | | | -0.2 | +0.01 | +0.2 | dB |
| | GT T2 | | -10 | | | Reference | | | |
| | GT T3 | | -40 | | | -0.2 | 0 | +0.2 | |
| | GT T4 | | -50 | | | -0.4 | -0.03 | +0.4 | |
| | GT T5 | | -55 | | | -1.2 | +0.15 | +1.2 | |
| Receive Gain Tracking | GT R1 | 1020 | 3 | | | -0.2 | -0.06 | +0.2 | dB |
| | GT R2 | | -10 | | | Reference | | | |
| | GT R3 | | -40 | | | -0.2 | -0.02 | +0.2 | |
| | GT R4 | | -50 | | | -0.4 | -0.02 | +0.4 | |
| | GT R5 | | -55 | | | -0.8 | -0.27 | +0.8 | |

*1 Psophometric filter is used

*2 Upper is specified for the MSM7543, lower for the MSM7544

AC Characteristics (Continued)

(V_{DD} = +5 V ±5%, Ta = -30°C to +85°C)

| Parameter | Symbol | Freq. (Hz) | Level (dBm0) | Condition | Min. | Typ. | Max. | Unit |
|--|-------------------------------------|------------|--------------|---|--|--------|--------|-------|
| Idle Channel Noise | Nidle T | — | — | AIN = SG *1 *2 | — | -74.5 | -70 | dBmOp |
| | Nidle R | — | — | | | *1 *3 | — | |
| | Absolute Level (Initial Difference) | AV T | 1020 | 0 | V _{DD} = 5.0 V Ta = 25°C *4 | 0.580 | 0.6007 | |
| | AV R | 0.580 | | | | 0.6007 | 0.622 | |
| Absolute Level (Deviation of Temperature and Power) | AV Tt | 1020 | 0 | V _{DD} = +5 V ±5% Ta = -30 to 85°C *4 | -0.2 | — | +0.2 | dB |
| | AV Rt | | | | -0.2 | — | +0.2 | dB |
| Absolute Delay | Td | 1020 | 0 | A to A BCLOCK = 64 kHz | — | — | 0.60 | ms |
| Transmit Group Delay | tgdt T1 | 500 | 0 | *5 | — | 0.19 | 0.75 | ms |
| | tgdt T2 | 600 | | | — | 0.11 | 0.35 | |
| | tgdt T3 | 1000 | | | — | 0.02 | 0.125 | |
| | tgdt T4 | 2600 | | | — | 0.05 | 0.125 | |
| | tgdt T5 | 2800 | | | — | 0.07 | 0.75 | |
| Receive Group Delay | tgdt R1 | 500 | 0 | *5 | — | 0.00 | 0.75 | ms |
| | tgdt R2 | 600 | | | — | 0.00 | 0.35 | |
| | tgdt R3 | 1000 | | | — | 0.00 | 0.125 | |
| | tgdt R4 | 2600 | | | — | 0.09 | 0.125 | |
| | tgdt R5 | 2800 | | | — | 0.12 | 0.75 | |
| Crosstalk Attenuation | CR T | 1020 | 0 | TRANS → RECV | 75 | 80 | — | dB |
| | CR R | | | RECV → TRANS | 70 | 76 | — | |

*1 Psophometric filter is used

*2 Upper is specified for the MSM7543, lower for the MSM7544

*3 Input "0" code to PCMIN

*4 AVR is defined at VFRO output

*5 Minimum value of the group delay distortion

AC Characteristics (Continued)

(V_{DD} = +5 V ±5%, T_a = -30°C to +85°C)

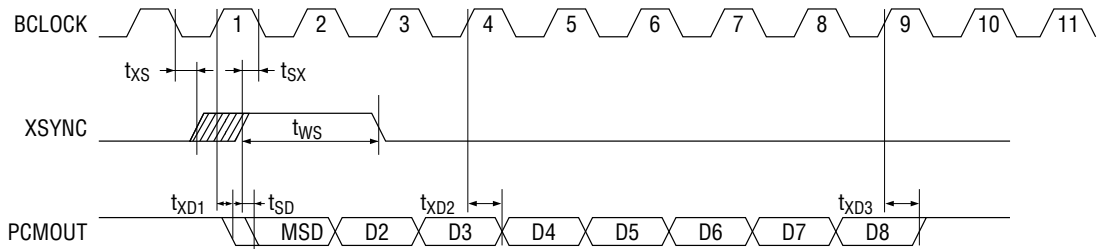
| Parameter | Symbol | Freq. (Hz) | Level (dBm0) | Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|------------------|--|---------------------|----------------------------------|------|-------|------|------|
| Discrimination | DIS | 4.6 kHz to 72 kHz | 0 | 0 to 4000 Hz | 30 | 32 | — | dB |
| Out-of-band Spurious | S | 300 to 3400 | 0 | 4.6 kHz to 100 kHz | — | -37.5 | -35 | dBm0 |
| Intermodulation Distortion | IMD | f _a = 470 f _b = 320 | -4 | 2f _a - f _b | — | -52 | -35 | dBm0 |
| D-to-D Mode Gain | — | 1020 | 0 | TMC = 1 PCMIN to PCMOUT | -1.0 | — | +1.0 | dB |
| Power Supply Noise Rejection Ratio | PSR T | 0 to 50 kHz | 50 mV _{pp} | *6 | — | 30 | — | dB |
| | PSR R | | | | | | | |
| Digital Output Delay Time | t _{SD} | C _L = 100 pF + 1 LSTTL | | | 50 | — | 200 | ns |
| | t _{xD1} | | | | 50 | — | 200 | |
| | t _{xD2} | | | | 50 | — | 200 | |
| | t _{xD3} | | | | 50 | — | 200 | |

*6 The measurement under idle channel noise

TIMING DIAGRAM

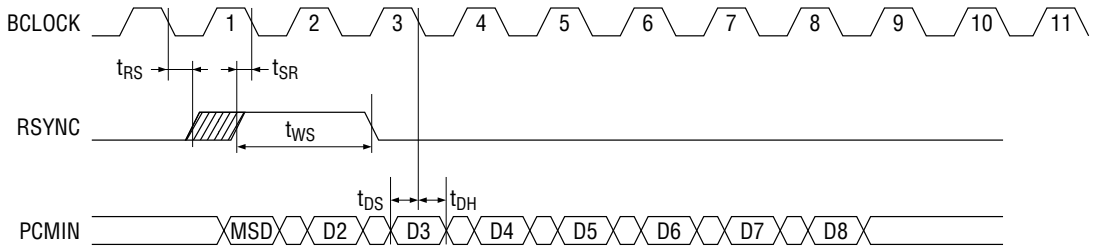
PCM Data Input/Output Timing

Transmit Timing

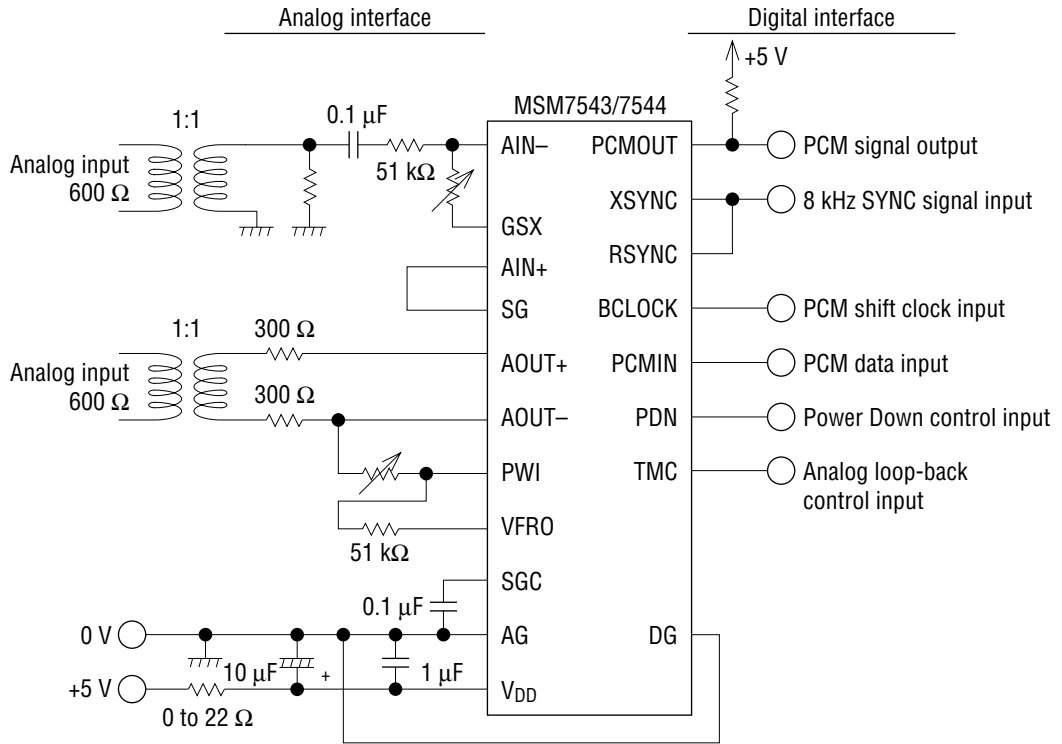


When $t_{XS} \leq 1/2 \cdot F_c$, the Delay of the MSD bit is defined as t_{XD1} .
 When $t_{SX} \leq 1/2 \cdot F_c$, the Delay of the MSD bit is defined as t_{SD} .

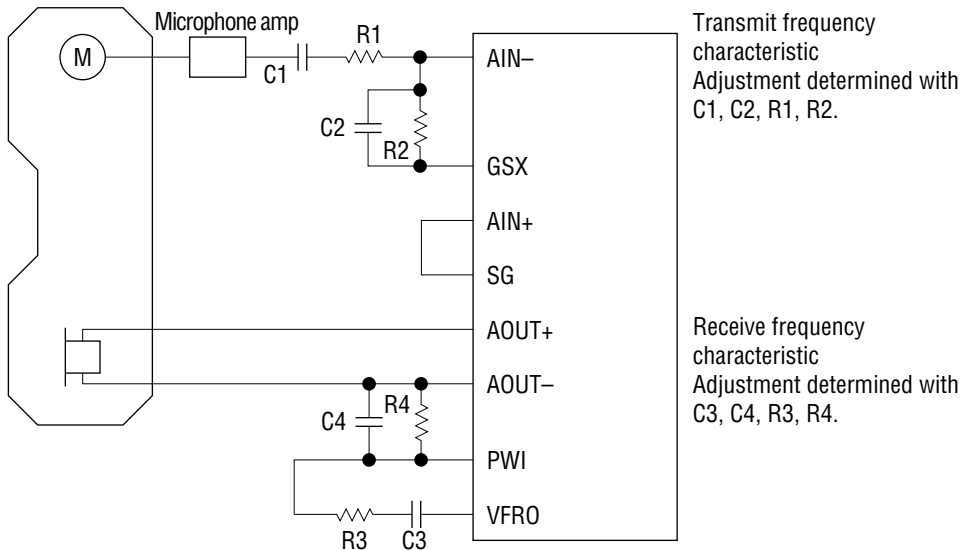
Receive Timing



APPLICATION CIRCUIT



FREQUENCY CHARACTERISTICS ADJUSTMENT CIRCUIT

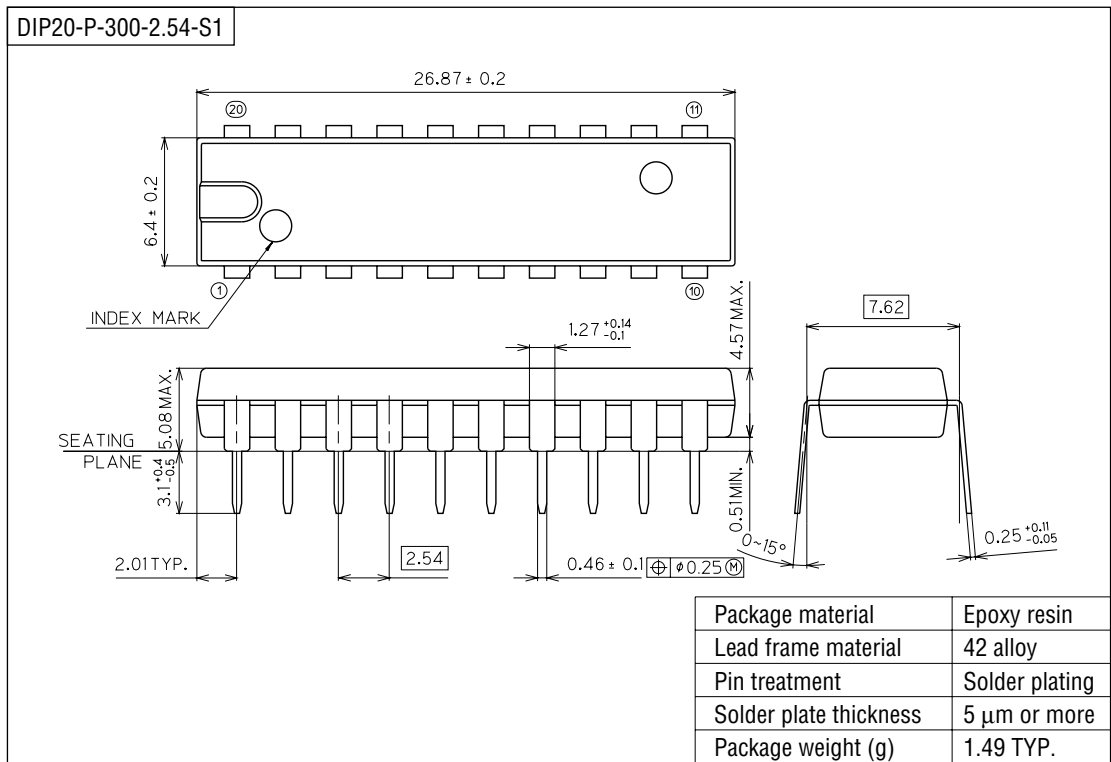


RECOMMENDATIONS FOR ACTUAL DESIGN

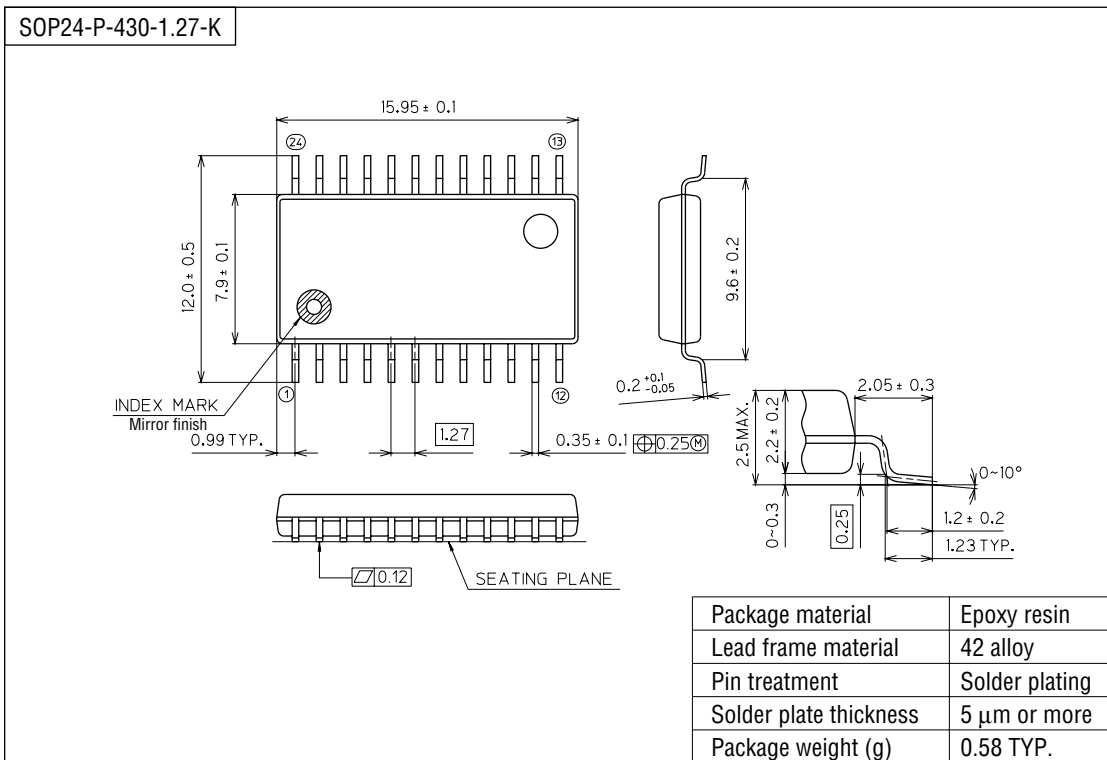
- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin each other as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If an IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.
- Keep the voltage on the V_{DD} pin not lower than -0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

PACKAGE DIMENSIONS

(Unit : mm)



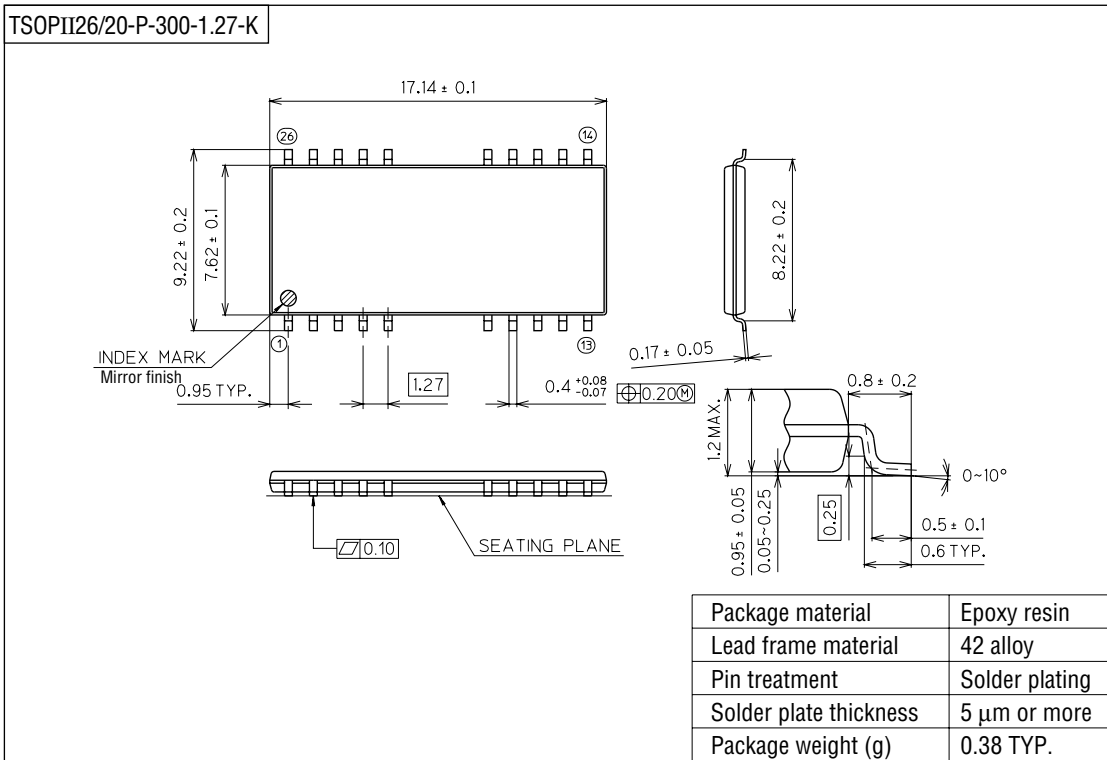
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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