PROCESS

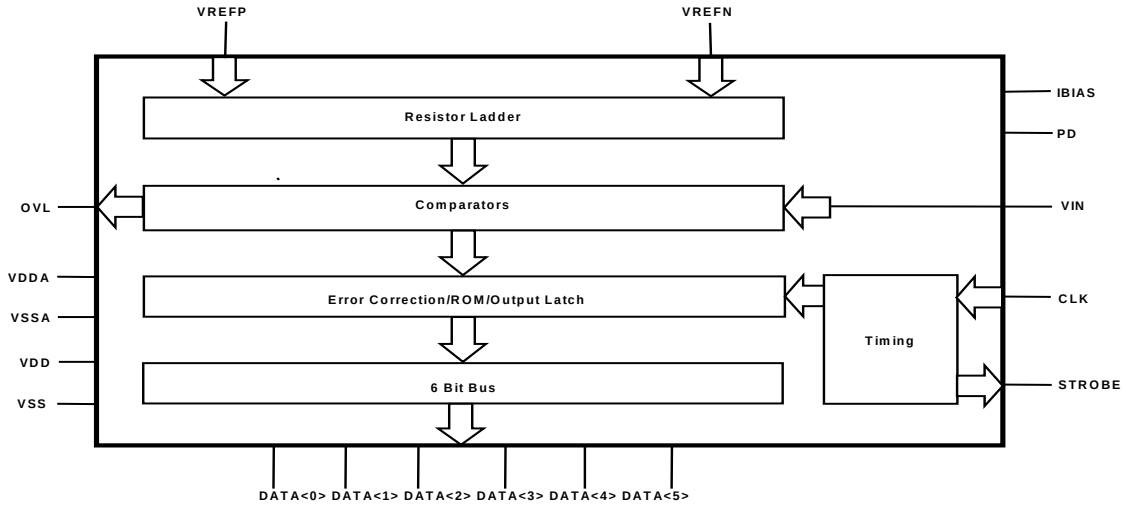
C35B3 (0.35um)

FEATURES

- Small Area < 0.257 mm^2
- Size x= 361 µm y= 710 µm
- Supply Voltage 3.0-3.6 V
- Junction Temp. Range -40 - 125°C
- Resolution 6-Bit
- Maximum Sampling Rate 100MS/s
- Low Input Capacitance < 5pF
- Output Code Binary

DESCRIPTION

The FLASH6 is a complete analog to digital converter cell which operates from a single supply. It performs sampling, analog-to-digital conversion, generating a 6 bit value in parallel form. The output word rate can be up to 100MS/s. The output data format is compatible with most µP and digital signal processors.



TECHNICAL DATA

($T_{junction}$ = -40 to 125 °C, VDDA=VDD=+3.0V to +3.6V, fclk = 100MHz, VREFP and VREFN as specified, pad resistors as specified in the functional block diagram, unless otherwise specified)

DC ACCURACY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution (No missing Code)		6	6	6	Bit
DNL	Differential Linearity Error		-0.8	±0.4	+0.8	LSB
INL	Integral Linearity Error		-0.8	±0.4	+0.8	LSB
OFF	Offset Error		-2		+2	LSB
GAINERR	Gain Error		-2		+2	LSB

CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IBIAS	Bias sink current			30		uA

REFERENCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VREFP	Pos. Reference Voltage		1.8	2.4	2.8	V
VREFN	Neg. Reference Voltage		0.35	0.4	0.6	V
VREF	Difference between VRP and VRN	VREFP-VREFN	1.2	2	2.45	V
R_{ref}	Reference Impedance [1)]			380		Ohm
TKR_{ref}				1.2		mOhm/K

ANALOG INPUT

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vin	Input Voltage Range		VREFN		VREFP	V
R_{in}	Input Impedance		100			MOhms
C_{in}					5	pF

AC ACCURACY (VREFP=2.4V, VREFN=0.4V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	f_{in}=1MHz		-41.3		dB
THD	Total Harmonic Distortion	f_{in}=30MHz		-41.3		dB
SFDR	Spurious Free Dynamic Range	f_{in}=1MHz		46.2		dB
SFDR	Spurious Free Dynamic Range	f_{in}=30MHz		46.2		dB
SNR	Signal to Noise Ratio	f_{in}=1MHz		35.88		dB
SNR	Signal to Noise Ratio	f_{in}=30MHz		34.1		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=1MHz		34.8		dB
SINAD	Signal to (Noise+Dist.) Ratio	f_{in}=30MHz		33.3		dB
ENOB	Effective Number of Bits	f_{in}=1MHz		5.5		Bit
ENOB	Effective Number of Bits	f_{in}=30MHz		5.24		Bit

1) VREFP to VREFN

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Pos. digital Supply Voltage	VDD=VDDA	3.0	3.3	3.6	V
VSS	Neg. digital Supply Voltage	VSS=VSSA	0	0	0	V
VIL	Digital Input Level		VSS		0.3*VDD	V
VIH			0.7*VDD		VDD	V
VOL	Digital Output Level			VSS		V
VOH				VDD		V

POWER REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDA	Pos. analog Supply Voltage	VDD=VDDA	3.0	3.3	3.6	V
VSSA	Neg. analog Supply Voltage	VSS=VSSA	0	0	0	V
IDD [1) 3)]	Supply Current Digital			7.5	15	mA
IDDA [1) 3)]	Supply Current Analog			4	8	mA
Psup [1) 3)]	Supply Power Consumption Power Up Mode			38	82,8	mW
IREF [1) 3)]	Reference Current	incl. Ref.		5	10	mA
Pdiss_tot [1) 3)]	Total Power Consumption			54,5	118,8	mW
Pdiss_pd [2) 3)]	Total Power Consumption Power Down Mode			30	60	mW

TIMING CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
1/Tconv	Conversion Rate		0.1	80	100	MS/sec
fclk	Master CLOCK Frequency		0.1	80	100	MHz
Tdap	Aperture Delay			1.8		ns
Tconv	Total Conversion Time			1		clk cycle
Tpwhclk	CLOCK Pulse width High		5	6.5		nsec
Tpwlclk	CLOCK Pulse width Low		5	6.5		nsec
Jclk	CLOCK Jitter				$1*e^{-3}$/fin	sec
Tdcs	Delay Time CLOCK to STROBE			5.5		nsec
Tsuds	Setup Time DATA to STROBE			0.8		nsec
Tdp	Delay Time Pipeline			1		nsec
Twakeupall	Wake up Time all			50		nsec
Twakeup	Wake up Time			Twkupall - Tdap		nsec

1) Measured during a conversion with 100MHz clock frequency.

2) After 10µs power down.

3) The measurement includes 8 digital (8mA) output pads.

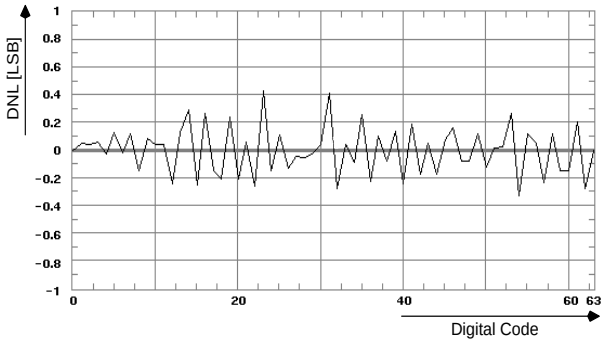
CODE TABLE

1LSB = (VREFP - VREFN) / 64.

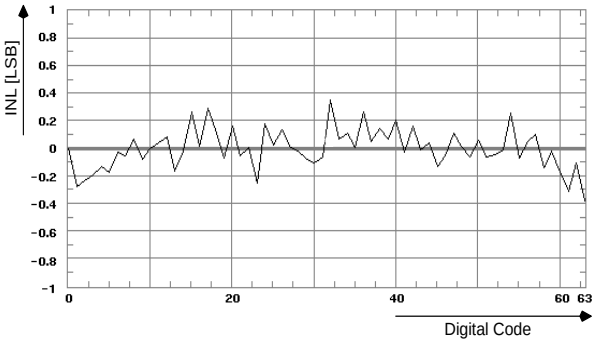
Output Code	Input Voltage: VIN-VINB
00 0000	VREFN…..0.5LSB
00 0001	0.5LSB…..1.5LSB
00 0010	1.5LSB…..2.5LSB
…	…
11 1111	62.5LSB…..VREFP

TYPICAL PERFORMANCE CHARACTERISTICS

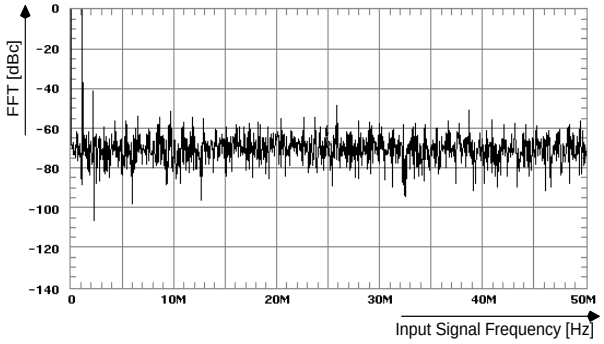
($T_{junction}$=25°C, VDDA=VDD=+3.3V, fclk=100MHz, VREFP=+2.4V and VREFN=0.4V, unless otherwise specified)



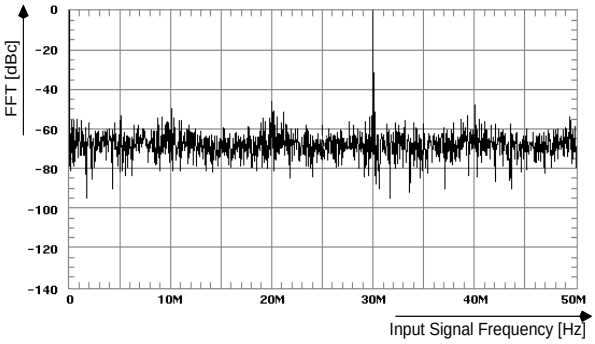
DNL



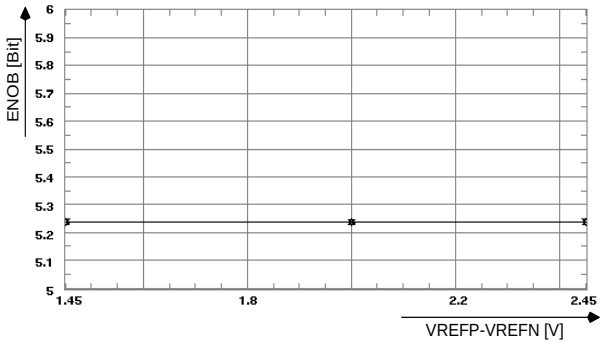
INL



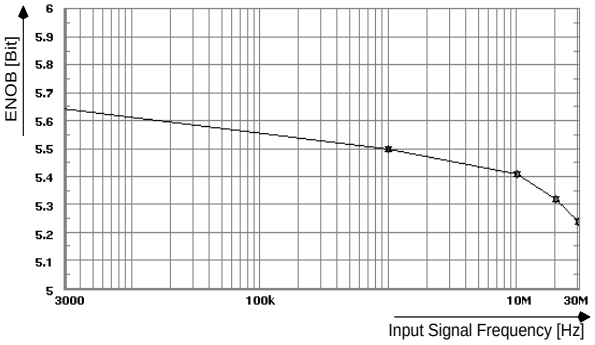
Spectrum @1MHz 1)



Spectrum @30MHz 1)



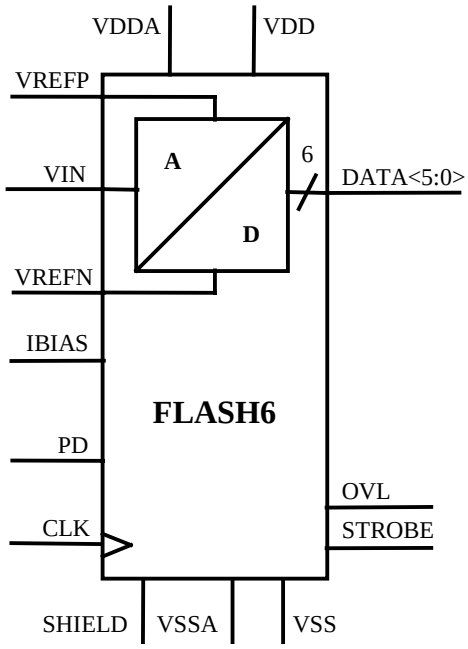
ENOB vs (VREFP-VREFN) @30MHz



ENOB vs Input Signal Frequency

1) The spectrum consists of 1024 pins

SYMBOL



PINLIST

Pin	Description	Typ	Cap
VIN	Input Voltage	AIN	5pF
VREFP	Pos. Reference Voltage	AIN	
VREFN	Neg. Reference Voltage	AIN	
IBIAS	Bias Current	AIN	
PD	Power down Signal	DIN	0.1pF
CLK	Master Clock	DIN	0.1pF
DATA<5:0>	Data Output (DATA<5>=MSB)	DOUT	
OVL	Overload	DOUT	
STROBE	Data Strobe Signal	DOUT	
VDDA	Pos. Analog Supply	S	
VSSA	Neg. Analog Supply	S	
SHIELD	Connect to VSSA	S	
VDD	Pos. Digital Supply	S	
VSS	Neg. Digital Supply	S	

THEORY OF OPERATION

The Macro Cell FLASH6 is a 6-bit single step parallel analog to digital converter. The architecture is based on a 380 Ohm polysilicon resistor reference ladder and static CMOS comparators. The thermometer code of the comparator outputs is encoded in a fast ROM encoder into straight binary code with CMOS logic signal levels. The last comparator output is connected unlatched to the OVL output. The area of the converter is small. The comparators do not need auto zeroing and therefore are fast and perform minimal kickback on the analog signal input. The conversion range is set by the reference inputs VREFP and VREFN. The output OVL indicates an overload condition when Vin > (VREFP - 0.5*LSB).

POWER SUPPLIES

The converter requires a single +3.3V power supply. The supplies for analog and digital are separated and may be connected together. However, for maximum noise immunity it is recommended to wire them on chip to separated pins, especially when the block is embedded in a large digital circuit. The supplies may then be connected together on PC-board level.
The proper use of blocking capacitors in the application is important

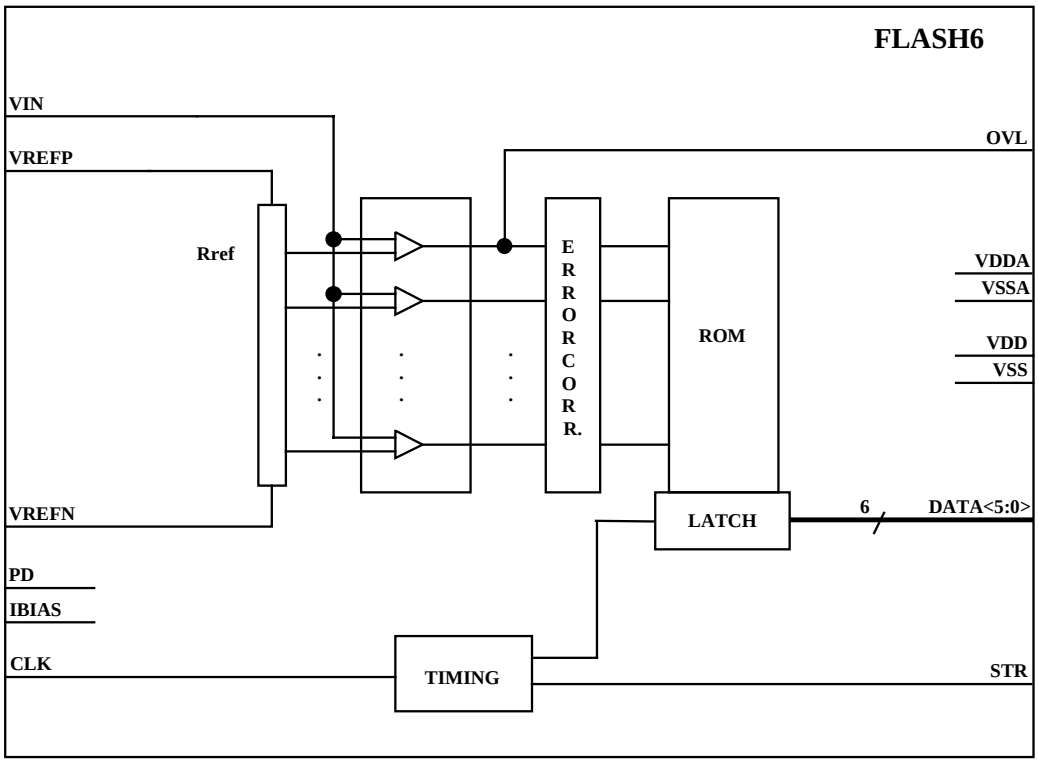
REFERENCE VOLTAGE

Both input pads VREFP and VREFN must have a 0 Ohm protection resistor. The ESD test was performed with ±1kV (Norm: MIL 883 E method 3015).
The proper use of blocking capacitors in the application is important !

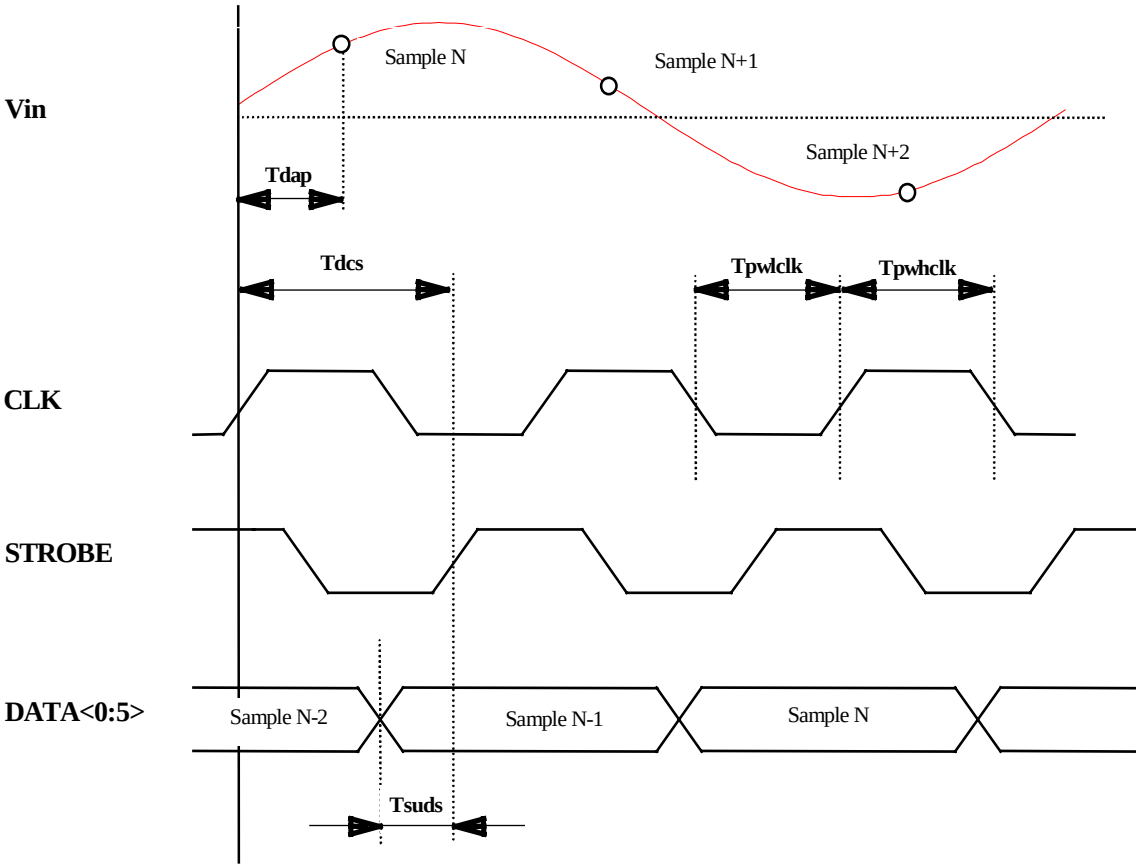
INPUT VOLTAGE

The input pad VIN must have a 0 Ohm protection resistor. The ESD test was performed with ±1kV (Norm: MIL 883 E method 3015).

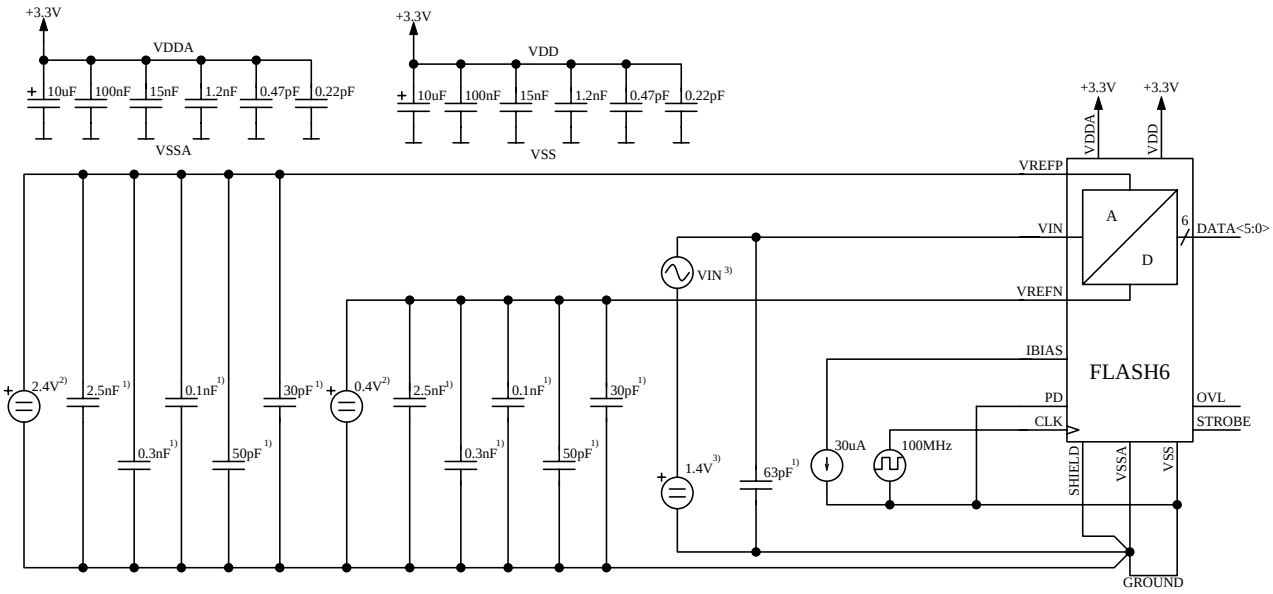
FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM OF FLASH6



TYPICAL APPLICATION



Configuration: Continuous Conversion at 100MS/sec

1) The value of the capacitor depends on the input frequency.
For SMD capacitors use the type NPO and for normal capacitors use the type MKT for best performance.

2) The accuracy for both reference voltages must be higher than the resolution of the ADC. In the typical application both voltages are filtered by a second order low pass filter (f_c=5Hz) and buffered with an AD711.

3) The accuracy for the input voltage must be higher than the resolution of the ADC. In the typical application the input voltage is filtered by a seven order low pass filter (f_c=32MHz) and buffered with a THS3001.

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