intersil

EL5123, EL5223, EL5323, EL5423

Data Sheet | March 20, 2002 | FN7176

12MHz 4, 8, 10 & 12 Channel Rail-to-Rail Input-Output Buffers

élantec

The EL5123, EL5223, EL5323, and EL5423 are low power, high voltage rail-to-rail input/output buffers designed primarily for use in reference voltage buffering applications for TFT_LCDs. They are available in quad (EL5123), octal (EL5223), 10-channel (EL5323), and 12-channel (EL5423) topologies. All buffers feature a -3dB bandwidth of 12MHz and operate from just 600µA per buffer. This family also features fast slewing and settling times, as well as a continuous output drive capability of 30mA (sink and source).

The quad channel EL5123 is available in the 10-pin MSOP package. The 8-channel EL5223 is available in both the 20-pin TSSOP and 24-pin LPP packages, the 10-channel EL5323 in the 24-pin TSSOP and 24-pin LPP packages, and the 12-channel EL5423 in the 28-pin TSSOP and 32-pin LPP packages. All buffers are specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NO	PACKAGE	TAPE & REEL	PKG. NO.
EL5123CY	10-Pin MSOP	-	MDP0043
EL5123CY-T7	10-Pin MSOP	7”	MDP0043
EL5123CY-T13	10-Pin MSOP	13”	MDP0043
EL5223CL	24-Pin LPP	-	MDP0046
EL5223CL-T7	24-Pin LPP	7”	MDP0046
EL5223CL-T13	24-Pin LPP	13”	MDP0046
EL5223CR	20-Pin TSSOP	-	MDP0044
EL5223CR-T7	20-Pin TSSOP	7”	MDP0044
EL5223CR-T13	20-Pin TSSOP	13”	MDP0044
EL5323CL	24-Pin LPP	-	MDP0046
EL5323CL-T7	24-Pin LPP	7”	MDP0046
EL5323CL-T13	24-Pin LPP	13”	MDP0046
EL5323CR	24-Pin TSSOP	-	MDP0044
EL5323CR-T7	24-Pin TSSOP	7”	MDP0044
EL5323CR-T13	24-Pin TSSOP	13”	MDP0044
EL5423CL	32-Pin LPP	-	MDP0046
EL5423CL-T7	32-Pin LPP	7”	MDP0046
EL5423CL-T13	32-Pin LPP	13”	MDP0046
EL5423CR	28-Pin TSSOP	-	MDP0044
EL5423CR-T7	28-Pin TSSOP	7”	MDP0044
EL5423CR-T13	28-Pin TSSOP	13”	MDP0044

Features

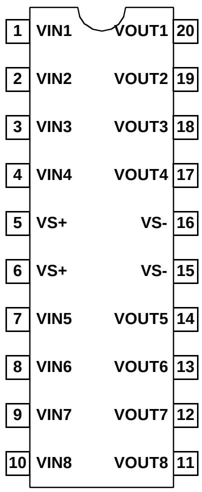
- 12MHz -3dB bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per buffer) = 600µA
- High slew rate = 15V/µs
- Rail-to-rail input/output swing
- Ultra-small packages

Applications

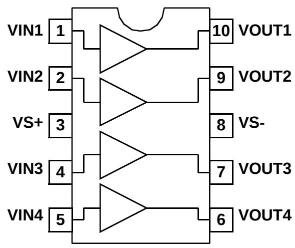
- TFT-LCD drive circuits
- Electronics notebooks
- Electronic games
- Touch-screen displays
- Personal communication devices
- Personal digital assistants (PDA)
- Portable instrumentation
- Sampling ADC amplifiers
- Wireless LANs
- Office automation
- Active filters
- ADC/DAC buffers

Pinouts

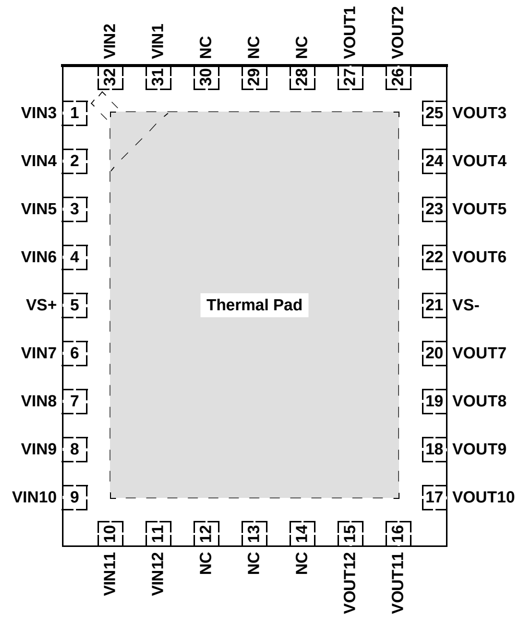
EL5223
(20-PIN TSSOP)
TOP VIEW



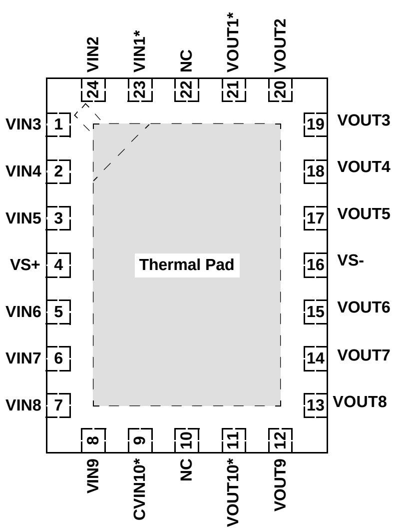
EL5123
(10-PIN MSOP)
TOP VIEW



EL5423
(32-PIN LPP)
TOP VIEW

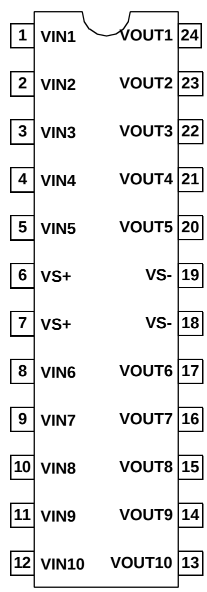


EL5223 & EL5323
(24-PIN LPP)
TOP VIEW

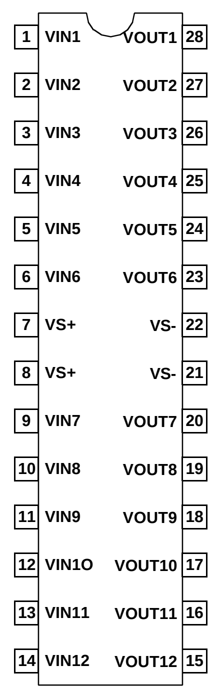


*** Not available in EL5223**

EL5323
(24-PIN TSSOP)
TOP VIEW



EL5423
(28-PIN TSSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- . . . .+18V
Input Voltage . . . .V_S- -0.5V, V_S +0.5V
Maximum Continuous Output Current 30mA
Maximum Die Temperature . . . .+125°C
Storage Temperature. . . . .-65°C to +150°C
Operating Temperature . . . .-40°C to +85°C
Power Dissipation . . . . See Curves
ESD Voltage 2kV

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 10kΩ and C_L = 10pF to 0V, T_A = 25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		0.5	12	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	-4.5V ≤ V_{OUT} ≤ 4.5V	0.99		1.01	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.95	-4.85	V
V_{OH}	Output Swing High	I_L = +5mA	4.85	4.95		V
I_{OUT} (max)	Output Current (Note 2)	R_L = 10Ω		±120		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	55	80		dB
I_S	Supply Current	No load (EL5123)		2.4	3.4	mA
		No load (EL5223)		5.5	6.8	mA
		No load (EL5323)		6	8.5	mA
		No load (EL5423)		7.45	10.1	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	-4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%	7	15		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		250		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

1. Measured over operating temperature range.
2. Instantaneous peak current.
3. Slew rate is measured on rising and falling edges.

Electrical Specifications

$V_S+ = +5V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 2.5V, $T_A = 25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		0.5	12	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	$0.5V \le V_{OUT} \le 4.5V$	0.99		1.01	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -2.5mA$		80	150	mV
V_{OH}	Output Swing High	$I_L = +2.5mA$	4.85	4.92		V
I_{OUT} (max)	Output Current (Note 2)	$R_L = 10\Omega$		±120		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	55	80		dB
I_S	Supply Current	No load (EL5123)		2.4	3.2	mA
		No load (EL5223)		5.2	6.5	mA
		No load (EL5323)		5.8	8	mA
		No load (EL5423)		7.2	9.7	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$1V \le V_{OUT} \le 4V$, 20% to 80%		12		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		250		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

1. Measured over operating temperature range.
2. Instantaneous peak current.
3. Slew rate is measured on rising and falling edges

Electrical Specifications

$V_S+ = +15V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 7.5V, $T_A = 25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 7.5V$		0.5	14	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	$V_{CM} = 7.5V$		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	$0.5V \le V_{OUT} \le 14.5V$	0.99		1.01	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -7.5mA$		80	150	mV
V_{OH}	Output Swing High	$I_L = +7.5mA$	14.85	14.95		V
I_{OUT} (max)	Output Current (Note 2)	$R_L = 10\Omega$	120	200		mA

Electrical Specifications

$V_S+ = +15V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 7.5V, $T_A = 25°C$ unless otherwise specified.

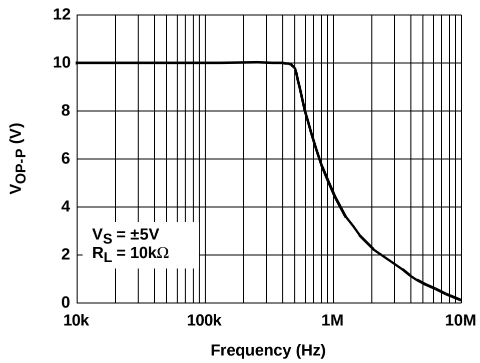
PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	55	80		dB
I_S	Supply Current	No load (EL5123)		2.4	3.7	mA
		No load (EL5223)		5.7	7.1	mA
		No load (EL5323)		6.2	8.7	mA
		No load (EL5423)		7.8	10.4	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$1V \le V_{OUT} \le 14V$, 20% to 80%		18		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		250		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

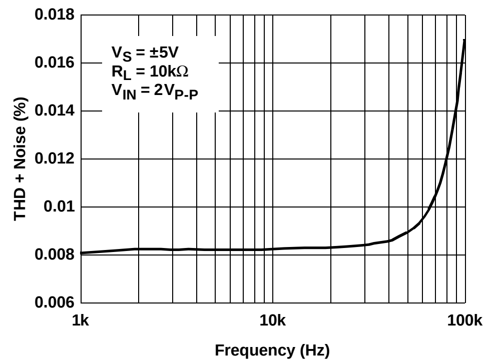
1. Measured over operating temperature range.
2. Instantaneous peak current.
3. Slew rate is measured on rising and falling edges.

Typical Performance Curves

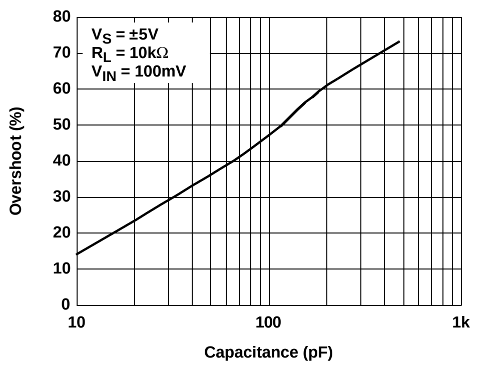
Output Swing vs Frequency



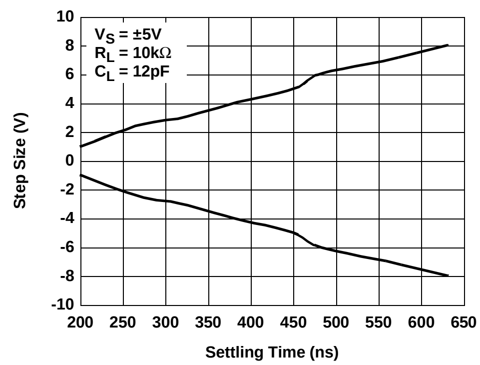
Total Harmonic Distortion + Noise vs Frequency



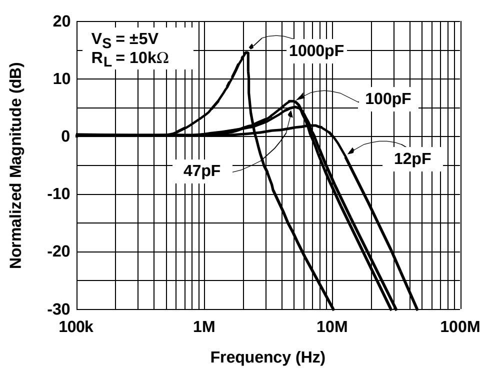
Overshoot vs Load Capacitance



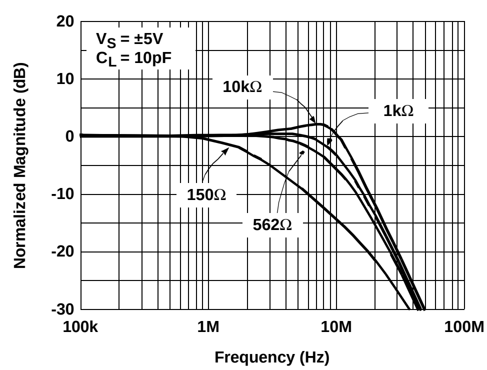
Settling Time vs Step Size



Frequency Response for Various C_L

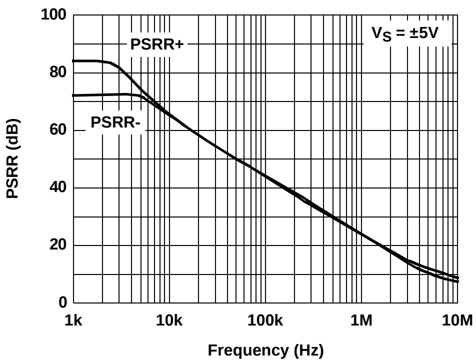


Frequency Response for Various R_L

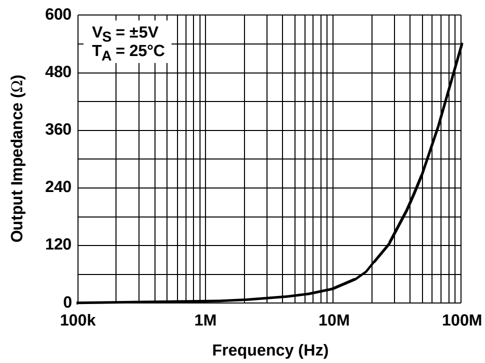


Typical Performance Curves (Continued)

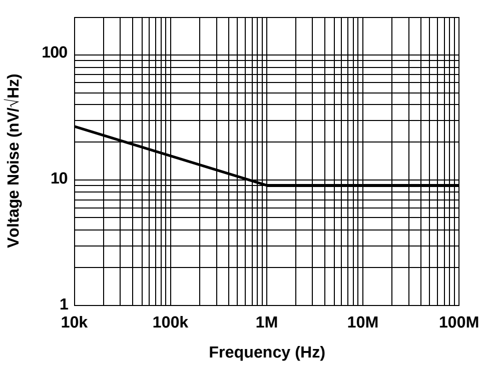
PSRR vs Frequency



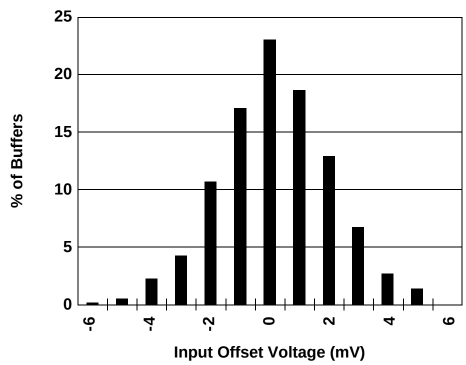
Output Impedance vs Frequency



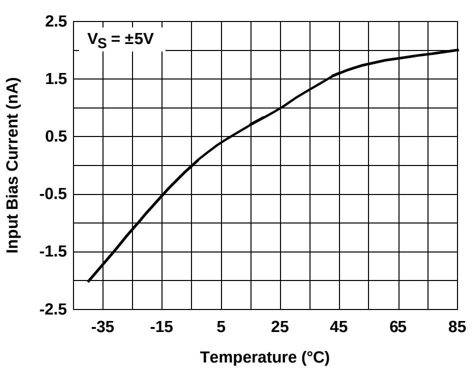
Input Noise Special Density vs Frequency



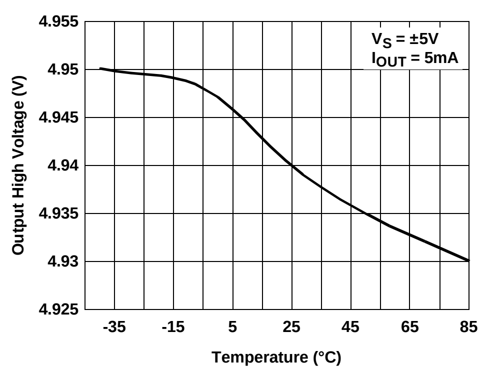
Input Offset Voltage Distribution



Input Bias Current vs Temperature

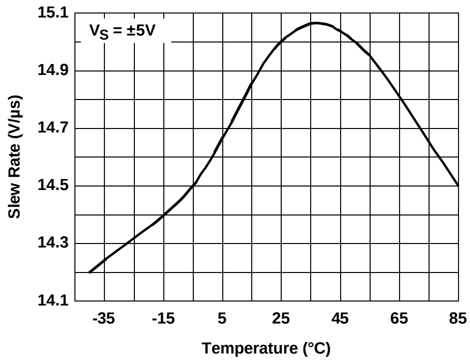


Output High Voltage vs Temperature

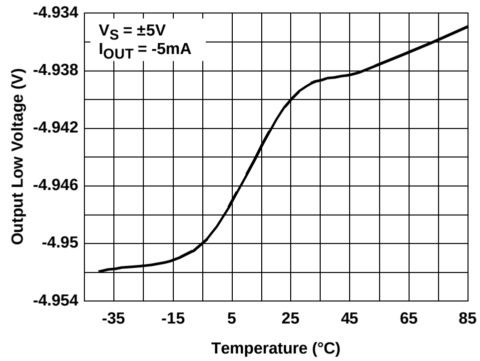


Typical Performance Curves (Continued)

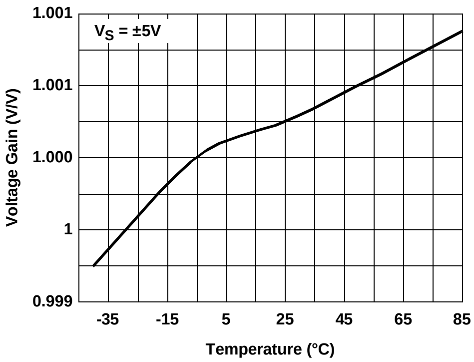
Slew Rate vs Temperature



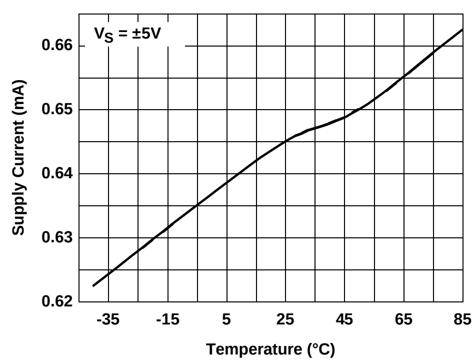
Output Low Voltage vs Temperature



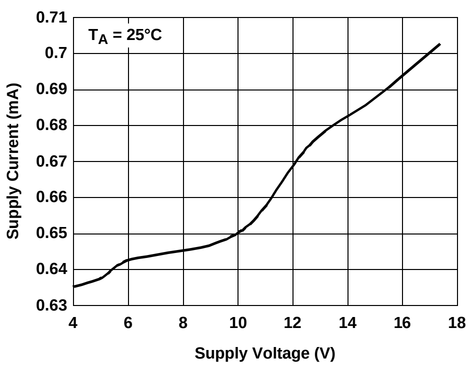
Voltage Gain vs Temperature



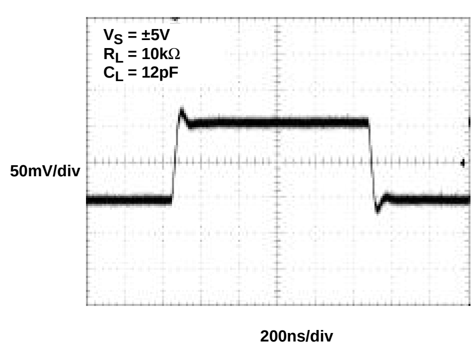
Supply Current per Channel vs Temperature



Supply Current per Channel vs Supply Voltage

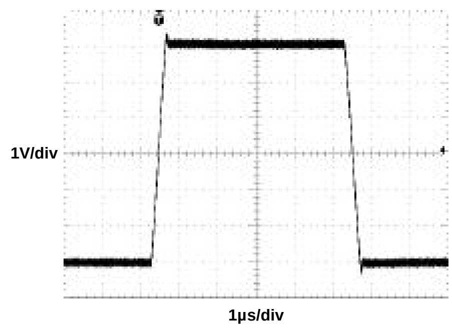


Small Signal Transient Response

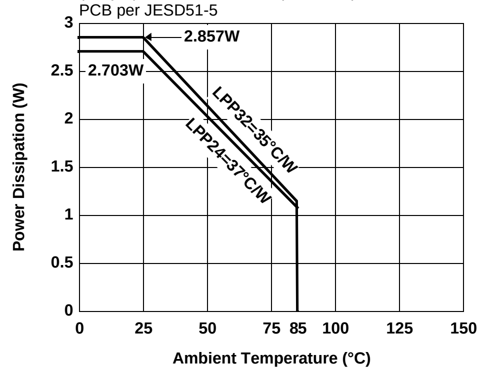


Typical Performance Curves (Continued)

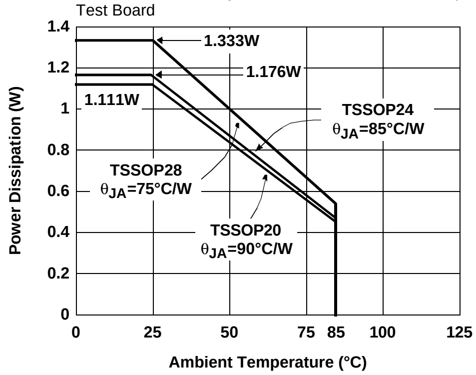
Large Signal Transient Response



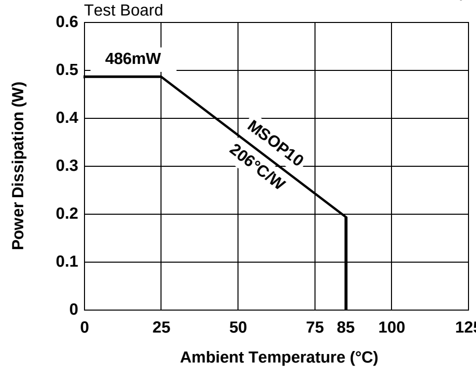
Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-7 High Effective Thermal Conductivity (4-layer) Test Board, LPP exposed diepad soldered to PCB per JESD51-5



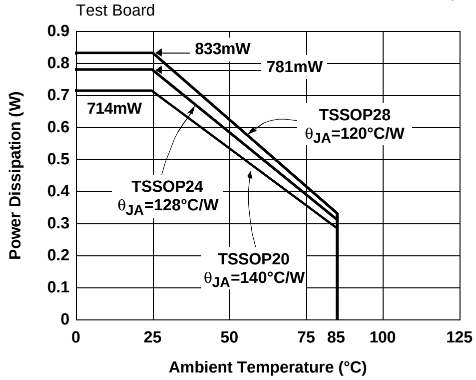
Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-7 High Effective Thermal Conductivity Test Board



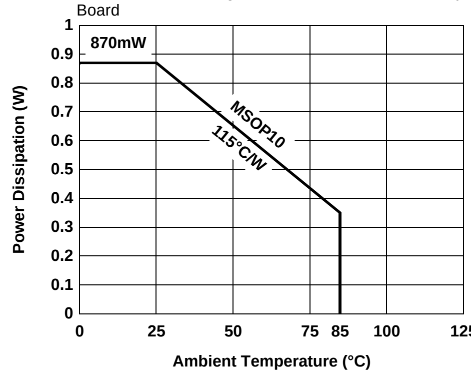
Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-3 Low Effective Thermal Conductivity Test Board



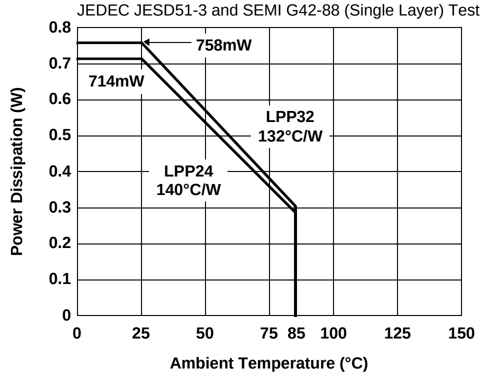
Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-3 Low Effective Thermal Conductivity Test Board



Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-7 High Effective Thermal Conductivity Test Board



Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-3 and SEMI G42-88 (Single Layer) Test Board



Applications Information

Product Description

The EL5123, EL5223, EL5323, and EL5423 unity gain buffers are fabricated using a high voltage CMOS process. It exhibits rail-to-rail input and output capability and has low power consumption (600µA per buffer). These features make the EL5123, EL5223, EL5323, and EL5423 ideal for a wide range of general-purpose applications. When driving a load of 10kΩ and 12pF, the EL5123, EL5223, EL5323, and EL5423 have a -3dB bandwidth of 12MHz and exhibits 15V/µs slew rate.

Operating Voltage, Input, and Output

The EL5123, EL5223, EL5323, and EL5423 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5123, EL5223, EL5323, and EL5423 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The output swings of the EL5123, EL5223, EL5323, and EL5423 typically extend to within 50mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 1 shows the input and output waveforms for the device. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.985V_{P-P}$.

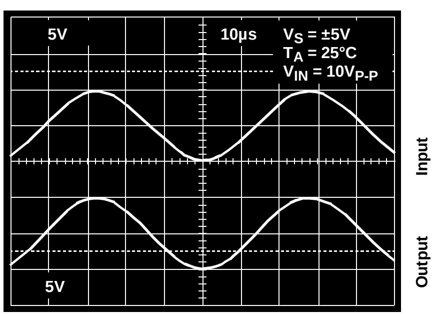


FIGURE 1. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5123, EL5223, EL5323, and EL5423 will limit the short circuit current to ±120mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±30mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5123, EL5223, EL5323, and EL5423 are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 2 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

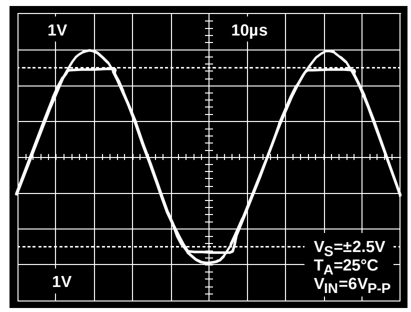


FIGURE 2. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5123, EL5223, EL5323, and EL5423 buffer, it is possible to exceed the 125°C "absolute-maximum junction temperature" under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{d\Theta_{JA}}$$

where:

T_{JMAX} = Maximum junction temperature

T_{AMAX}= Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S -) \times I_{LOAD}i]$$

when sinking.

where:

i = 1 to Total number of buffers

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent current per channel

$V_{OUT}i$ = Maximum output voltage of the application

$I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves.

Unused Buffers

It is recommended that any unused buffer have the input tied to the ground plane.

Driving Capacitive Loads

The EL5123, EL5223, EL5323, and EL5423 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The buffers drive 10pF loads in parallel with 10kΩ with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a “snubber” circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ pin to ground. A 4.7µF tantalum capacitor should then be connected from V_S+ pin to ground. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.