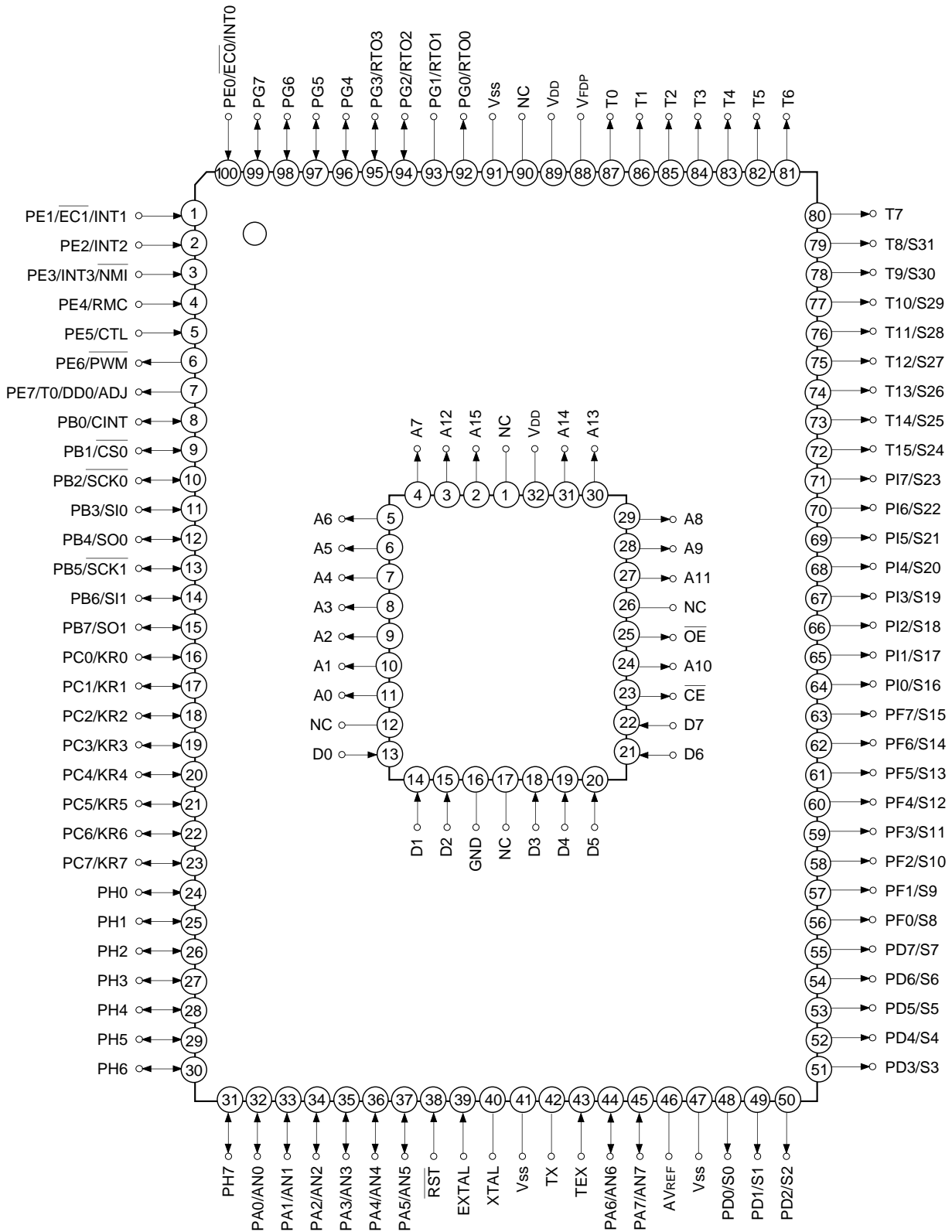
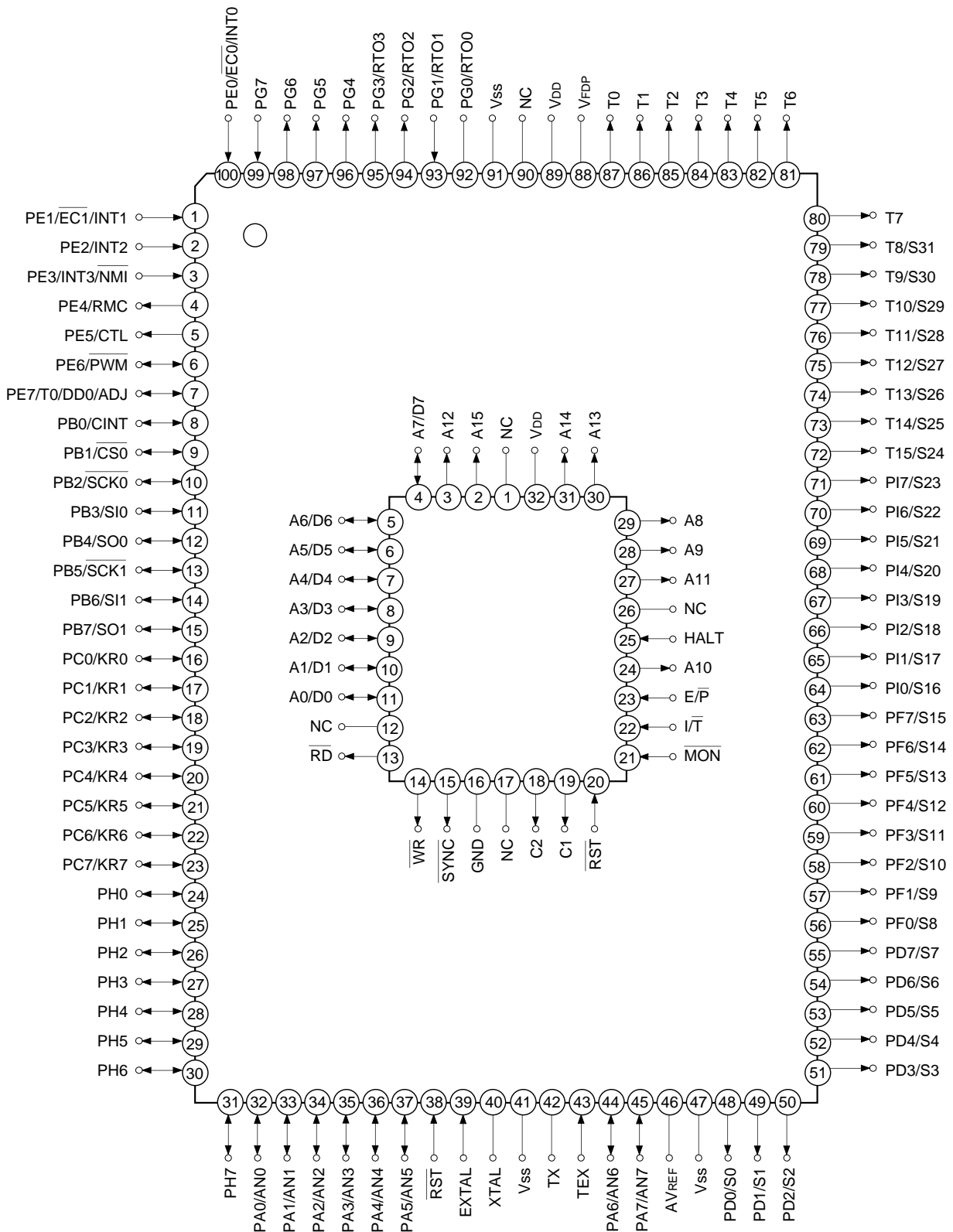


Pin Assignment in Piggyback Mode



- Note)**
1. NC (Pin 90) is always connected to V_{DD}.
 2. V_{ss} (Pins 41 and 91) are both connected to GND.

Pin Assignment in Evaluator Mode

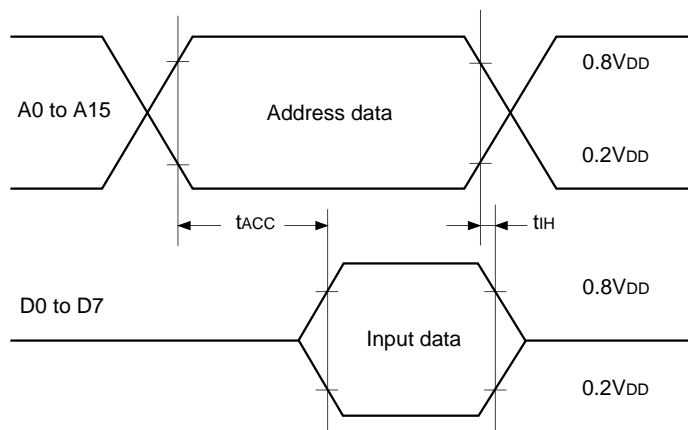


- Note)**
1. NC (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 91) are both connected to GND.

EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{cc} = 4.5$ to 5.5V , $V_{ss} = 0\text{V}$ reference)

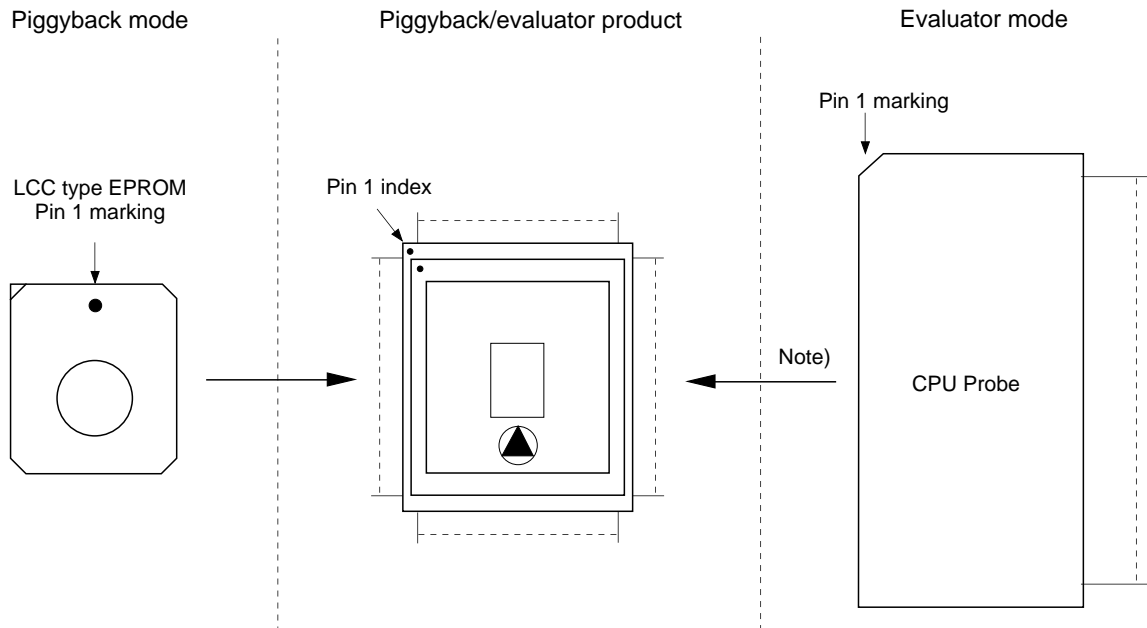
Item	Symbol	Pins	Min.	Max.	Unit
Address → Data Input delay time	t_{ACC}	A0 to A15 D0 to D7		120	ns
Address → Data Hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Products List

Option item	Products		
	Mask		Piggyback/evaluator
	CXP82220	CXP82224	CXP82200-U01Q
Package	100-pin plastic QFP		100-pin ceramic PQFP
ROM capacitance	20K bytes	24K bytes	EPROM 24K bytes
Pull-up resistance for reset pin	Existent/Non-existent		Existent
Power-on reset circuit	Non-existent		Non-existent
Pull-down resistance for high voltage drive pin	Existent/Non-existent		Only port for display

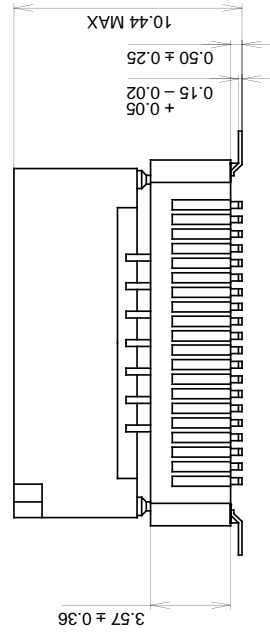
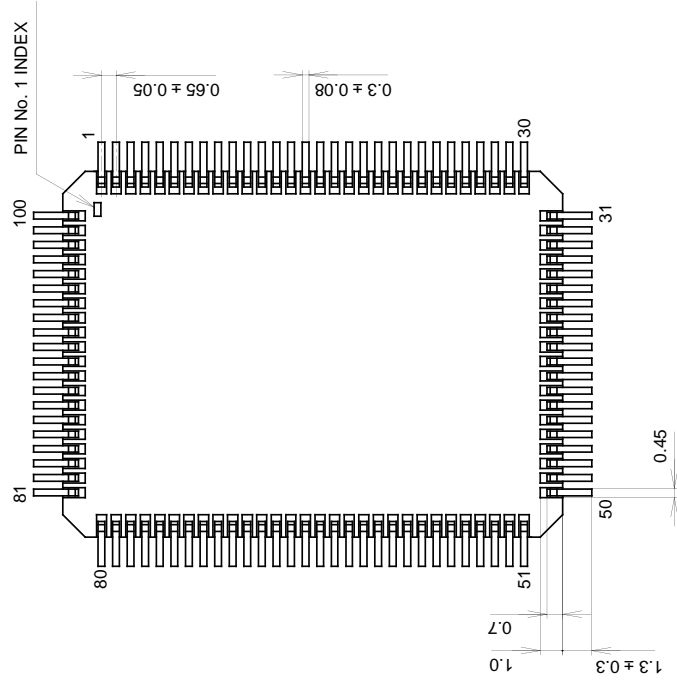
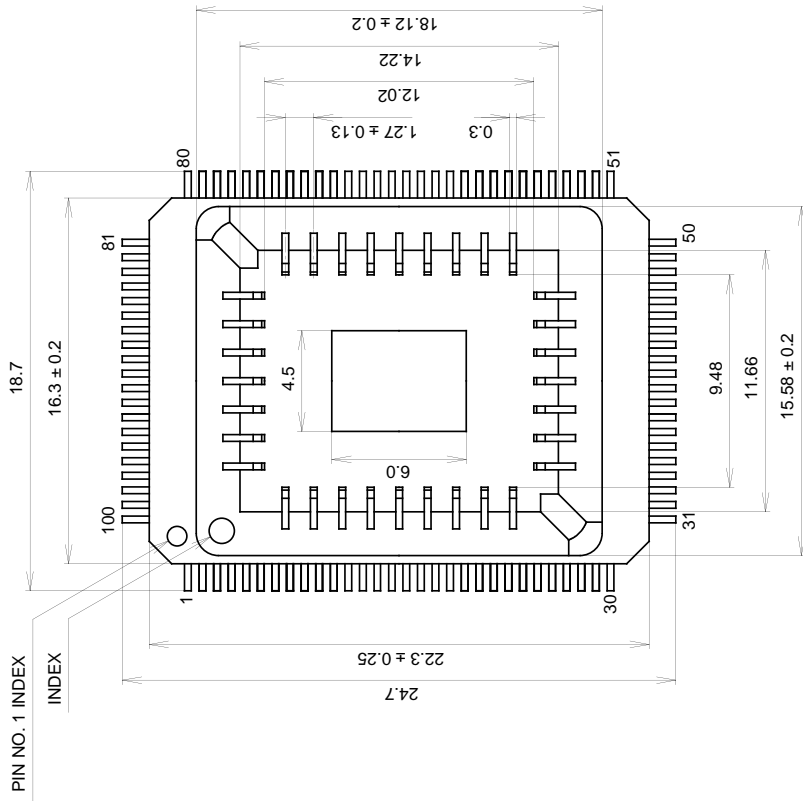
Piggyback mode/evaluator mode can be switched as shown below.



Note) Evaluation cap should be connected to CPU probe.

Package Outline Unit: mm

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

SONY CODE	PQFP-100C-L01
EIAJ CODE	AGFP100-C-0000-A
JEDEC CODE	