

Reference Voltage and Driver IC for LCD

Description

The CXD2475TQ is suitable IC for applying reference voltage for gamma correction which is necessary for TFT liquid crystal display. This IC has a built-in 9 channels of rail-to-rail buffer circuit which enables 2-input switch and a common driver circuit.

Features

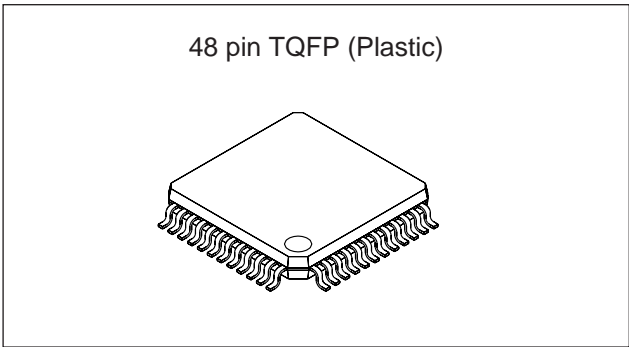
- Built-in 9 channels of rail-to-rail buffer circuit
- Built-in common driver circuit
- Current consumption: 3.6mA (typ.)
- Package: 48pin TQFP

Structure

Bi-CMOS IC

Applications

Small liquid crystal monitor



Absolute Maximum Ratings (Ta = 25°C)

- | | | | |
|---|-------|-------------|-------|
| • Supply voltage | Vcc*1 | 7.0 | V |
| | VvG*2 | 7.0 | V |
| | VvC*3 | ≤ Vcc + 0.2 | V |
| | VvG*4 | ≥ GND - 0.2 | V |
| • Operating temperature | Topr | -25 to +85 | °C |
| • Storage temperature | Tstg | -55 to +150 | °C |
| • Allowable power dissipation (Ta ≤ 25°C) | Pd | 1.72 | W |
| • Reduced ratio (Ta < 25°C) | | 13.8 | mW/°C |

Operating Conditions

- | | | | |
|------------------|-------|-------------------|---|
| • Supply voltage | Vcc*1 | 4.5 to 5.0 to 5.5 | V |
| | VvG*2 | 4.0 to Vcc | V |
| | VvC*3 | 4.0 to Vcc | V |
| | VvG*4 | 0 to 1.0 | V |

*1 Applied to Vcc – GND.

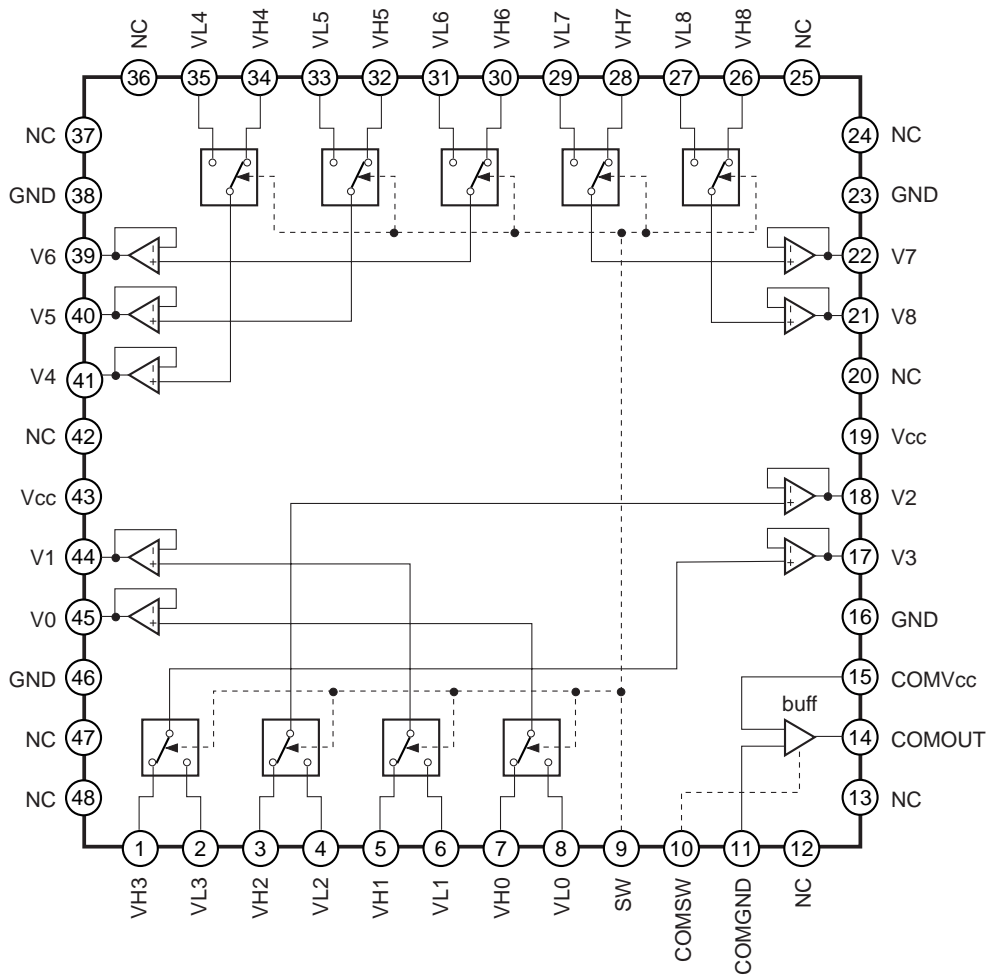
*2 Applied to COMVcc – COMGND

*3 Applied to COMVcc – GND

*4 Applied to COMGND – GND

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Block Diagram



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description		
1	VH3	0.2 to 4.8V		DC input when SW is high.		
2	VL3			DC input when SW is low.		
3	VH2			DC input when SW is high.		
4	VL2			DC input when SW is low.		
5	VH1			DC input when SW is high.		
6	VL1			DC input when SW is low.		
7	VH0			DC input when SW is high.		
8	VL0			DC input when SW is low.		
26	VH8			DC input when SW is high.		
27	VL8			DC input when SW is low.		
28	VH7			DC input when SW is high.		
29	VL7			DC input when SW is low.		
30	VH6			DC input when SW is high.		
31	VL6			DC input when SW is low.		
32	VH5			DC input when SW is high.		
33	VL5			DC input when SW is low.		
34	VH4			DC input when SW is high.		
35	VL4			DC input when SW is low.		
17	V3			0.2 to 4.8V		V3 output.
18	V2					V2 output.
21	V8	V8 output.				
22	V7	V7 output.				
39	V6	V6 output.				
40	V5	V5 output.				
41	V4	V4 output.				
44	V1	V1 output.				
45	V0	V0 output.				
9	SW			Input switch. VL is output for low; VH for high.		
10	COMSW			COM output switch. COMVcc level is output for low; COMGND level for high.		

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	COMGND	0 to 1.0V		COM output ground.
14	COMOUT			COM output.
15	COMVcc	4.0 to Vcc		COM power supply.
19	Vcc	5.0V		5V power supply.
43	Vcc	5.0V		5V power supply.
16	GND			GND.
23	GND			GND.
38	GND			GND.
46	GND			GND.
12	NC			No connected.
13	NC			No connected.
20	NC			No connected.
24	NC			No connected.
25	NC			No connected.
36	NC			No connected.
37	NC			No connected.
42	NC			No connected.
47	NC			No connected.
48	NC			No connected.

Note)

- GND
Make sure that Pins 16, 23, 38 and 46 are connected to GND potential, and do not release them.
- Decoupling capacitor
Locate decoupling capacitor connected between power supply and GND as near IC pin as possible.
- Design VH and VL input pins not to have capacity.

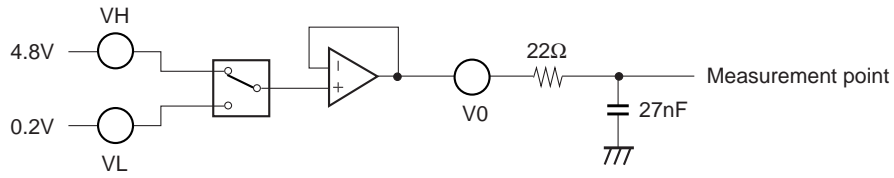
Electrical Characteristics

(Ta = 25°C, Vcc = COMVcc = 5V, COMGND = 0V)

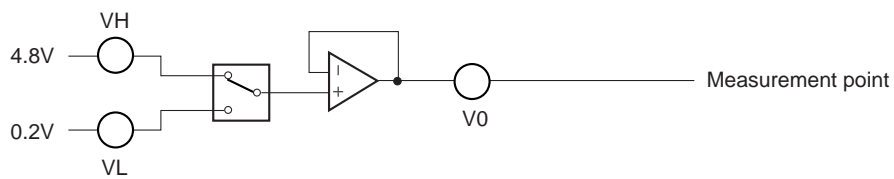
No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Current consumption (Vcc + COMVcc)	ICC	Input voltage = 2.5V	—	3.6	6.0	mA
2	VH, VL input current high	I _{IH}	Input voltage = 4.8V	-0.1	—	0.1	μA
3	VH, VL input current low	I _{IL}	Input voltage = 0.2V	-0.1	—	0.1	μA
4	SW, COMSW input current high	I _{ISH}	Input voltage = 5V	-0.1	—	0.1	μA
5	SW, COMSW input current low	I _{ISL}	Input voltage = 0V	-0.4	—	0.1	μA
6	VREF voltage gain	A _V	Input voltage = 0.2 to 4.8V	0.985	—	—	V/V
7	VREF output voltage high	V _{OH}	I _{SOURCE} = 10mA	Vcc - 0.2	—	—	V
8	VREF output voltage low	V _{OL}	I _{SINK} = 10mA	—	—	0.2	V
9	COMOUT output voltage high	V _{COH}	I _{SOURCE} = 10mA	COMVcc - 0.1	—	—	V
10	COMOUT output voltage low	V _{COL}	I _{SINK} = 10mA	—	—	COMGND + 0.1	V
11	VREF offset voltage	V _{OFF}		—	—	20	mV
12	VREF load regulation	ΔV _O	Input voltage = 0.2 to 4.8V I _{SOURCE} = 10mA I _{SINK} = 10mA	—	±5	±10	mV
13	SW, COMSW input voltage high	V _{IH}		2	—	—	V
14	SW, COMSW input voltage low	V _{IL}		—	—	0.8	V
15	VREF transient time (1)	t _{tvLH1}	Measurement circuit 1	—	5	8	μs
		t _{tvHL1}					
16	VREF transient time (2)	t _{tvLH2}	Measurement circuit 2	—	3.5	6	μs
		t _{tvHL2}					
17	VREF propagation delay time (1)	t _{tpvLH1}	Measurement circuit 1	—	3.5	6	μs
		t _{tpvHL1}					
18	VREF propagation delay time (2)	t _{tpvLH2}	Measurement circuit 2	—	2.5	5	μs
		t _{tpvHL2}					
19	VREF propagation delay time difference (1)	Δt _{pv1}	t _{tpvLH1} - t _{tpvHL1}	—	—	±1.6	μs
20	VREF propagation delay time difference (2)	Δt _{pv2}	t _{tpvLH2} - t _{tpvHL2}	—	—	±0.8	μs
21	COM transient time	t _{ttcLH}	Measurement circuit 3	—	3	5	μs
		t _{ttcHL}					
22	COM propagation delay time	t _{tpcLH}	Measurement circuit 3	—	1.6	3	μs
		t _{tpcHL}					
23	COM propagation delay time difference	Δt _{pc}	t _{tpcLH} - t _{tpcHL}	—	—	±1	μs

Measurement Circuits

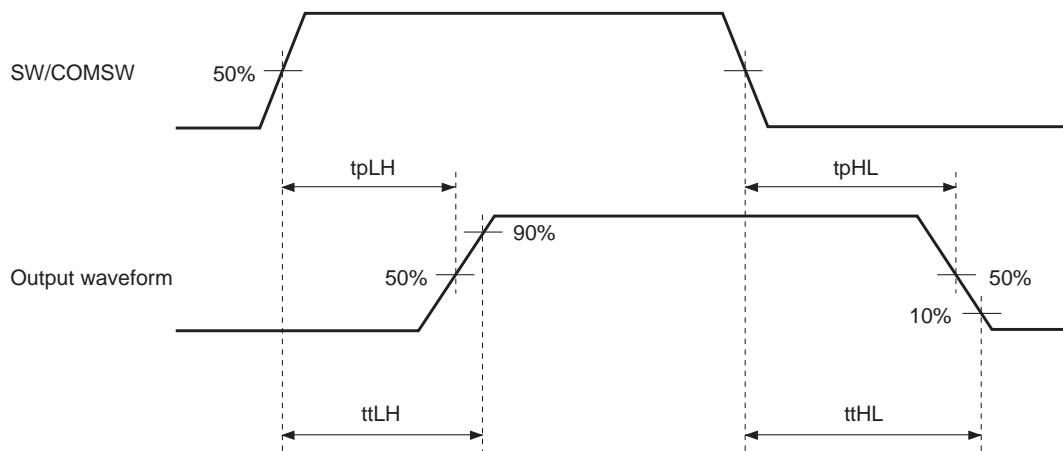
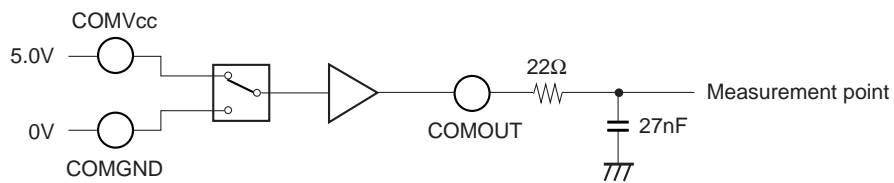
Measurement circuit 1



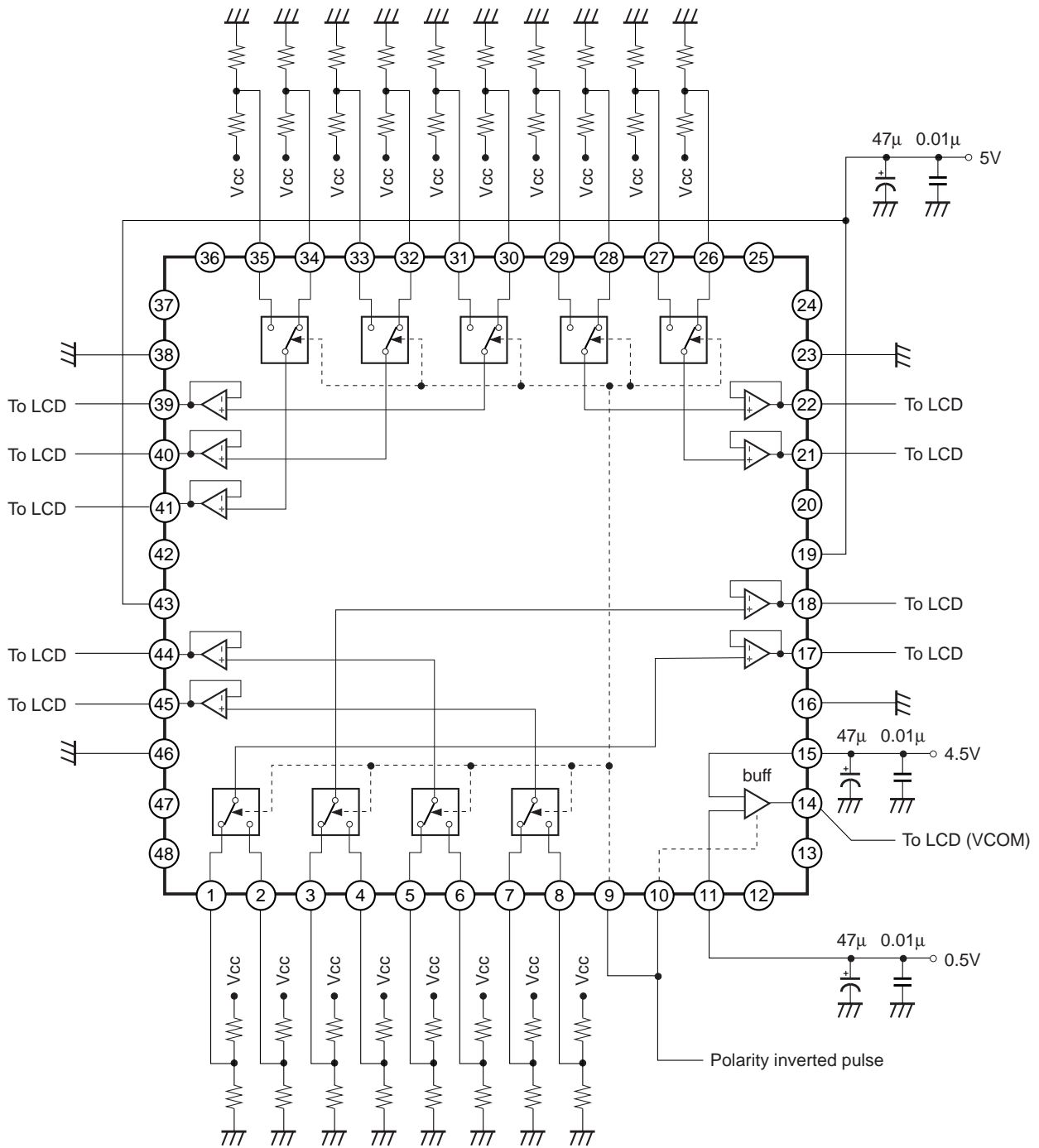
Measurement circuit 2



Measurement circuit 3



Application Circuit

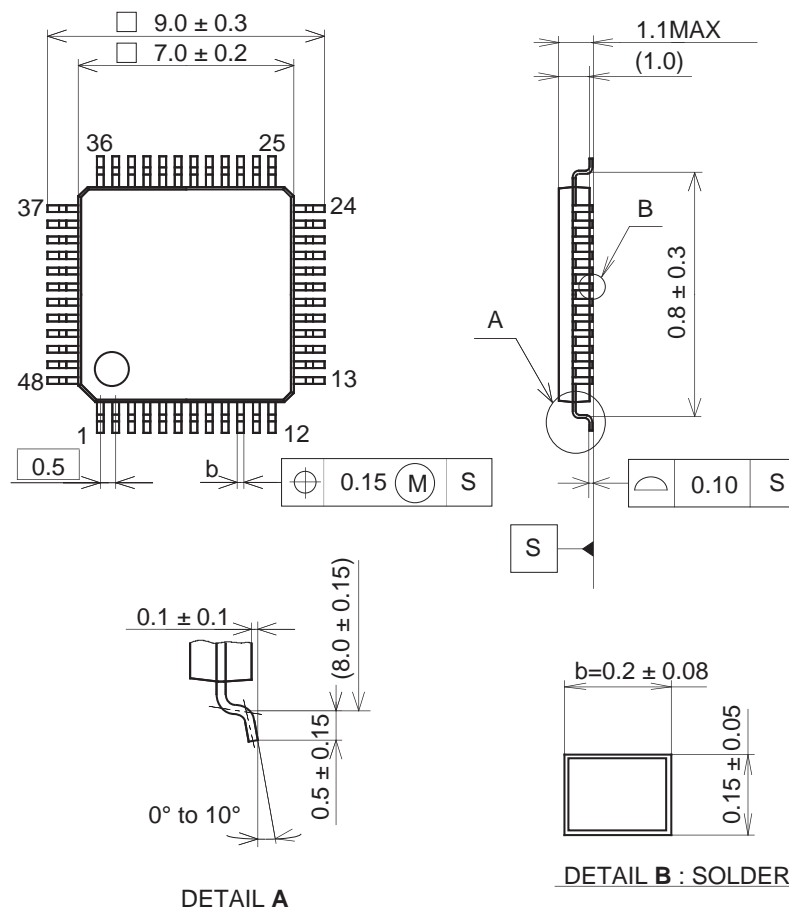


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit: mm

48PIN TQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	TQFP-48P-L111
EIAJ CODE	P-TQFP48-7x7-0.5
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.14g