

GENERAL DESCRIPTION

API820G is a tiny-controller-based voice synthesizer IC which contains all the function of API820G series and has an OTP (One Time Programmable) ROM inside.

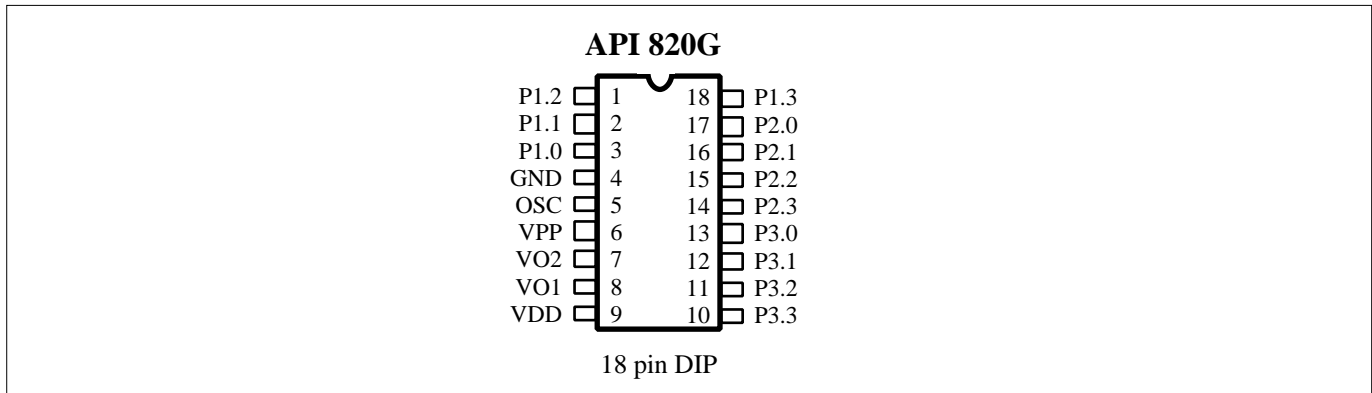
FEATURES

- API820G – ROM : 64k x 10 bits (21 sec@6K sample rate).
- Single power supply 2.4V ~ 5.5V.
- Port1 and Port2 with wake-up function.
- Power down mode for saving power consumption.
- Single ROM for voice and program data.
- Readable ROM code data.
- One 6-bit timer overflow control.
- Two stacks for subroutine calling.
- Fixed current D/A to drive external connected transistor for audio output.
- Multiple playing speeds in 2KHz ~ 32KHz for voice playback.
- 5-bit ASPCM synthesizer.
- Multiple levels of volume control.
- Multiple playing speeds in 2KHz ~ 32KHz for voice playback.

PIN DESCRIPTIONS

Pin NO.	I/O	Symbol	Function
1	I	P1.2/OEB/Mode option	Bit 2 of Port 1 / Program control signal
2	I	P1.1/PGMB/Mode option	Bit 1 of Port 1 / Program control signal
3	I	P1.0	Bit 0 of Port 1
4	I	VSS	Negative power supply.
5	I	OSC/ACLK	Oscillation component connection pin / Program control signal
6	I	TEST/Vpp	Test/Programing.
7	O	VO2	Voice output.
8		VO1	No connect
9	I	VDD	Positive power supply.
10	I/O	P3.3	Bit 3 of Port 3.
11	I/O	P3.2	Bit 2 of Port 3.
12	I/O	P3.1	Bit 1 of Port 3.
13	I/O	P3.0	Bit 0 of Port 3.
14	I/O	P2.3	Bit 3 of Port 2.
15	I/O	P2.2	Bit 2 of Port 2.
16	I/O	P2.1/Dout	Bit 1 of Port 2 / Program data output signal
17	I/O	P2.0/Din	Bit 0 of Port 2 / Program data input signal
18	I/O	P1.3/Din.out.clk/Mode option	Bit 3 of Port 1 / Program control signal

PIN ASSIGNMENT



PROGRAMMING MODE

Mode	P13	P12	P11
Regular	0	0	0
Security	0	0	1

TIMING PARAMETER

Symbol	Parameter	Min.	Max.	Unit
Trs	Level set up time	2		us
Tmcs	Mode code setup time	2		us
Tdsu	Data set up time	100		ns
Tdsh	Data hold time	100		ns
Tas	ACLK to byte select time	2		us
Tacpw	Address clock pulse width	2		us
Tppw	Program pulse width	100		us
Tps	Programming mode set up time	4		us
Toed	Output enable setup time	300		ns

Note : Segment ROM S1, S0 is programed just while 5 LSBs of ADDR are all 0.

Programming for security mode :

When programming in security mode, the waveform is just like above. The programming data is as below :

B11 ~ B1	B0
User defined	Security bit

Note : When security = 0, enable security;
When security = 1, disable security.

DC PROGRAMMING CHARACTERISTICS ($V_{DD} = 5V \pm 0.5v$, $V_{PP} = 12.5V \pm 0.5v$)

Items	Sym.	Min.	Max.	Unit	Test Conditions
Input high voltage	V_{IH}	2.2	$V_{DD}+1.0$	V	
Input low voltage	V_{IL}	-0.3	0.8	V	
Input current	I_{IN}	-	10	μA	$V_{DD}=5V$, $V_{IN}=0 \sim V_{DD}$
Output high voltage	V_{OH}	2.4	-	V	$I_{OH}=400\mu A$
Output low voltage	V_{OL}	-	0.4	V	$I_{OL}=2.1mA$
VDD supply current	I_{DD}	-	100	mA	$V_{DD}=5V$
VPP supply current	I_{PP}	-	50	mA	$V_{PP}=12.5V$

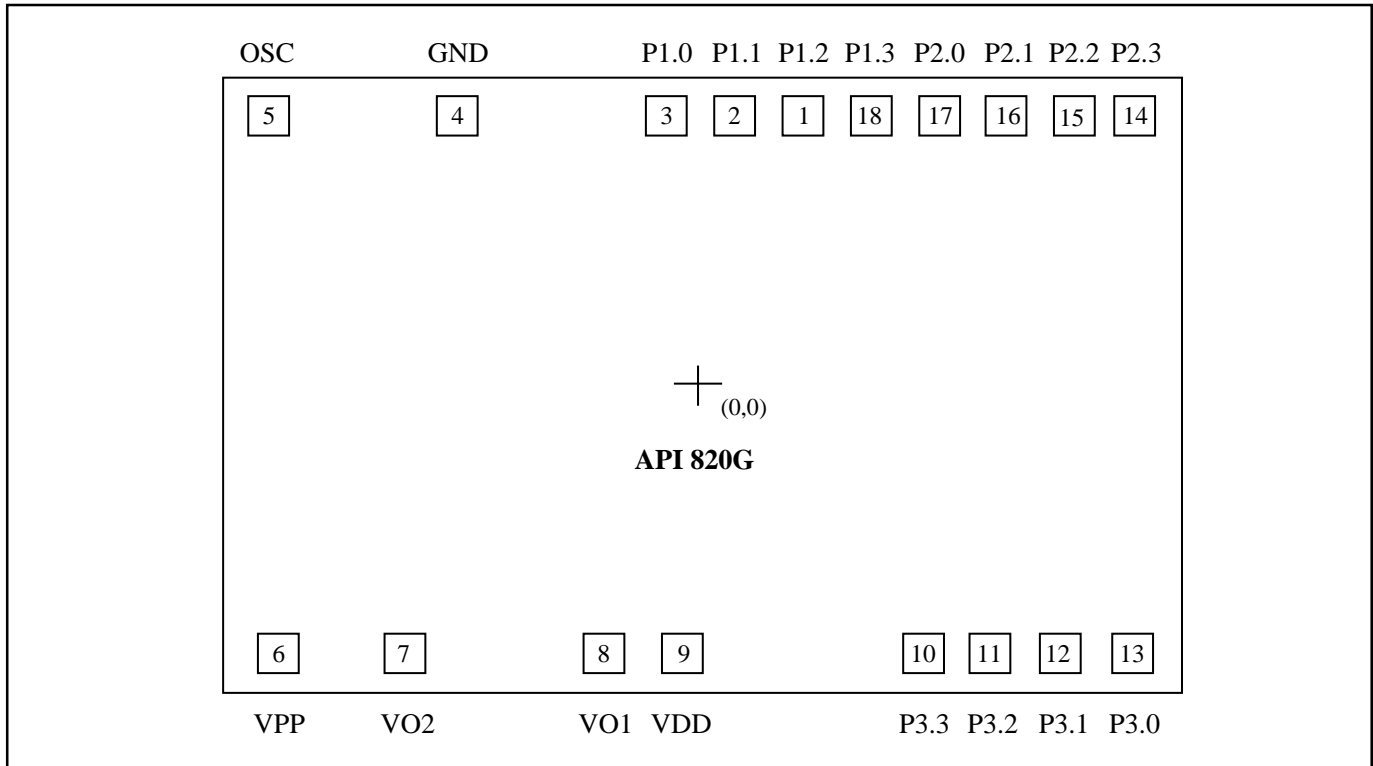
ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Min.	Max.	Unit
Supply Voltage	$V_{DD}-V_{SS}$	-0.3	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Operating Temperature	T_{OP}	0	70	$^{\circ}C$
Storage Temperature	T_{STG}	-55	+125	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($V_{DD} = 3V, 25^{\circ}C$ unless otherwise specified)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating voltage	V_{DD}	2.4	3.0	5.5	V	
Standby current	I_{DDS}	-	-	1.0	μA	$V_{DD}=3V$
Operating current	I_{DDO}	-	-	250	μA	$V_{DD}=3V$, No load
Drive current of P2,P3	I_{OD}	2.0	3.0	-	mA	$V_{DD}=3V$, $V_O=2.4V$
Sink current of P3	I_{OS}	2.3	3.5	-	mA	$V_{DD}=3V$, $V_O=0.4V$
Sink current of P2 (after KEYB)	I_{OS1}	2.3	3.5	-	mA	$V_{DD}=3V$, $V_O=0.4V$
Sink current of P2 (before KEYB)	I_{OS2}	-	3.0	10	μA	$V_{DD}=3V$, $V_O=0.4V$
Input current of P1	I_{IH}	-	3.0	10	μA	$V_{DD}=3V$
Output current of VO1, VO2	I_{VO}	4.0	5.0	6.0	mA	$V_{DD}=3V$, $V_O=0.7V$, two channel full scale output
Oscillation resistor	Rosc	-	100	-	K Ω	$V_{DD}=2.4V \sim 5.5V$
Oscillator frequency	Fosc	0.9	1.0	1.1	MHz	$V_{DD}=2.4V \sim 5.5V$
Oscillator frequency deviation	$\frac{\Delta F_{osc}}{F_{osc}}$	-10	-	10	%	$V_{DD}=2.4V \sim 5.5V$

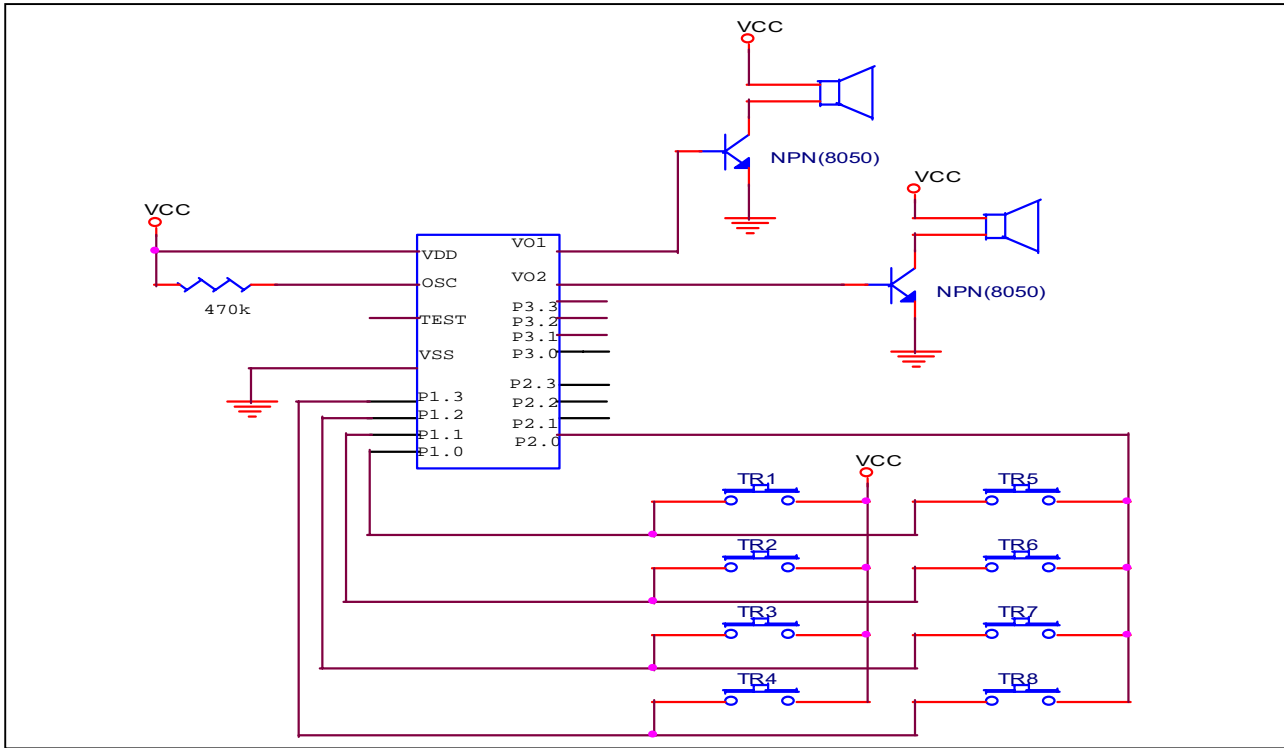
PAD DIAGRAM



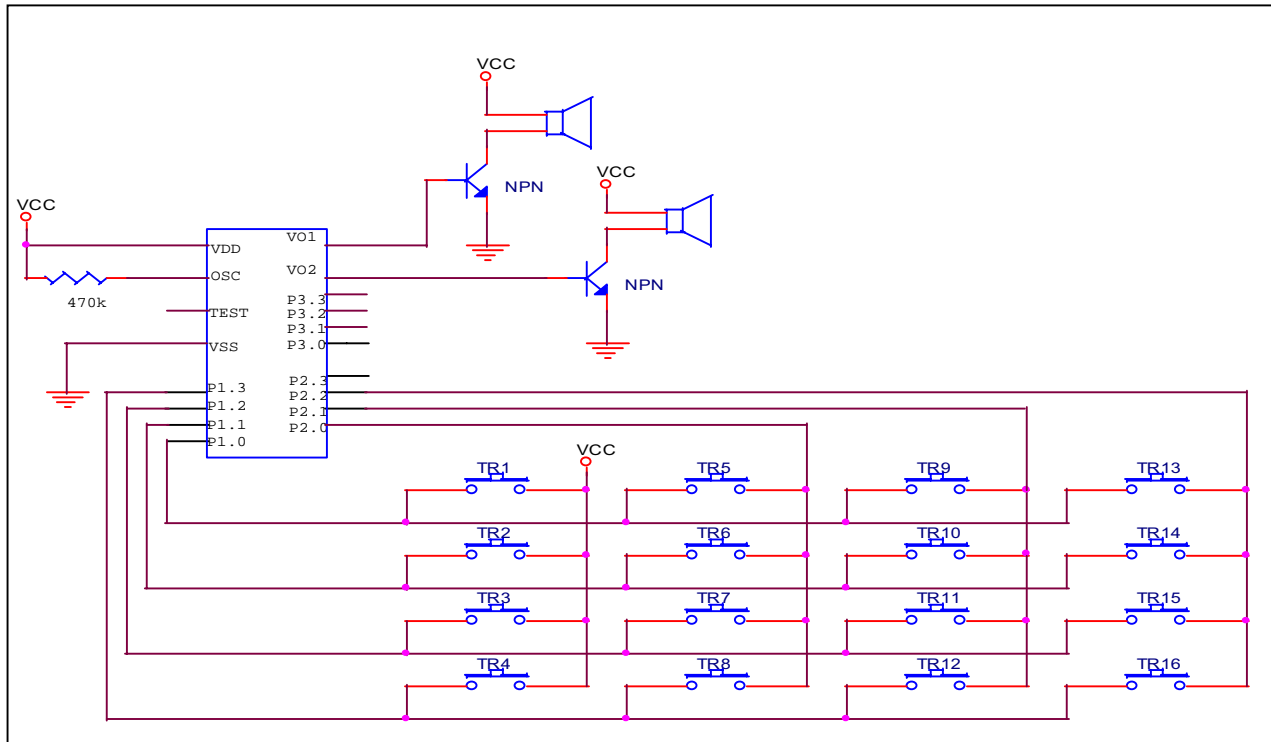
Chip Size : 2930 x 2100 um

For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	P1.2	325.8	900.6
2	P1.1	128.7	900.6
3	P1.0	-56.5	900.6
4	GND	-708.4	876.7
5	OSC	-1325.0	879.0
6	VPP	-1256.2	-890.0
7	VO2	-879.3	-890.0
8	VO1	-233.4	-890.0
9	VDD	-13.7	-878.4
10	P3.3	963.2	-878.4
11	P3.2	1084.1	-878.4
12	P3.1	1205.0	-878.4
13	P3.0	1325.9	-878.4
14	P2.3	1275.9	900.6
15	P2.2	1090.6	900.6
16	P2.1	893.5	900.6
17	P2.0	708.2	900.6
18	P1.3	511.1	900.6



8 Key Application Circuit



16 Key Application Circuit