DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC133
13-input NAND gate

Product specification
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

13-input NAND gate 74HC133

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The HC133 is an high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC133 provides the 13-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A..M to Y	C_L = 15 pF; V_{CC} = 5 V	9	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation per gate	notes 1 and 2	19	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For HC the condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
74HC133N	16	DIL	plastic	SOT38
74HC133D	16	SO	plastic	SOT109A

See also *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1..7, 10.. 15	A.. G, H..M	data input
8	GND	ground (0 V)
9	Y	data output
16	V_{CC}	positive supply voltage

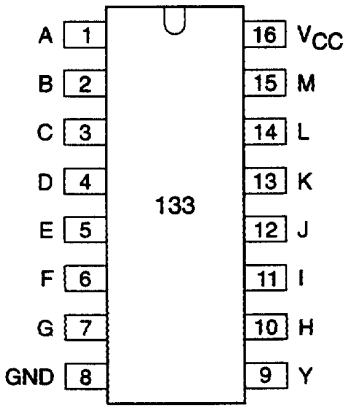


Fig.1 Pin configuration.

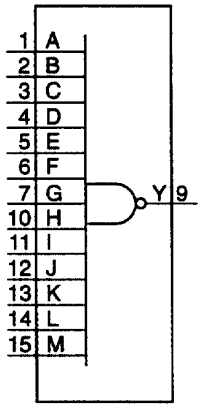


Fig.2 Logic symbol.

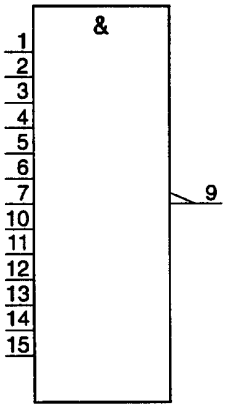


Fig.3 IEC logic symbol.

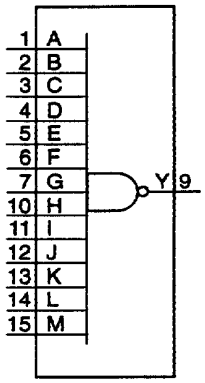


Fig.4 Functional diagram;
$Y = \overline{ABCDEFGHIJKLM}$.

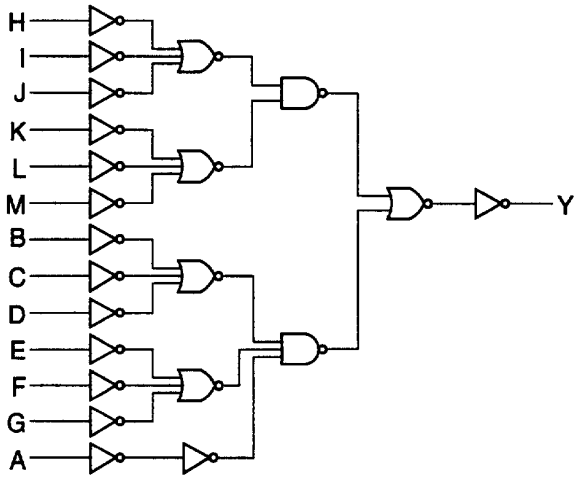


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS													OUTPUT
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**	**M**	**Y**
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	X	X	X	L	X	X	X	X	X	X	X	H
X	X	X	X	X	X	L	X	X	X	X	X	X	H
X	X	X	X	X	X	X	L	X	X	X	X	X	H
X	X	X	X	X	X	X	X	L	X	X	X	X	H
X	X	X	X	X	X	X	X	X	L	X	X	X	H
X	X	X	X	X	X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

DC CHARACTERISTICS FOR 74HC

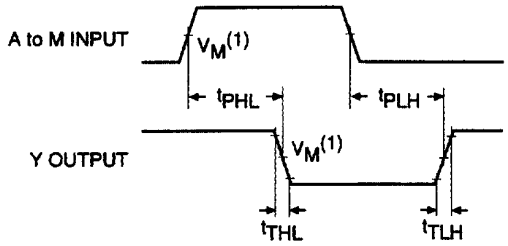
For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_f = t_r$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A..M to Y	– – –	36 13 10	110 22 19	– – –	140 28 23	– – –	165 33 28	ns	2.0 4.5 6.0	Fig.6
t_{THL}/t_{TLH}	output transition time	– – –	19 7 6	75 15 13	– – –	95 19 16	– – –	110 22 19	ns	2.0 4.5 6.0	Fig.6



(1) HC: V_M = 50%; V_I = GND to V_{CC}.

Fig.6 Waveforms showing the input (A, B, C, D, E, F, G, H, I, J, K, L, M) to output (Y) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.