NEC

MOS INTEGRATED CIRCUIT
μPD4704

EXTENSION 8-BIT UP/DOWN COUNTER
CMOS INTEGRATED CIRCUITS

DESCRIPTION

The μPD4704 is 8-bit up/down counters for extension of the μPD4702 incremental encoder counter. They perform an up/down-count using an 8-bit width with a μPD4702 carry or borrow signal as input. In addition, a carry output and borrow output are also provided for further extension of the count width, enabling extension to be performed in 8-bit units.

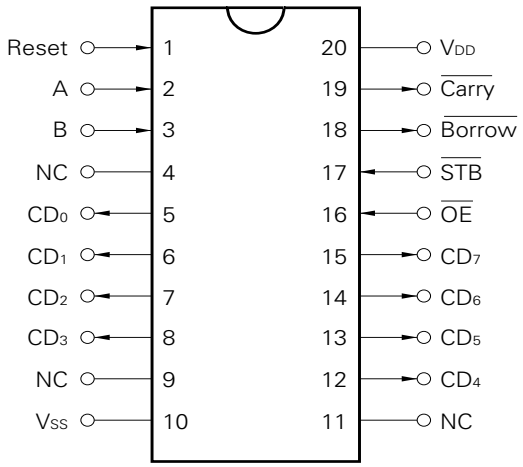
FEATURES

- 8-bit up/down counter for extension of μPD4702
- Count data output controllable (latch and 3-state output)
- Extension carry and borrow outputs
- CMOS, single +5 V power supply

PIN NAMES

$\overline{\text{Up}}$: Up-count input
$\overline{\text{Down}}$: Down-count input
$\overline{\text{Reset}}$: Counter reset input
$\overline{\text{STB}}$: Latch strobe signal input
$\overline{\text{OE}}$: Output control signal input
$\text{CD}_{0\text{-}7}$: Count data outputs
$\overline{\text{Carry}}$: Carry pulse output
$\overline{\text{Borrow}}$: Borrow pulse output

PIN CONFIGURATION (Top View)

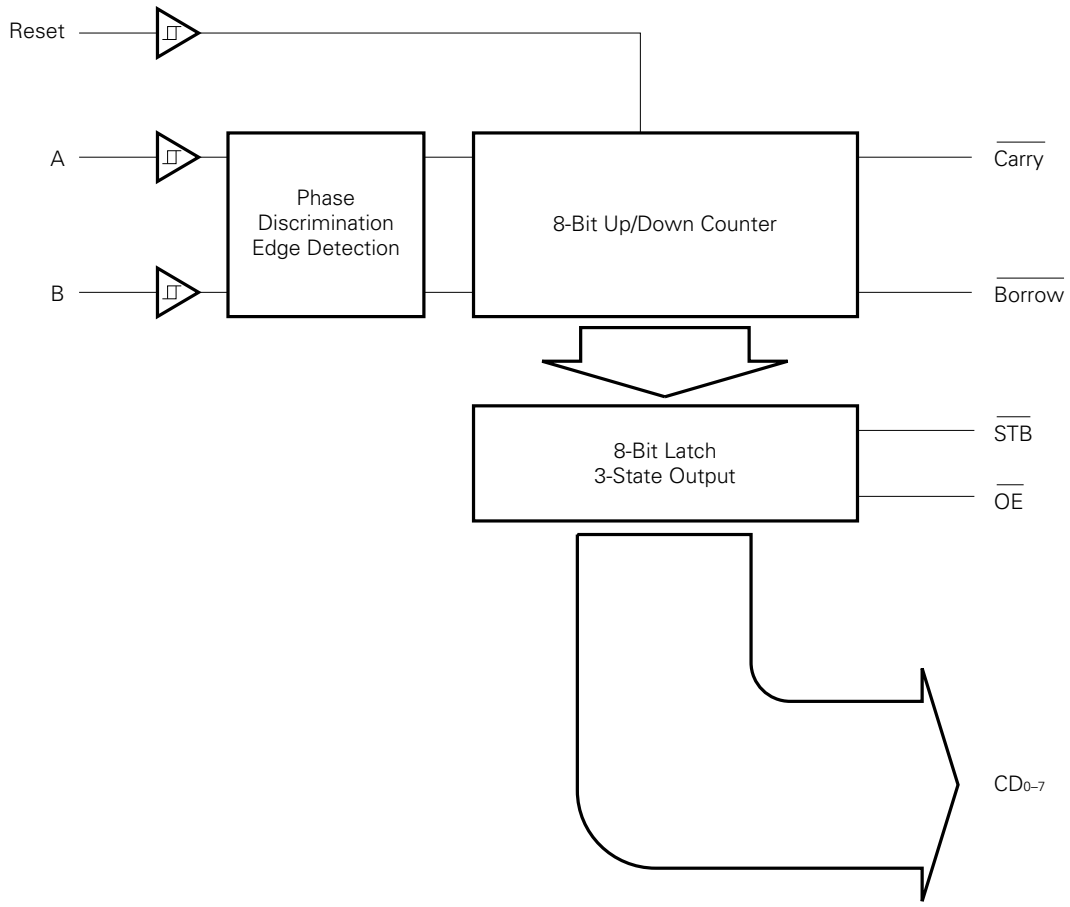


ORDERING INFORMATION

Part Number	Package
μPD4704C	20-pin plastic DIP (300 mil)
μPD4704G	20-pin plastic SOP (300 mil)

Document No. IC-3305A (2nd edition)
(O. D. No. IC-8762B)
Date Published April 1997 P
Printed in Japan

BLOCK DIAGRAM



PIN FUNCTIONS

Pin Name	Input/Output	Function
$\overline{\text{Up}}$ $\overline{\text{Down}}$	Input	Up-count & down-count signal input pins Count is performed on rise of signal.
$D_{0\text{ to }7}$	Output (3-state)	Count data output pins. Activated when $\overline{OE}$ is "L", high impedance outputs when $\overline{OE}$ is "H".
$\overline{\text{Carry}}$	Output	8-bit counter carry signal output pin (active-low)
$\overline{\text{Borrow}}$	Output	8-bit counter borrow signal output pin (active-low)
RESET	Input (Schmitt)	8-bit counter reset signal output pin Counter is reset when this pin is "H".
$\overline{OE}$	Input	Count data output control signal input pin
$\overline{STB}$	Input	Counter data output latch signal. Data is latched on the fall of $\overline{STB}$, and is held while $\overline{STB}$ = "L".
V_{DD}		Power supply input pin
GND		Ground pin

TRUTH TABLE 1 (COUNTER BLOCK)

×: H or L

$\overline{UP}$	$\overline{DOWN}$	RESET	$\overline{Carry}$	$\overline{Borrow}$	Remarks
×	×	H	×	×	Reset
H	↓	H	×	↓	Reset
H	↓	L	×	×	Down-count
↓	H	L	×	×	Up-count
L	↓	L	×	×	Disabled (count undefined)
↓	L	L	×	×	Disabled (count undefined)
H	L	L	H	L	Borrow output when count = 00_H
L	H	L	L	H	Carry output when count = $0FF_H$

TRUTH TABLE 2 (LATCH & OUTPUT BLOCKS)

×: H or L

$\overline{STB}$	$\overline{OE}$	CD_0 to CD_7
×	H	Output disable (3-state)
×	L	Output enable
H	×	Data through (count value load)
L	×	Data latch (count value retention)

1. DESCRIPTION OF OPERATIONS

(1) Count operation

The μPD4704 is designed as 8-bit up/down counter for extension of the μPD4702. The first-stage $\overline{\text{Carry}}$ output is connected to the $\overline{\text{UP}}$ input of the μPD4704, and similarly, the $\overline{\text{Borrow}}$ output is connected to the $\overline{\text{DOWN}}$ input. A count is executed on the rising edge of the $\overline{\text{UP}}$ input or $\overline{\text{DOWN}}$ input.

If the μPD4704 is to be used alone, without being connected to the μPD4702, either $\overline{\text{UP}}$ or the $\overline{\text{DOWN}}$ must be "H". If a count pulse is input to $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$ while the other is "L", the count value may change.

(2) Latch operation

An R-S flip-flop is inserted in the latch circuit input as shown in Fig. 1, and when $\overline{\text{STB}}$ is changed from "H" to "L" while the $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$ input is "L", the internal latch signal $\overline{\text{STB}}$' remains at "H" until the end of the count operation. Therefore, latching is not performed during a count operation. If $\overline{\text{STB}}$ changes from "H" to "L" $t_{SUDSTB1}$ (40 ns) or more after the falling edge of $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$, the post-count data is latched, and if $\overline{\text{STB}}$ changes from "H" to "L" within $t_{SUDSTB2}$ (10 ns) after the falling edge of $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$, then conversely, the pre-count data is latched.

Caution is required since, when $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$ is "L" (during a count operation), the latch operation is kept waiting even if $\overline{\text{STB}}$ is changed from "H" to "L", and therefore if a reset is executed the latch contents will also be reset (see Figs. 2 and 3).

Fig. 1 $\overline{\text{STB}}$ Input Circuit

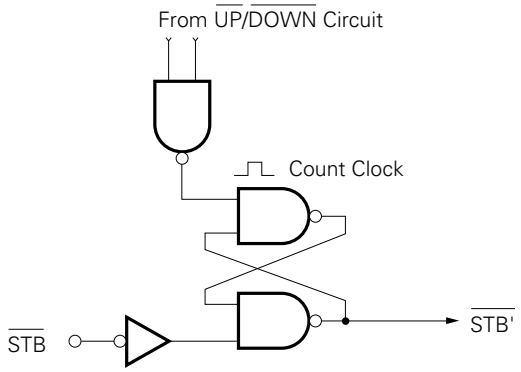


Fig. 2 Relation Between $\overline{STB}$ Timing and Counter Value

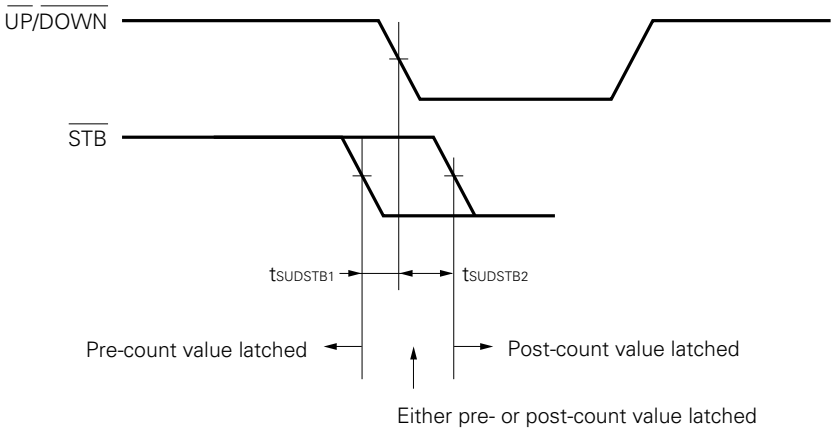
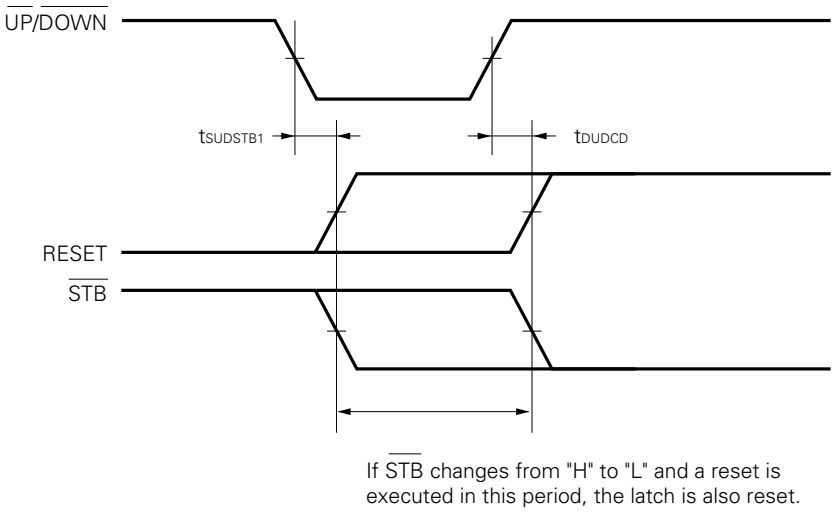


Fig. 3 $\overline{STB}$ and RESET Timing



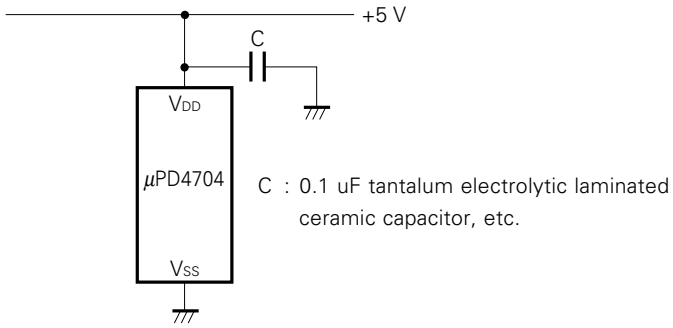
(3) Carry & borrow outputs

If the counter performs an up-count operation when the count value is 0FF$_H$, an active-low pulse is output to the $\overline{Carry}$ output (the pulse width is virtually the same as the $\overline{UP}$ or $\overline{DOWN}$ pulse L period). Similarly, if the counter performs a down-count operation when the count value is 00$_H$, an active-low pulse is output to the $\overline{Borrow}$ output. A $\overline{Borrow}$ pulse is also output if a down-count operation is performed while RESET is "H" (during a reset), and therefore, when a μPD4704 is added, a reset must be executed at the same time.

2. OPERATING PRECAUTIONS

As the μPD4704 incorporates an 8-bit counter, a large transient current flows in the case of a count value which changes all the bits (such as $00_H \leftrightarrow 0FF_H$ or $7F_H \leftrightarrow 080_H$). This will cause misoperation unless the impedance of the power supply line is sufficiently low. It is therefore recommended that a decoupling capacitor (of around 0.1 μF) be connected between V_{DD} and V_{SS} right next to the IC as shown in Fig. 4.

Fig. 4 Decoupling Capacitor



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS} = 0 V)

PARAMETER	SYMBOL	RATING		UNIT
Supply voltage	V_{DD}	–0.5 to +7.0		V
Input voltage	V_I	–1.0 to V_{DD} +1.0		V
Output voltage	V_O	–0.5 to V_{DD} +0.5		V
Operating temperature	T_{opt}	–40 to +85		°C
Storage temperature	T_{stg}	–65 to +150		°C
Permissible loss	P_D	500 (DIP)	200 (SOP)	mW

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING		UNIT
			MIN.	MAX.	
Input voltage low	V_{IL}			0.8	V
Input voltage high	V_{IH}	Reset	2.6		V
	V_{IH}	Other than the above	2.2		V
Output voltage low	V_{OL}	I_{OL} = 12 mA		0.45	V
Output voltage high	V_{OH}	I_{OH} = –4 mA	V_{DD} – 0.8		V
Static consumption current	I_{DD}	V_I = V_{DD}, V_{SS}		50	μA
Input current	I_I	V_I = V_{DD}, V_{SS}	–1.0	1.0	μA
3-state output leak current	I_{OFF}		–10	10	μA
Dynamic consumption current	$I_{DD\ dyn}$	f_{IN} = 16 MHz, C_L = 50 pF		12	mA
Hysteresis voltage	V_H	Reset	0.2		V

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
$\overline{Up}$ / $\overline{Down}$	Cycle	t_{CYCT}	f_{in} = 16 MHz	60		ns
	Input pulse width	t_{PWUDL}		25		ns
		t_{PWUDH}		35		ns
	Setup time	t_{SRSUD}		0		ns
	Up/down switchover setupt time	t_{SUDM}		100		ns
$CD_{0\ to\ 7}$	Reset time	t_{DRSCD}			60	ns
	Output delay	t_{DUDCD}			70	ns
	Output delay	t_{DOECD}			50	ns
	Output delay	t_{DSTBCD}			50	ns
	Float time	t_{FOECD}			40	ns
$\overline{Carry}$ / $\overline{Borrow}$	Output delay	t_{DUDCB1}			50	ns
		t_{DUDCB2}			100	ns
	Output pulse width	t_{PWCB}		30		ns
RESET	Reset pulse width	t_{PWRS}		40		ns
$\overline{STB}$	Setting time	$t_{SUDSTB1}$		40		ns
		$t_{SUDSTB2}$		10		ns

AC Timings

Fig. 1 Up/Down Signal Input Timing

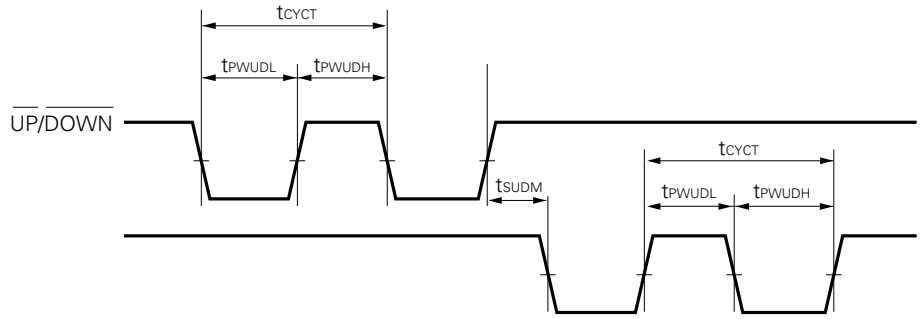


Fig. 2 Count Data Output Timing

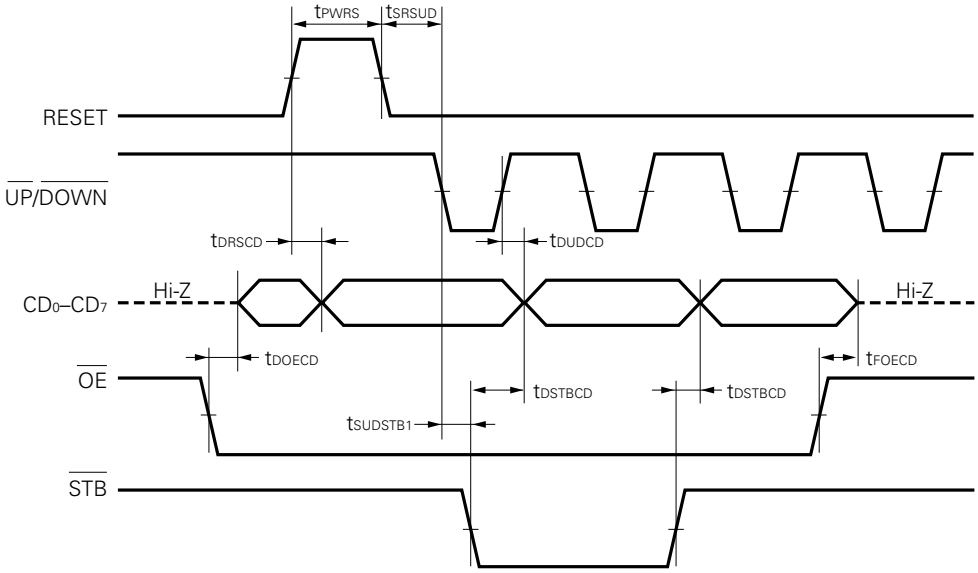


Fig. 3 Carry/Borrow Signal Output Timing

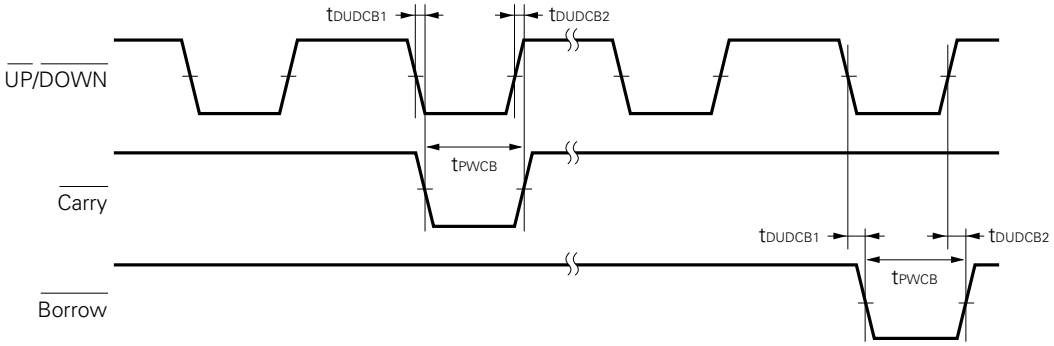
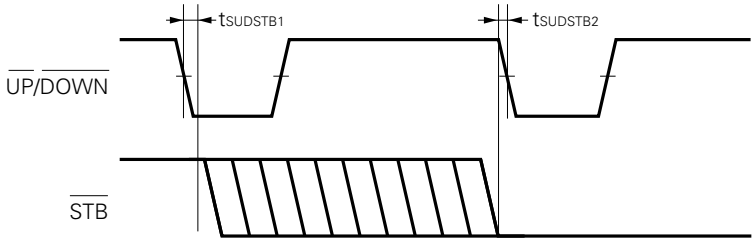
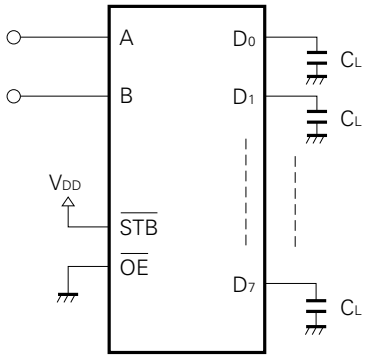


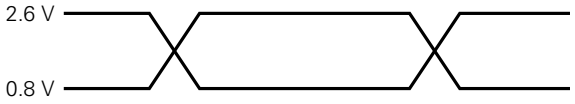
Fig. 4 Strobe Signal Output Timing



Consumption Current Measurement Circuit

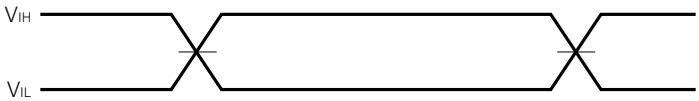


Measurement Conditions
A, B inputs
f_{IN} = 16 MHz



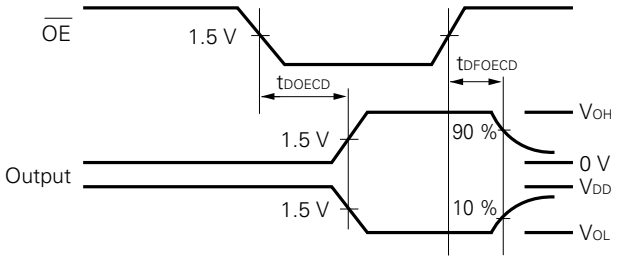
$\overline{STB}$ input connected to V_{DD} or $\overline{OE}$ input connected to V_{SS}.
Load on all outputs, C_L = 50 pF.

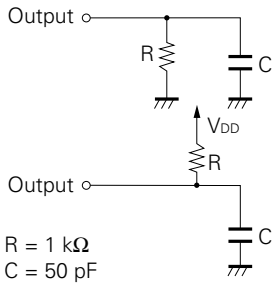
AC Test Input Waveform



V_{IH} = 2.6 V (RESET input)
V_{IH} = 2.2 V (inputs other than RESET)
V_{IL} = 0.8 V
Timing measurement is performed at 1.5 V.

- 3 state output

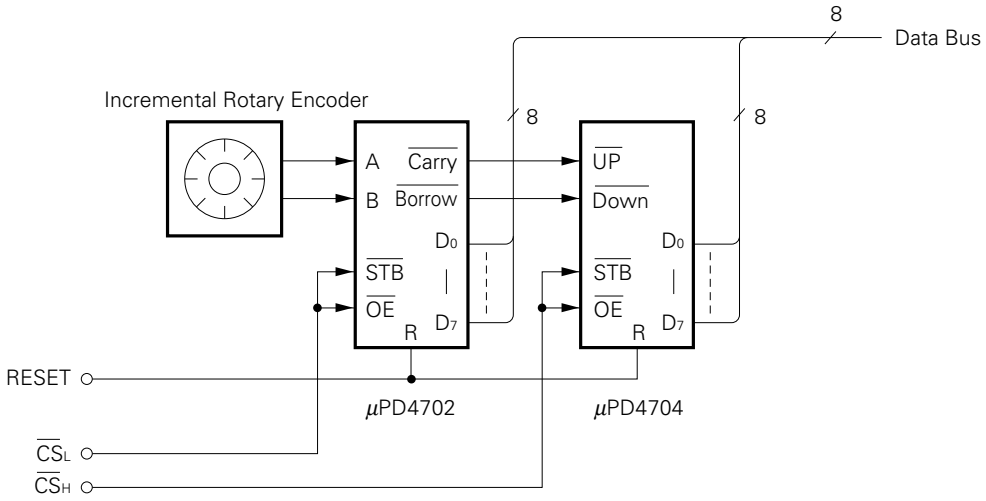




R = 1 kΩ
C = 50 pF

Sample Application Circuits

16-bit counter



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual" (IEI-1207)**.

μPD4704G

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: None	IR35-00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: None	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	○

* Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note Do not apply more than a single process at once, except for "Partial heating method".

TYPES OF THROUGH HOLE MOUNT DEVICE

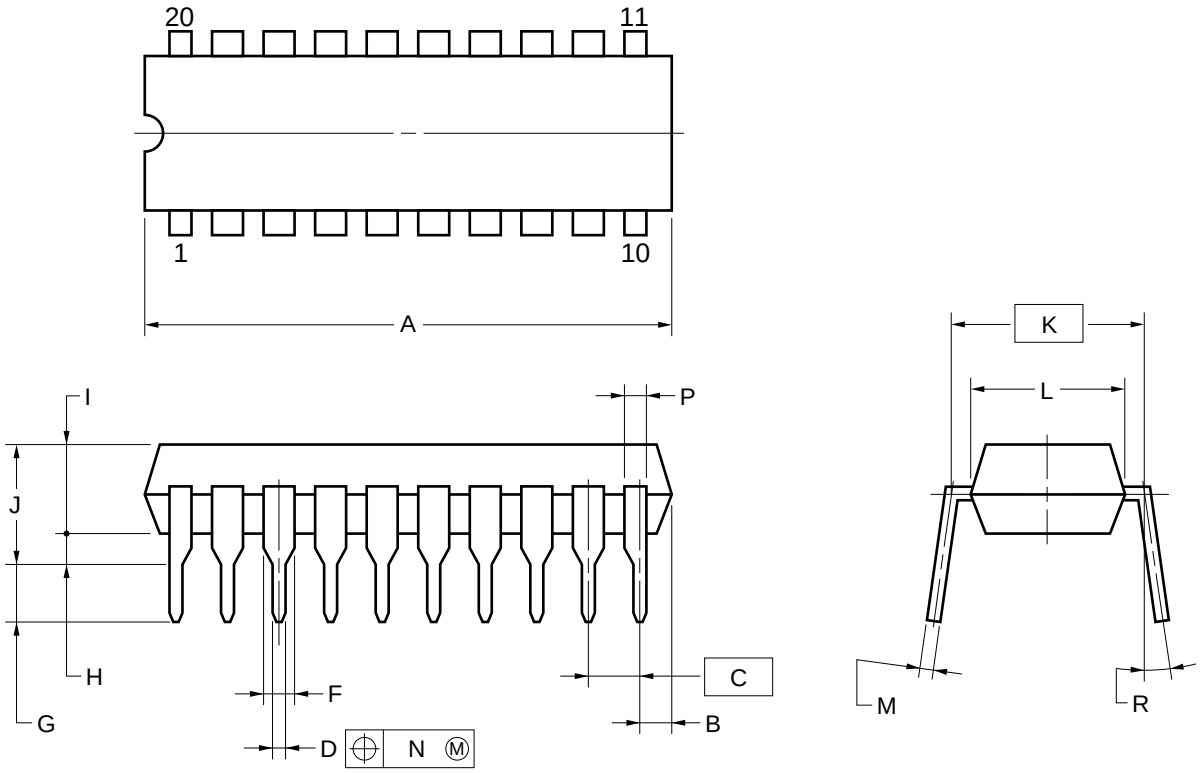
μPD4704C

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

REFERENCE

Dcodument name	Document No.
NEC semiconductor device reliability/quality control system	IEI-1212
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134

20PIN PLASTIC DIP (300 mil)



NOTES

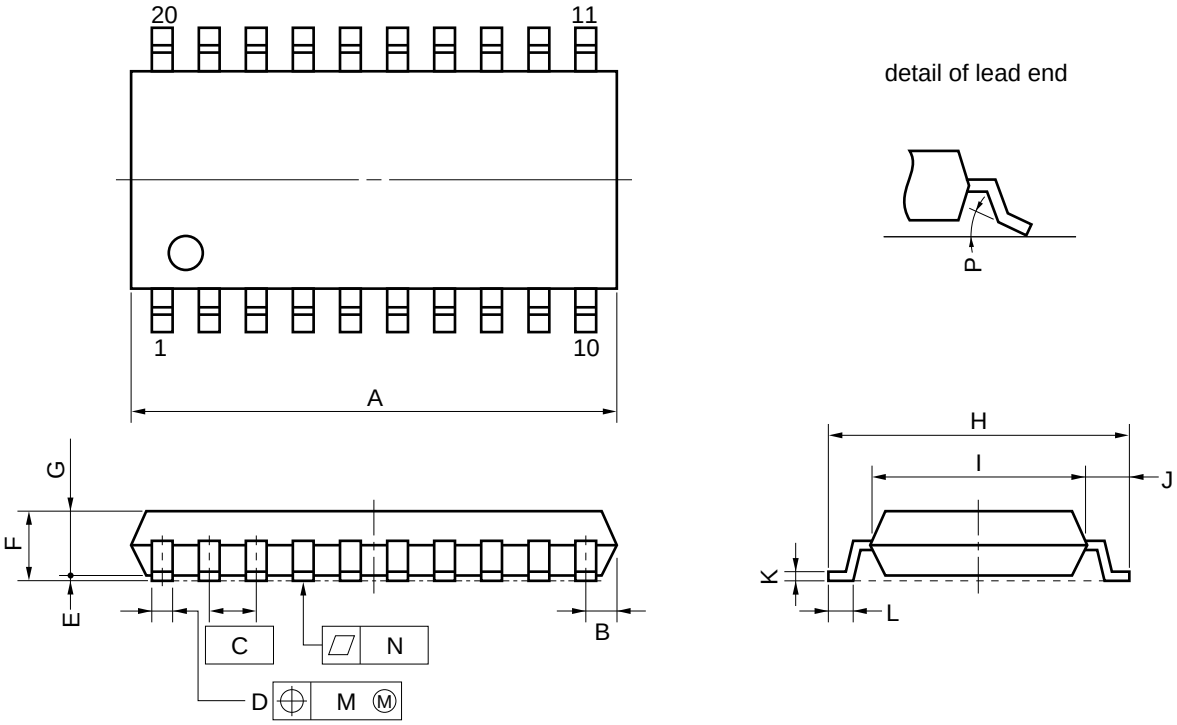
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	25.40 MAX.	1.000 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	3.5 ± 0.3	0.138 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P20C-100-300A,C-1

20 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P20GM-50-300B, C-4

[MEMO]

[MEMO]

[MEMO]

M4 96.5