DATA SHEET

BITSTREAM CONVERSION

UDA1361TS
96 kHz sampling 24-bit stereo audio ADC

Product specification
File under Integrated Circuits, IC01

2001 Jan 17

BITSTREAM CONVERSION

FEATURES

General

- Low power consumption
- 256, 384, 512 and 768f_s system clock
- 2.4 to 3.6 V power supply
- Supports sampling frequency of 5 to 110 kHz
- Small package size (SSOP16)
- Integrated high-pass filter to cancel DC offset
- Power-down mode
- Supports 2 V (RMS) input signals
- Easy application
- Master or slave operation.

Multiple format output interface

- I^2S-bus and MSB-justified format compatible
- Up to 24 significant bits serial output.

Advanced audio configuration

- Stereo single-ended input configuration
- High linearity, dynamic range and low distortion.

GENERAL DESCRIPTION

The UDA1361TS is a single chip stereo Analog-to-Digital Converter (ADC) employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording functions.

The UDA1361TS supports the I^2S-bus data format and the MSB-justified data format with word lengths of up to 24 bits.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1361TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
I_{DDA}	analog supply current	f_s = 48 kHz				
		operating mode	–	10.5	–	mA
		Power-down mode	–	0.5	–	mA
I_{DDD}	digital supply current	f_s = 48 kHz				
		operating mode	–	3.5	–	mA
		Power-down mode	–	0.45	–	mA
T_{amb}	ambient temperature		–40	–	+85	°C
Analog						
$V_{i(rms)}$	input voltage (RMS value)	at 0 dB(FS) equivalent	–	1.1	–	V
		at –1 dB(FS) signal output	–	1.0	–	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 48 kHz				
		at –1 dB	–	–88	–83	dB
		at –60 dB; A-weighted	–	–40	–34	dB
		f_s = 96 kHz				
		at –1 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–40	–37	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted				
		f_s = 48 kHz	–	100	–	dB
		f_s = 96 kHz	–	100	–	dB
α_{cs}	channel separation		–	100	–	dB

BLOCK DIAGRAM

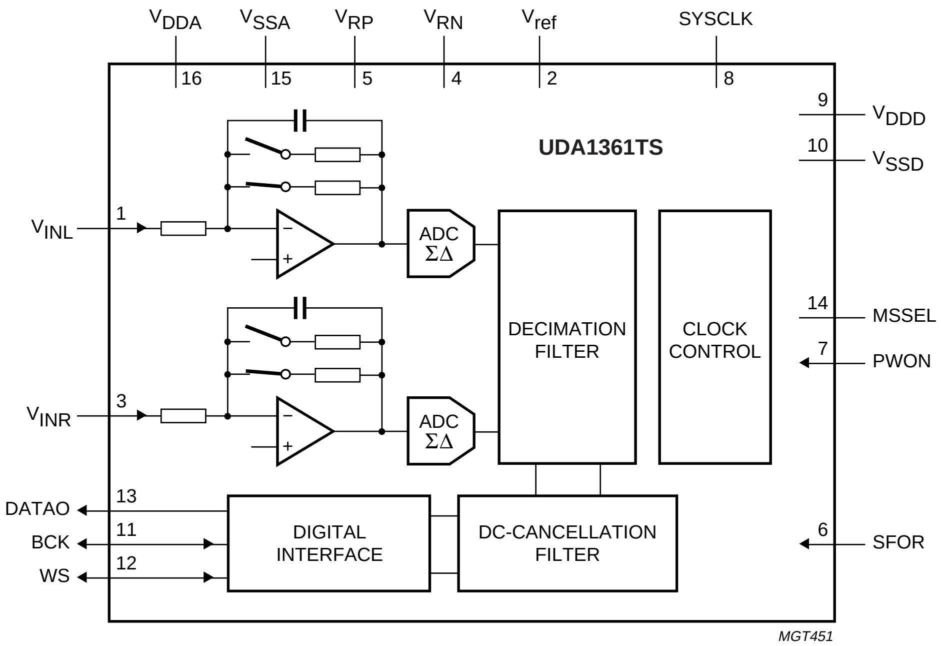


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{INL}	1	left channel input
V_{ref}	2	reference voltage
V_{INR}	3	right channel input
V_{RN}	4	negative reference voltage
V_{RP}	5	positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock 256, 384, 512 or 768f_s
V_{DDD}	9	digital supply voltage
V_{SSD}	10	digital ground
BCK	11	bit clock input/output
WS	12	word select input/output
DATAO	13	data output
MSSEL	14	master/slave select
V_{SSA}	15	analog ground
V_{DDA}	16	analog supply voltage

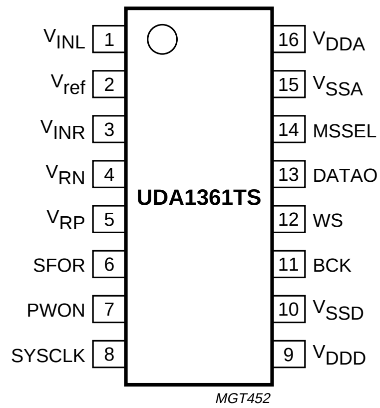


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System clock

The UDA1361TS accommodates master and slave modes. The system devices must provide the system clock regardless of master or slave mode. In the master mode a system clock frequency of $256f_s$ is required. In the slave mode a system frequency of 256, 384, 512 or $768f_s$ is automatically detected (for a system clock of $768f_s$ the sampling frequency must be limited to 55 kHz). The system clock must be locked in frequency to the digital interface input signals.

Input level

The overall system gain is proportional to V_{DDA}, or more accurately the potential difference between the reference voltages V_{VRP} and V_{VRN}. The –1 dB input level at which THD + N/S is specified corresponds to –1 dB(FS) digital output (relative to the full-scale swing). With an input gain switch, the input level can be calculated as follows:

$$\text{at 0 dB gain: } V_i(-1\ \text{dB}) = \frac{V_{VRP} - V_{VRN}}{3} = \text{V (RMS)}$$

$$\text{at 6 dB gain: } V_i(-1\ \text{dB}) = \frac{V_{VRP} - V_{VRN}}{2 \times 3} = \text{V (RMS)}$$

In applications where a 2 V (RMS) input signal is used, a 12 kΩ resistor must be connected in series with the input of the ADC. This forms a voltage divider together with the internal ADC resistor and ensures that only 1 V (RMS) maximum is input to the IC.

Using this application for a 2 V (RMS) input signal, the gain switch must be set to 0 dB. When a 1 V (RMS) input signal is input to the ADC in the same application the gain switch must be set to 6 dB.

An overview of the maximum input voltage allowed against the presence of an external resistor and the setting of the gain switch is given in Table . The power supply voltage is assumed to be 3 V.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE (RMS)
Present	0 dB	2 V
Present	0 dB	1 V
Absent	0 dB	1 V
Absent	6 dB	0.5 V

Multiple format output interface

The serial interface provides the following data output formats in both master and slave modes (see Figs 3, 4 and 5).

- I^2S-bus with data word length of up to 24 bits
- MSB-justified serial format with data word length of up to 24 bits.

The master mode drives pins WS (word select; $1f_s$) and BCK (bit clock; $64f_s$). WS and BCK are received in slave mode.

Table 2 Master/slave select

MSSEL	MASTER/SLAVE SELECT
L	slave mode
H	master mode
M	(reserved for digital test)

Table 3 Select data format

SFOR	DATA FORMAT
L	I^2S-bus data format
H	MSB-justified data format
M	(reserved for analog test)

Decimation filter

The decimation from $64f_s$ is performed in two stages. The first stage realizes a 4th-order sinx/x characteristic. This filter decreases the sample rate by 8.

The second stage, a FIR filter, consists of 3 half-band filters, each decimating by a factor of 2.

Table 4 Decimation filter characteristic

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_S$	±0.01
Pass-band droop	$0.45f_S$	–0.2
Stop band	>0.55 f_S	–70
Dynamic range	0 to 0.45 f_S	>135

DC cancellation filter

A IIR high-pass filter is provided to remove unwanted DC components. The filter characteristics are given in Table 5.

Table 5 DC cancellation filter characteristic

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	–	none
Pass-band gain	–	0
Droop	at $0.00045f_S$	–0.031
Attenuation at DC	at $0.00000036f_S$	>40
Dynamic range	0 to $0.45f_S$	>135

Mute

On recovery from Power-down, the serial data output DATAO is held LOW until valid data is available from the decimation filter. This time tracks with the sampling frequency:

$$t = \frac{12288}{f_s}$$, t = 256 ms when f_s = 48 kHz.

Power-down mode/input voltage control

The PWON pin can control the power saving together with the optional gain switch for 2 or 1 V (RMS) input.

The UDA1361TS supports 2 V (RMS) input using a series resistor of 12 kΩ. For the definition of the pin settings for 1 or 2 V (RMS) mode, it is assumed that this resistor is present as a default component.

Table 6 Power-down/input voltage control

PWON	POWER-DOWN OR GAIN
L	Power-down mode
M	0 dB gain
H	6 dB gain

Serial interface formats

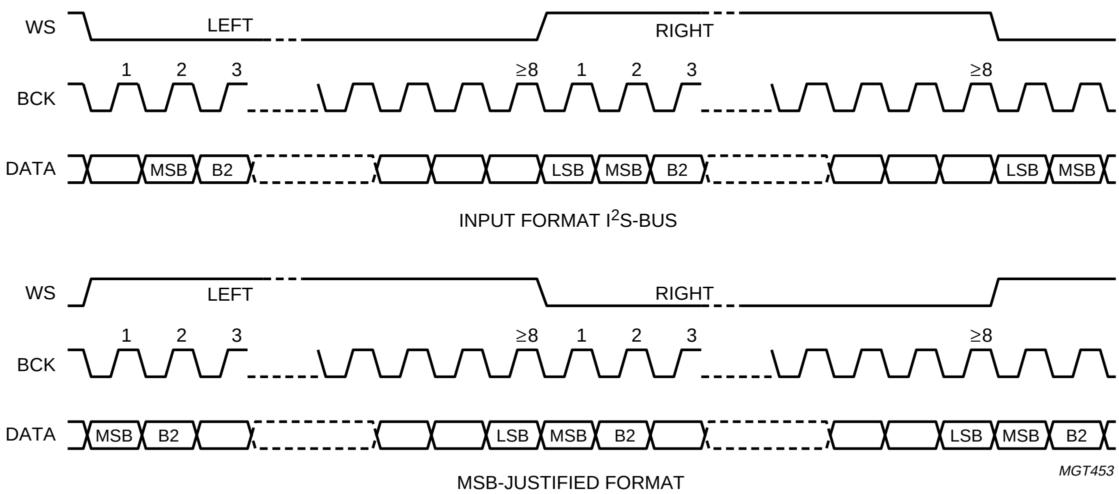


Fig.3 Serial interface formats.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	4.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	HBM; note 2	–3000	+3000	V
		MM; note 2	–300	+300	V

Notes

1. All supply connections must be made to the same power supply.
2. ESD behaviour is tested in accordance with JEDEC II standard:
   a) Human Body Model (HBM); equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
   b) Machine Model (MM); equivalent to discharging a 200 pF capacitor through a 0.75 µH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{(th\ j\text{-}a)}$	thermal resistance from junction to ambient	in free air	130	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 3$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 10 and 15); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
I_{DDA}	analog supply current	$f_s = 48$ kHz				
		operating mode	–	10.5	–	mA
		Power-down mode	–	0.5	–	mA
		$f_s = 96$ kHz				
		operating mode	–	10.5	–	mA
		Power-down mode	–	0.5	–	mA
I_{DDD}	digital supply current	$f_s = 48$ kHz				
		operating mode	–	3.5	–	mA
		Power-down mode	–	0.45	–	mA
		$f_s = 96$ kHz				
		operating mode	–	7.0	–	mA
		Power-down mode	–	0.65	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pin (SYSCLK)						
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
V_{IL}	LOW-level input voltage		–0.5	–	+0.8	V
$\|I_{LI}\|$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
Digital 3-level input pins (PWON, SFOR, MSSEL)						
V_{IH}	HIGH-level input voltage		$0.9V_{DD}$	–	$V_{DD} + 0.5$	V
V_{IM}	MIDDLE-level input voltage		$0.4V_{DD}$	–	$0.6V_{DD}$	V
V_{IL}	LOW-level input voltage		–0.5	–	+0.4	V
Digital input/output pins (BCK, WS)						
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
V_{IL}	LOW-level input voltage		–0.5	–	+0.8	V
$\|I_{LI}\|$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
V_{OH}	HIGH-level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
Digital output pin (DATAO)						
V_{OH}	HIGH-level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
Analog						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
R_I	input resistance		–	12	–	kΩ
C_I	input capacitance		–	20	–	pF

Note

1. All power supply connections must be connected to the same external power supply unit.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = 3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 10 and 15); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$V_{i(rms)}$	input voltage (RMS value)	at 0 dB(FS) equivalent	1.1	–	V
		at –1 dB(FS) signal output	1.0	–	V
$\lvert \Delta V_i \rvert$	unbalance between channels		<0.1	0.4	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 48 kHz			
		at –1 dB	–88	–83	dB
		at –60 dB; A-weighted	–40	–34	dB
		f_s = 96 kHz			
		at –1 dB	–85	–80	dB
		at –60 dB; A-weighted	–40	–37	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted			
		f_s = 48 kHz	100	–	dB
		f_s = 96 kHz	100	–	dB
α_{cs}	channel separation		100	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 30 mV (p-p)	30	–	dB

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA}$ = 2.4 to 3.6 V; T_{amb} = –40 to +85 °C; all voltages referenced to ground (pins 10 and 15); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock timing						
T_{sys}	system clock cycle	$f_{sys} = 256f_s$	35	88	780	ns
		$f_{sys} = 384f_s$	23	59	520	ns
		$f_{sys} = 512f_s$	17	44	390	ns
		$f_{sys} = 768f_s$	17	30	260	ns
t_{CWL}	LOW-level system clock pulse width		$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_{CWH}	HIGH-level system clock pulse width		$0.40T_{sys}$	–	$0.60T_{sys}$	ns
Serial data timing						
$T_{cy(CLK)(bit)}$	bit clock period	$f_{cy} = \frac{1}{T_{cy}}$; master mode	$64f_s$	$64f_s$	$64f_s$	Hz
		$f_{cy} = \frac{1}{T_{cy}}$; slave mode	–	–	$64f_s$	Hz
t_{BCKH}	bit clock HIGH time		50	–	–	ns
t_{BCKL}	bit clock LOW time		50	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{d(o)(D)(BCK)}$	data output delay time (from BCK falling edge)		–	–	40	ns
$t_{d(o)(D)(WS)}$	data output delay time (from WS edge)	MSB-justified format	–	–	40	ns
$t_{h(o)(D)}$	data output hold time		0	–	–	ns
$t_{r(WS)}$	word select rise time		–	–	20	ns
$t_{f(WS)}$	word select fall time		–	–	20	ns
f_{WS}	word select period		1	1	1	f_s
$t_{d(WS)(BCK)}$	word select delay from BCK	master mode	–40	–	+40	ns
$t_{su(WS)}$	word select set-up time	slave mode	20	–	–	ns
$t_{h(WS)}$	word select hold time	slave mode	10	–	–	ns

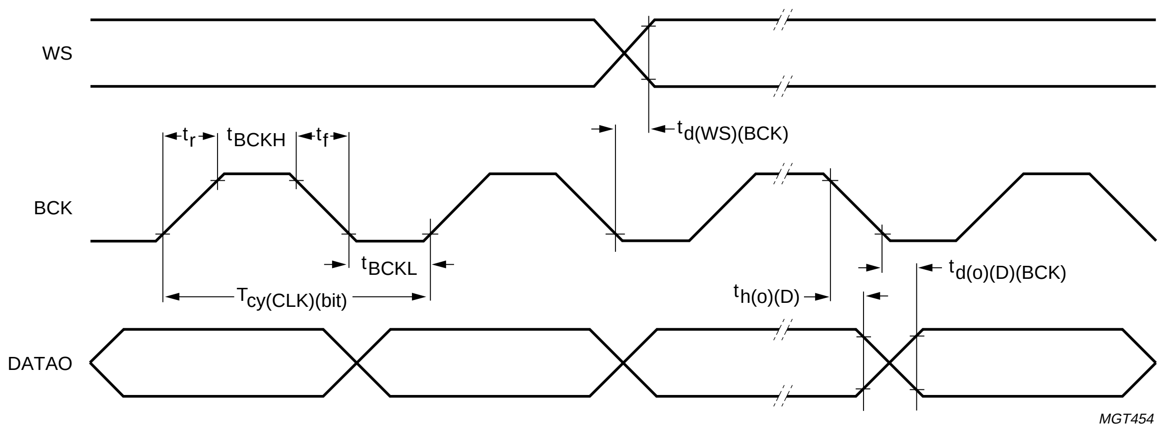


Fig.4 Serial interface master mode timing.

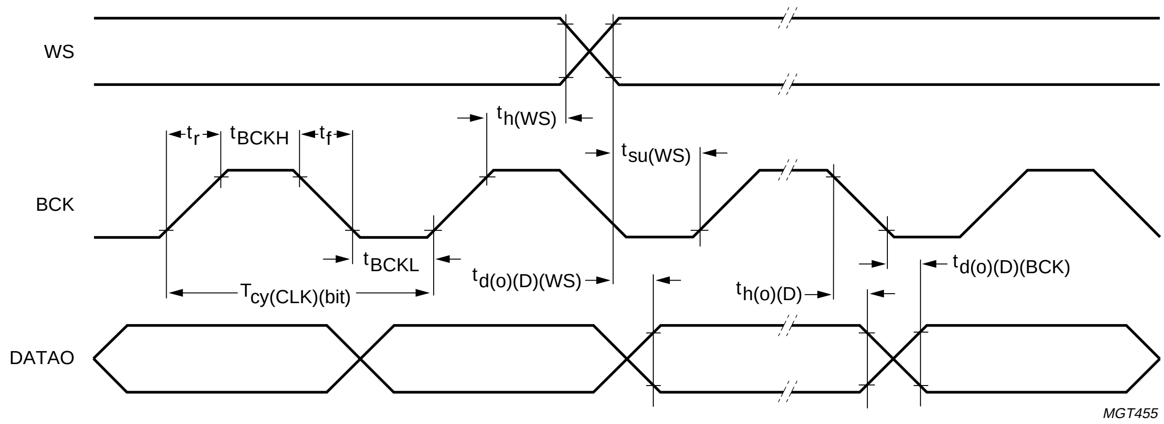
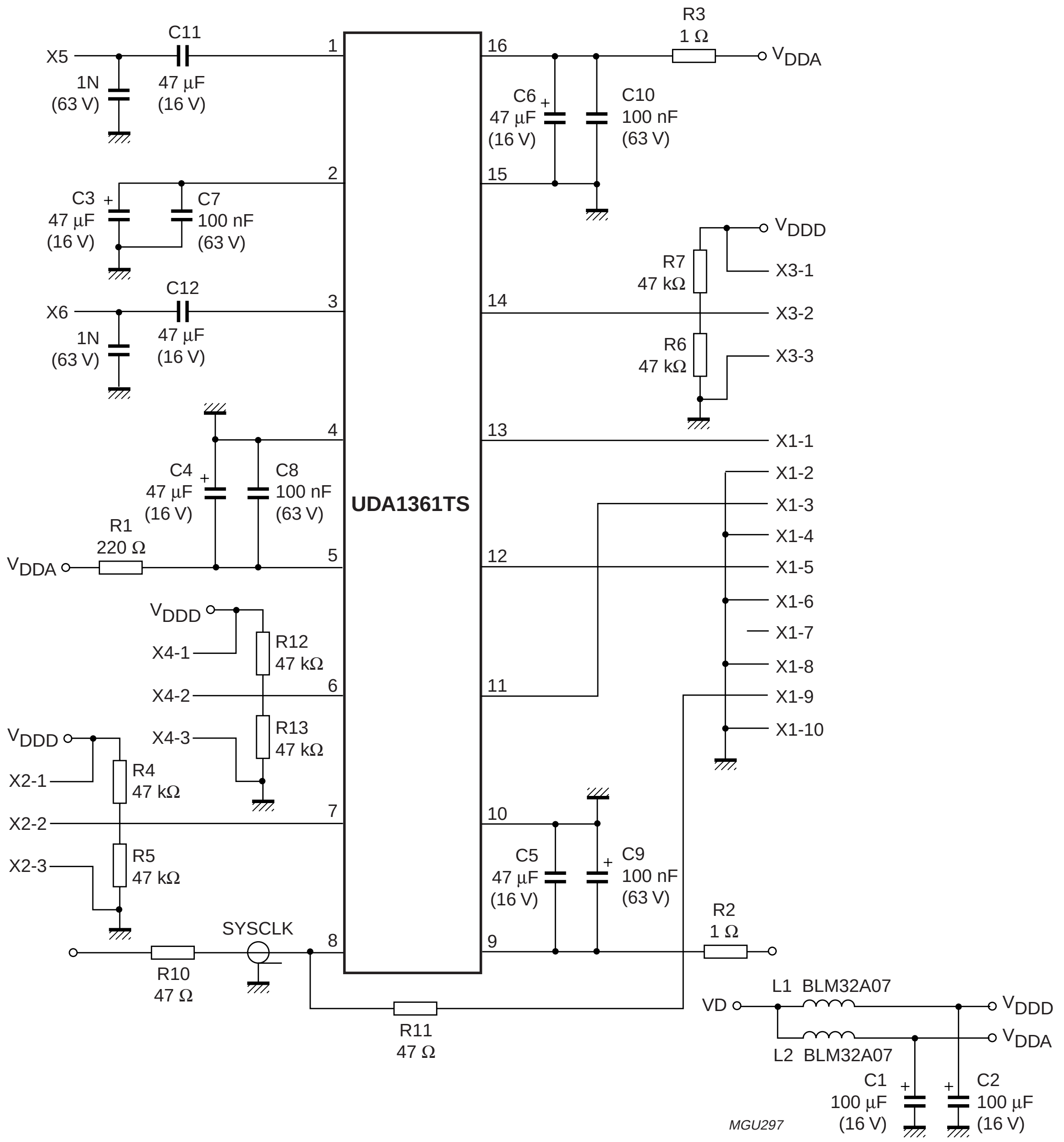


Fig.5 Serial interface slave mode timing.

APPLICATION INFORMATION

The application information illustrated in Fig.6, is an optimum application environment. Simplification is possible at the cost of some performance degradation.

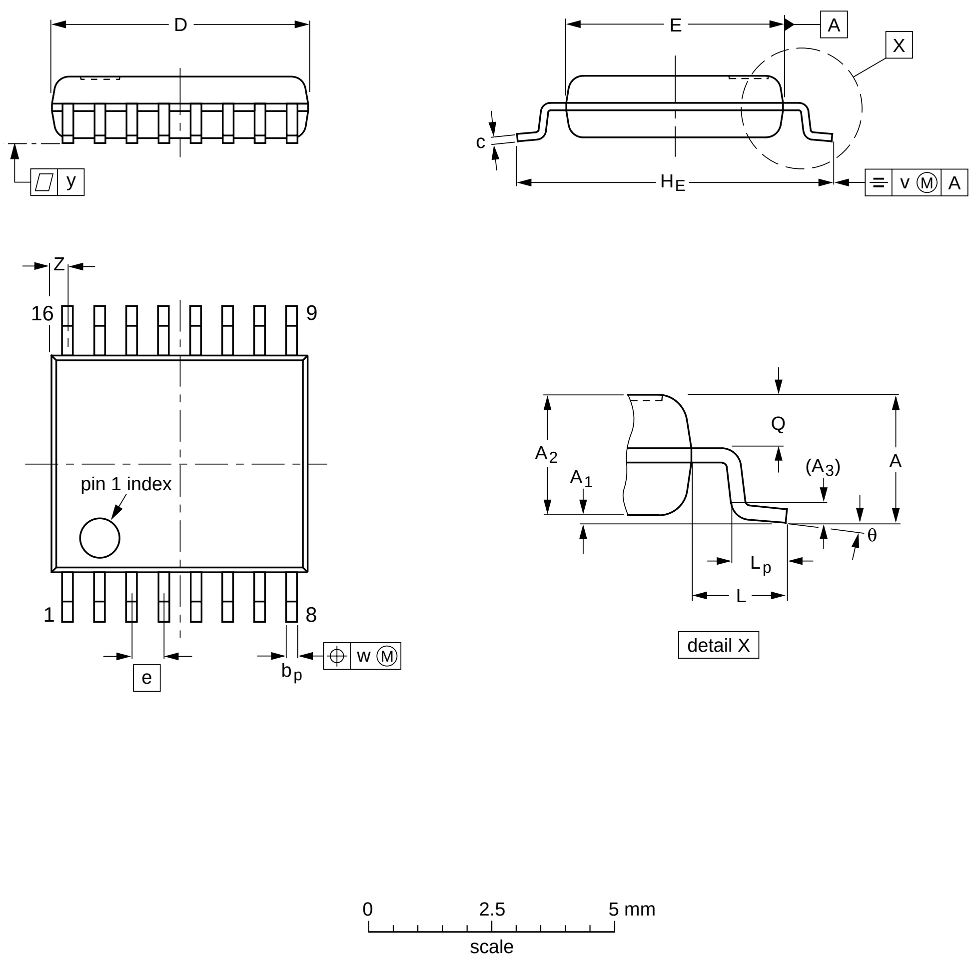


The capacitors at the input of the ADC can be reduced. It should be noted that the cut-off frequency of the capacitor with the 12 kW input resistance of the ADC will also change.

Fig.6 Application diagram.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1		MO-152				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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